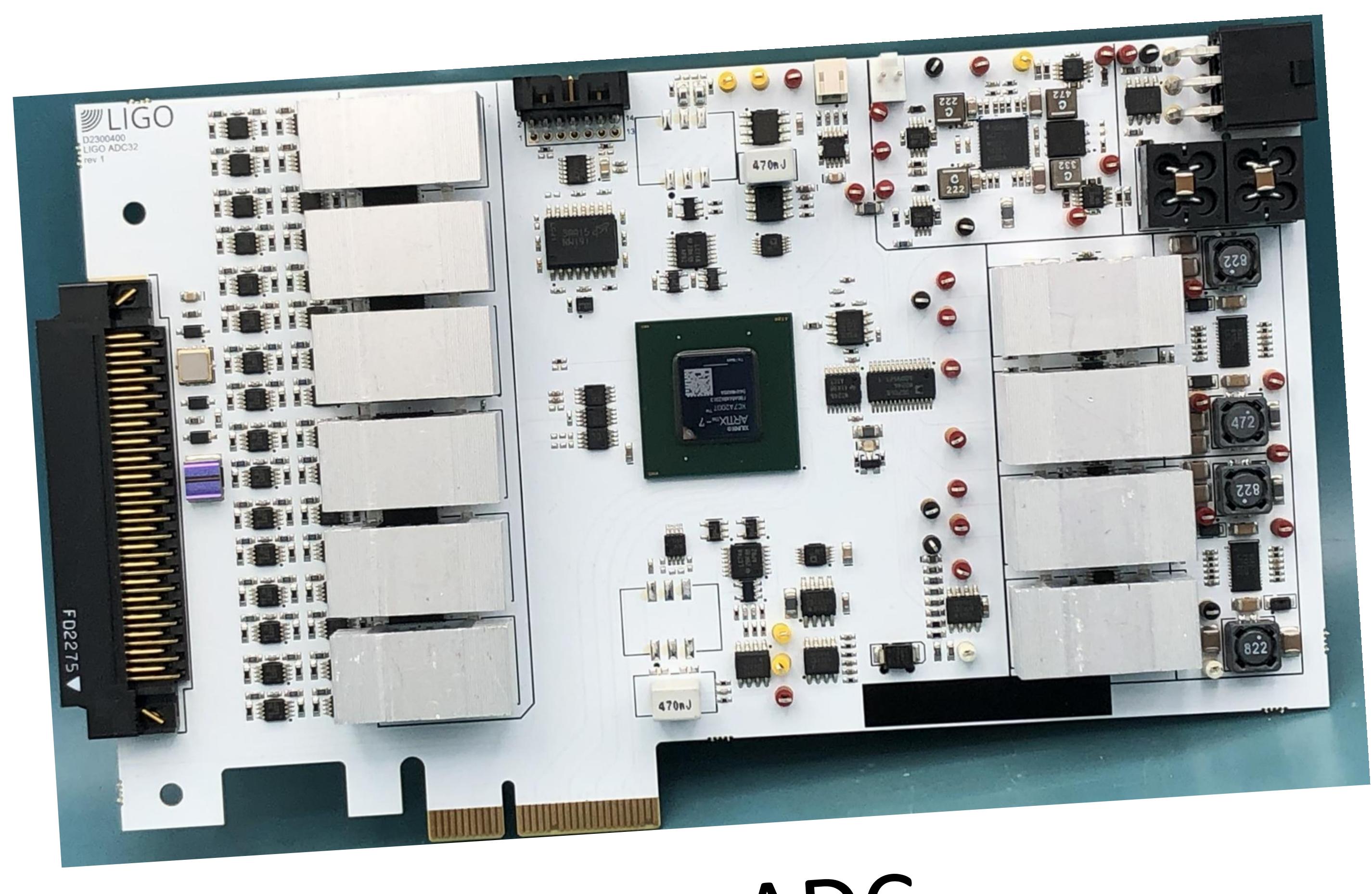


# Converter Refresh for Future LIGO Upgrades

Daniel Sigg & Marc Pirello

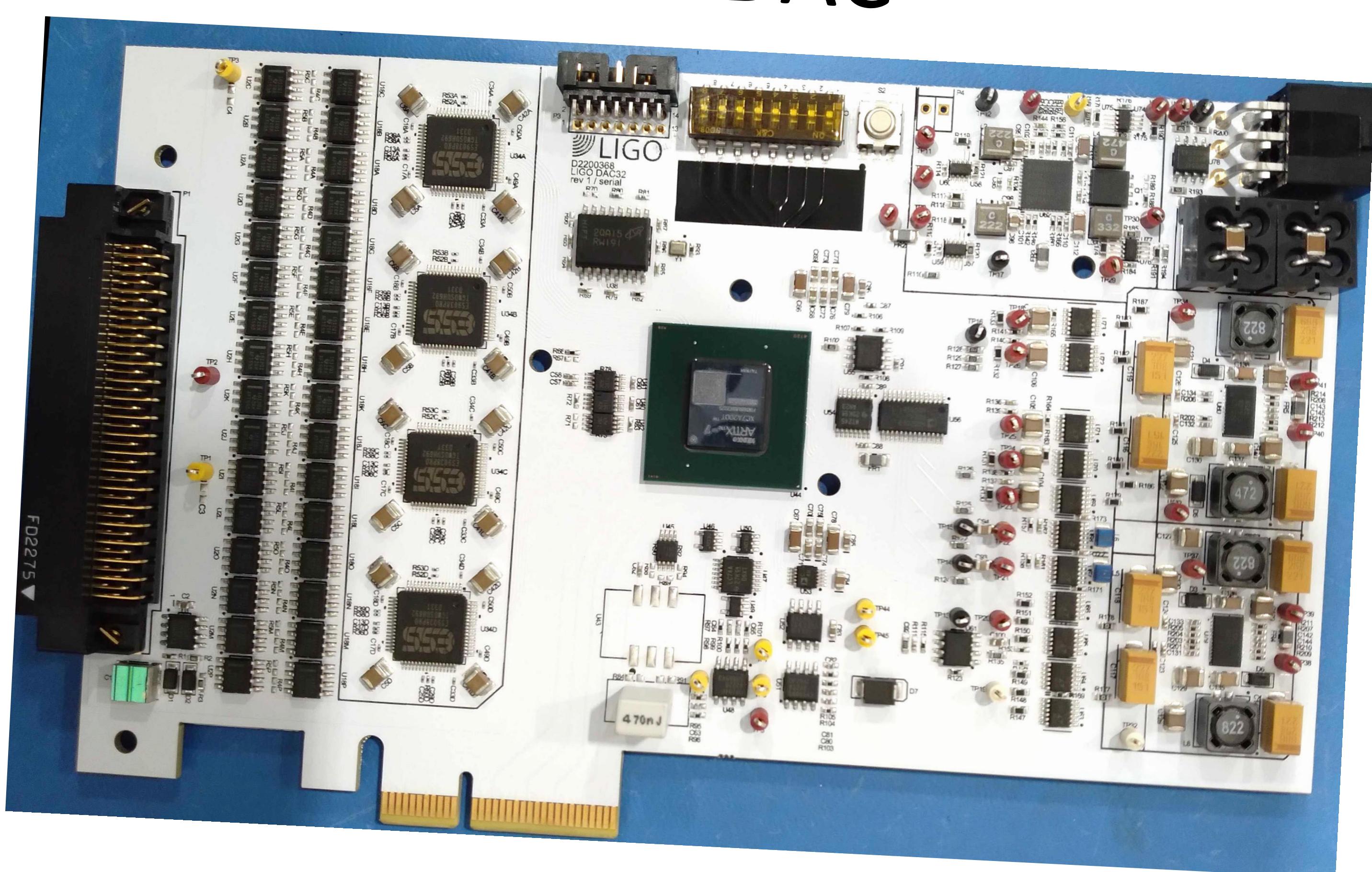
## Features:

- 32-Channels / Differential
- $\Sigma\Delta$ -Technology w/ IIR Filters
- Faster Sampling Rates
- AA/AI Filters in FPGA
- Timing System Integration
- Time Stamped Data thru DMA



New ADC

New DAC



## Performance:

- ADC  $\pm 20V$  / DAC  $\pm 10V$
- DAC: 50nV/VHz @ 100Hz
- ADC: 200nV/VHz (prelim.)
- No Rogue Lines/Oscillators
- Full RTCDS Integration
- DAC: 6 Months Running at H1
- DAC: see T2400066

## Future Developments:

- Fast Digital Servo 10-100kHz Bandwidth
- ADC → FPGA → DAC
- Sampling Rate  $\approx 8MHz$
- 4-8 Inputs & 2-4 Outputs
- Switchable Whitening
- Integration with RTCDS

G2500359-v1

