LIGO Converter Design
Common Mode Board Functionality

Daniel Sigg and Marc Pirello

LIGO Hanford Observatory

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Concepts

- Basic Features: see G2201990
- Build on Analog Devices' Quad Channel, Low Latency, Data Acquisition and Signal Generation Module CN0585 and CN0584.
  - 4 channel input (16-bit) & 4 channel output (16-bit)
  - Will support 2^{23} Hz (~8.4 MHz) sampling clock
  - ADC: ADAQ23876 (could upgrade to 18-bit with ADAQ23878)
  - DAC: AD3552R
  - Quoted input-to-output latency: 250ns (running at 15MSPS);
    ~500ns maybe more realistic for us → 18 degrees phase loss at 100kHz
- Will have to think about whitening filters
  - SNR 91.5dB (ADAQ23878) → ~100nV/√Hz @ ±10V input
  - How much is needed? Switching?
- Integration with RTCDS: same as DAQ (albeit not at full rate)

Concepts (2)

- Chassis located in field rack?
  - Remote PCIe, e.g., Adnaco RA3-01 (has a minimum order of 50)
  - Power supply synchronized to GPS. Is this enough?
  - Would need separate timing interface fiber
  - Could connect directly to computer through fiber
- Support chassis to chassis interconnects?
  - Current common mode servo feeds back to mode cleaner servo
  - Could use gigabit links over fiber, e.g., Aurora protocol (simple point-to-point serial)
- Support RF demodulation?
  - For example LTC2107 sampling at 2^{28} Hz (~134 MHz).
  - Under sample for frequencies >2^{27} Hz.
  - SNR 79.5 dBFS → ~10nV/√Hz @ ±1.2V input
  - Delay small < 60ns, but processing time needed for demodulation
  - Stability of demodulation phase?

Concepts (3)

- FPGA:
  - XC7A200T-2
    - 740 DSP slices
    - up to 16 gigabit receivers, PCIe Gen 2
  - XCAU25P-2
    - 1200 DSP slices
    - 12 gigabit receivers, PCIe Gen 3
    - Could move up to even bigger chips KU3P/KU5P with 1368/1824 DSP slices
  - For testing could use Opal Kelly XEM8310 development board
  - More recent GHz-converters use gigabit receivers
  - Older GHz-converters use 8 or 16 parallel LVDS lanes + clock & sync

Proposed R&D: Develop 2 Prototypes

- Fast 100kHz servo board
  - Target application: common mode board and similar
  - Sampling rate around 8MHz
  - 4-8 inputs & 2-4 outputs
  - Includes switchable whitening
  - Fiber gigabit links to other chassis
- RF receiver with integrated demodulation,
  - Target application: wavefront sensors, slower servos (<<10kHz BW)
  - Sampling rate for RF front-end >100MHz
  - Sampling rate after demodulation 1-8 MHz
  - Up to 6 RF inputs (4 RF signals + 2 demodulation signal)
  - Optional 2-4 lower frequency outputs
  - Fiber gigabit links to other chassis

Support R&D

- Remote PCIe over fiber
  - Test Adnaco RA3
  - Direct fiber receiver possible? Adnaco PCIe clock is 101MHz!
- Fiber point-to-point links
  - Protocol & gigabit/SFP solution
  - Latency
  - Clock: can we use 2^N clock?
- RF Demodulation
  - Local demodulation signal numerically generated in the FPGA
    - Phase stability of timing system good enough?
    - Requires re-sampling and resynchronization?
- Chassis power
  - Noise injection & ground contamination