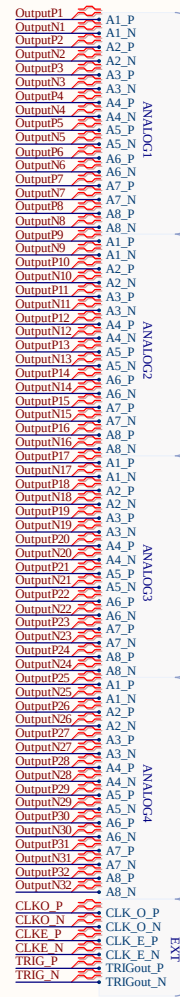
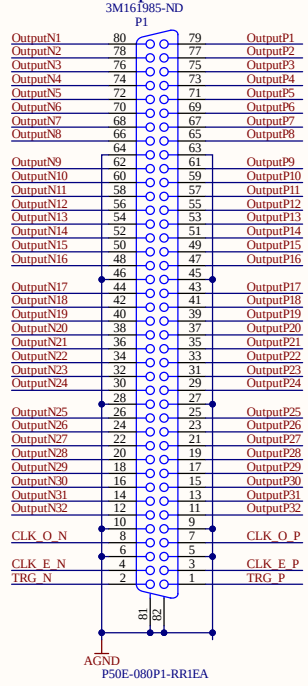
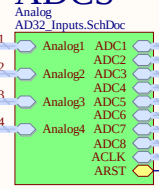




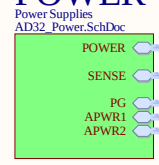
Diff Outputs to IFO



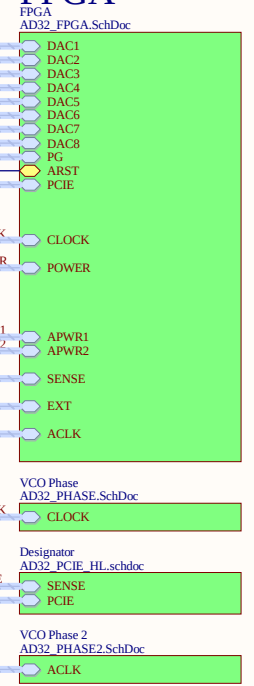
ADCS



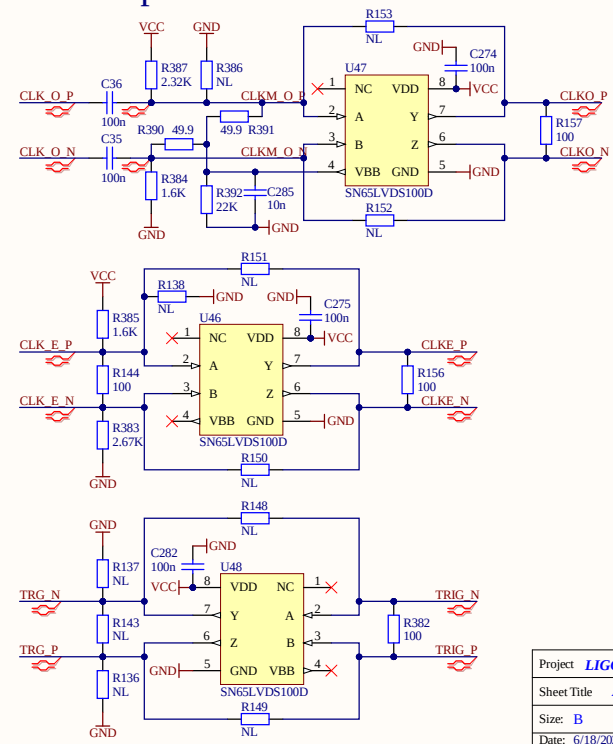
POWER



FPGA



Input Clock Buffers



Power Usage:
3x SN65LVDS100D
25mA * 3.3V * 3 = 247mW

Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power:
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD - VCCAUX
VCC1V0 = VCCINT - VCCBRAM

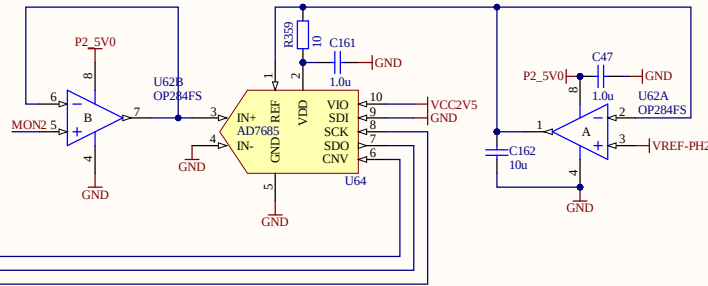
PCIE
AVTT = 1.2V
AVCC = 1.0V

Project LIGO ADC 32			LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation		
Sheet Title ADC Top Sheet					
Size: B	DCC D2300400	Rev: 2			
Date: 6/18/2026	Time: 11:50:49 AM	Sheet: 1 of 17	Drawn By: M. Pirello, D. Siag		
File: ADC_TOP.SchDoc					

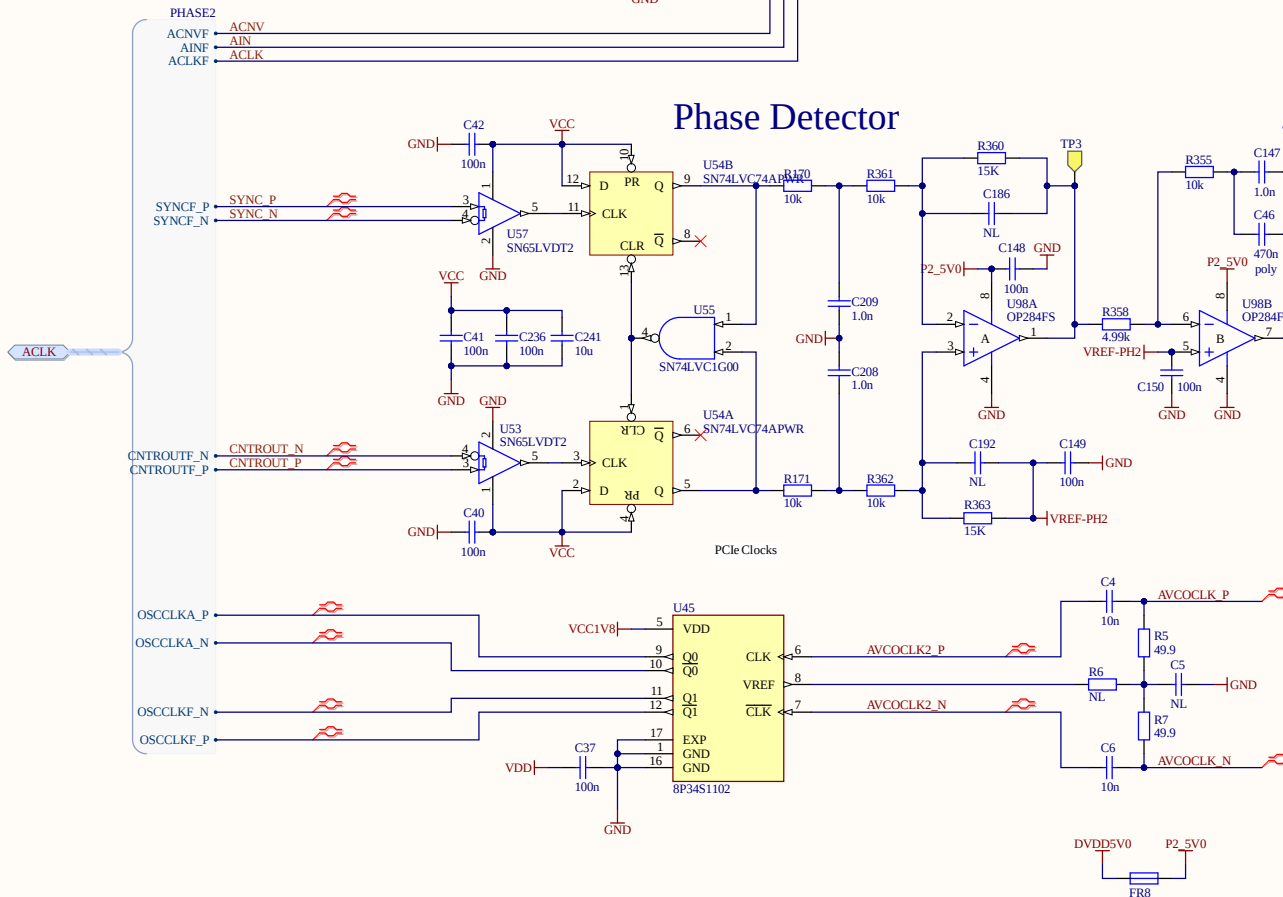




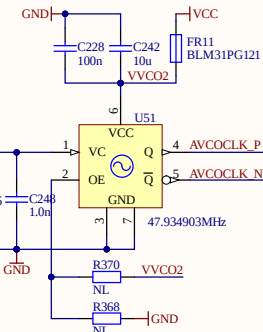
Control Voltage Monitor



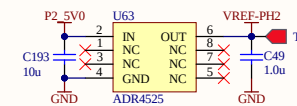
Phase Detector



Vectron VCO



2.5V Reference



Power Usage (350mW)
AD7685 2.5V*50uA = <1mW
2x OP284FS 20mA * 5V * 2 = 200mW
2x SN74LVC74APWR 10uA * 3.3V * 2 = <1mW
SN74LVC1G00 10uA * 3.3V * 2 = <1mW
2x SN65LVD12 8mA * 3.3V * 2 = 53mW
ADR4525 950uA * 5V = 4.75mW
OCXO = n/a
8P3451102 40mA * 1.8V = 90mW

Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 => P1_5V0
DVDD5V0 => P2_5V0

FPGA Power:
AVCC1V8 = XADC VCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCle
AVTT = 1.2V
AVCC = 1.0V

Project	LIGO ADC 32		LIGO Laboratory	
Sheet Title	VCO & Phase Detector		California Institute of Technology	
Size:	B	DCC D2300400	Rev: 2	Massachusetts Institute of Technology
Date:	6/18/2026	Time: 11:50:49 AM	Sheet: 3 of 17	National Science Foundation
File:	AD32_PHASE2.SchDoc		Drawn By:	M. Pirello, D. Siag



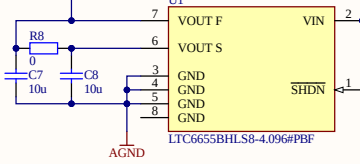
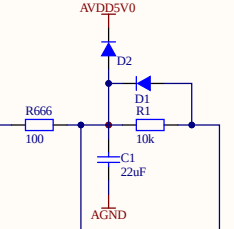
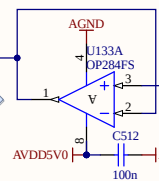
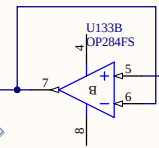
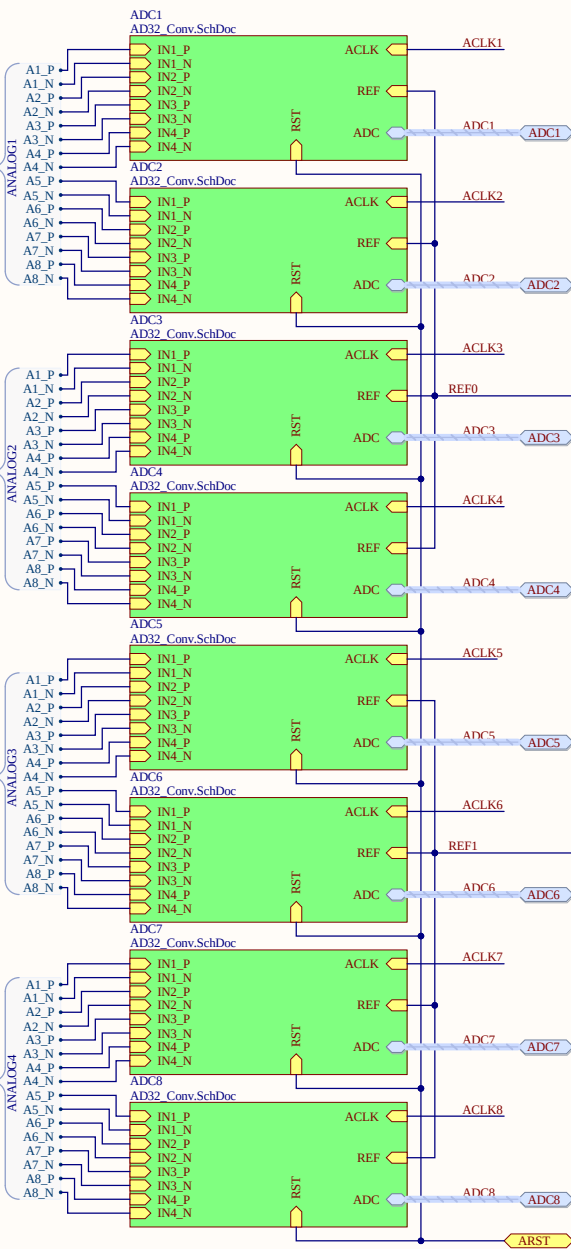


ANALOG1

ANALOG2

ANALOG3

ANALOG4



LTC6655LNL8 Package
Dropout Voltage 500mV
Separate VOUTS/NR from VOUTF? Maybe
place a zero ohm resistor for optional part
deployment.

Power Usage (504mW)
OP284FS 20mA * 5V = 100mW
LTC6655 7.5mA * 15V = 112mW
SI53365-B-GT 150mA * 1.8V = 270mW
SN65LVD12 8mA * 3.3V = 22mW

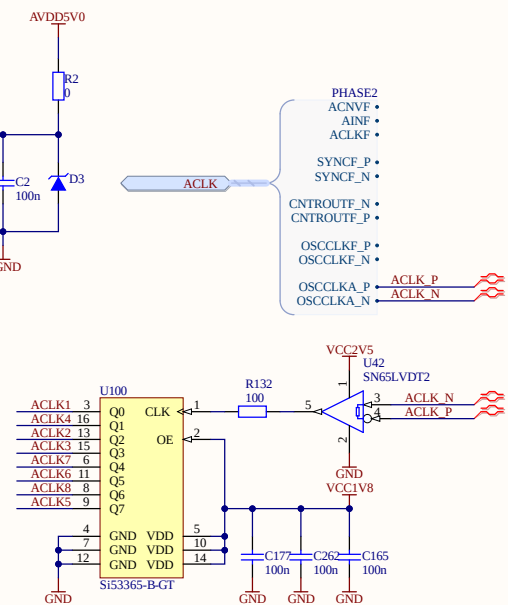
Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

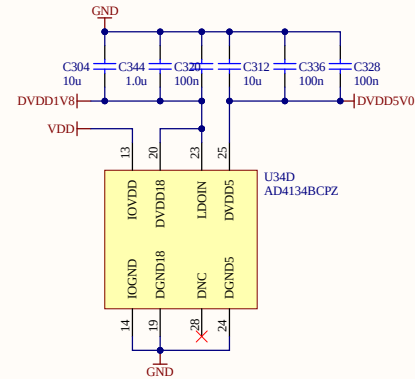
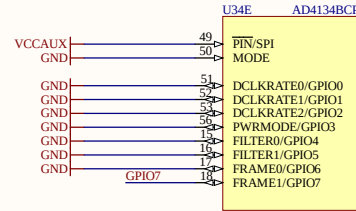
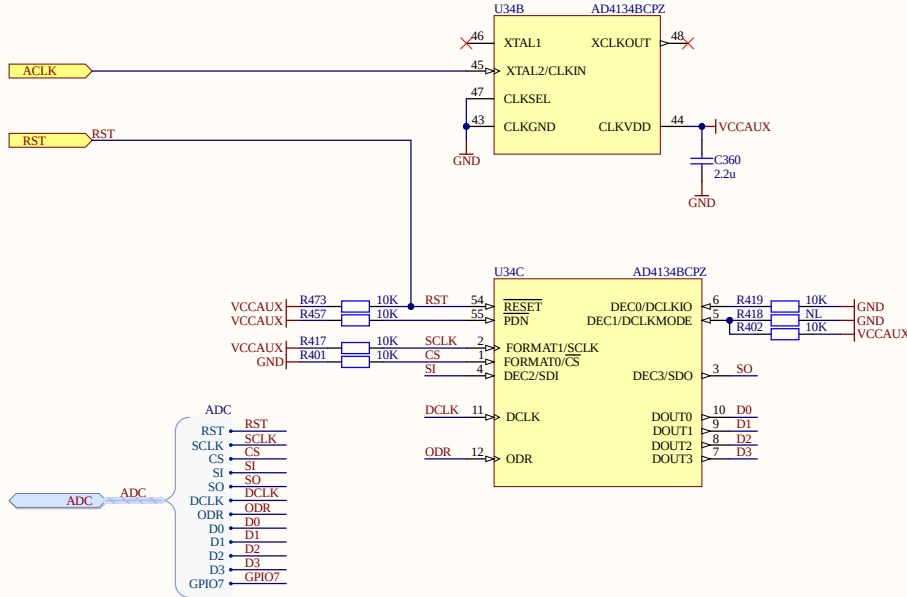
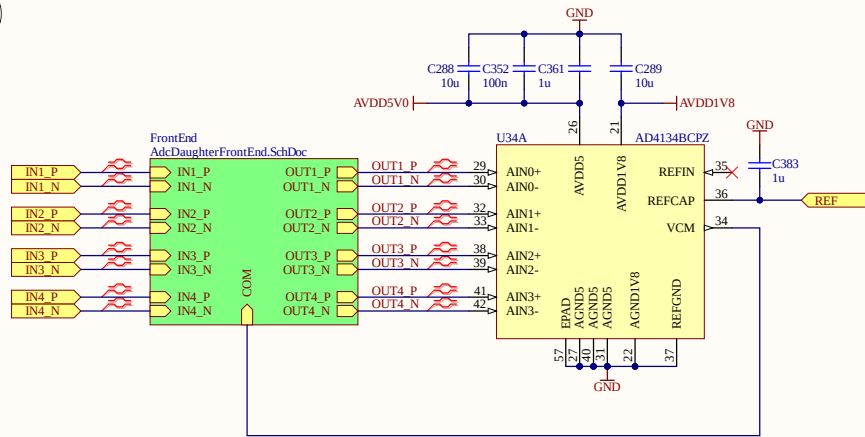
FPGA Power:
AVCC1V8 = XADC VCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCle
AVTT = 1.2V
AVCC = 1.0V



Project	LIGO ADC 32	LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	Converter Prototype Analog Inputs	
Size: B	DCC D2300400	Rev: 2
Date: 6/18/2026	Time: 11:50:50 AM	Sheet: 4 of 17
File: AD32_Inputs.SchDoc		Drawn By: M. Pirello, D. Siag





ADC INFORMATION
AD4134BCPZ is compatible with prior version AD7134BCPZ
Max Current Requirements, there are 8 chips
AVDD5 - 11mA * 8 = 88mA Max
DVDD5 - 44.8mA * 8 = 358mA
AVDD1V8 - 81mA * 8 = 648mA
DVDD1V8 - 105.5mA * 8 = 844mA
IOVDD - 3.17mA * 8 = 25.4mA
CLKVDD - 3.53mA * 8 = 28.3mA

Supplies
AVDD5 needs one
DVDD5 needs one
AVDD1V8 needs two
DVDD1V8 needs two

Power Usage (3.2266W)
AVDD5 = 88mA * 5V = 440mW
DVDD5 = 358mA * 5V = 1.8W
AVDD1V8 = 648mA * 1.8V = 1.17W
DVDD1V8 = 844mA * 1.8V = 1.52W
IOVDD = 25.4mA * 1.8V = 45.7mW
CLKVDD 28.3mA * 1.8V = 50.9mW

Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCIe
AVTT = 1.2V
AVCC = 1.0V

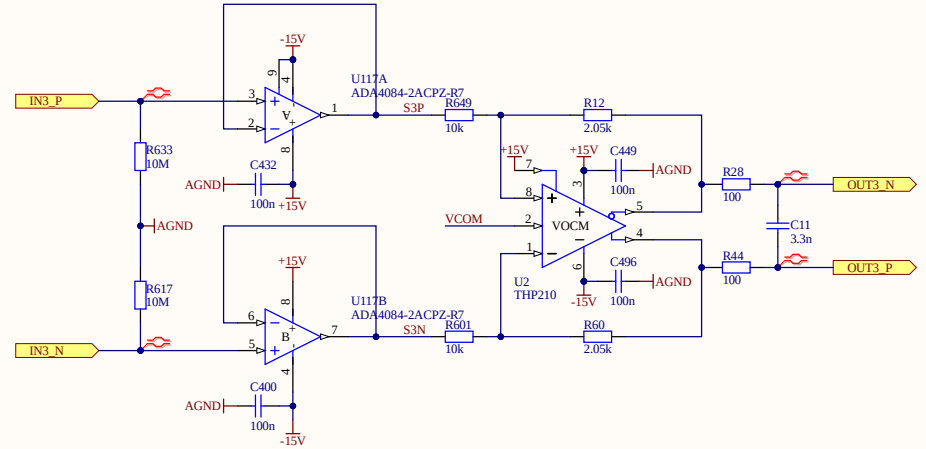
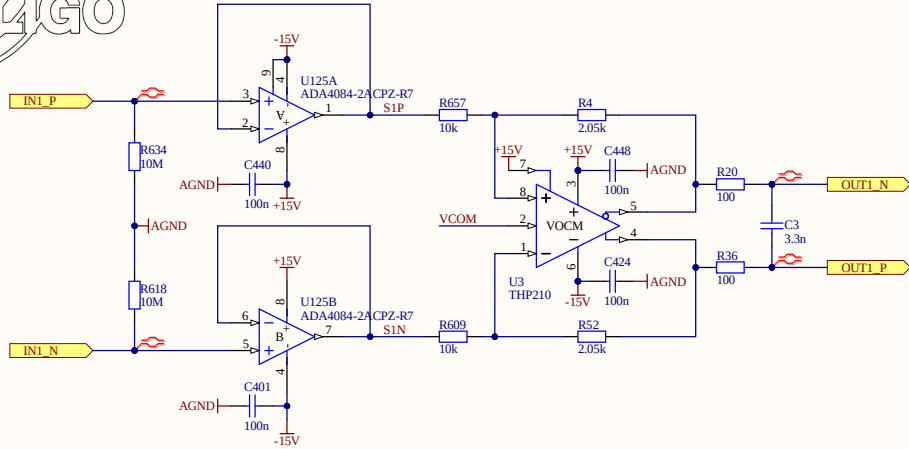
Power Dissipation
12.5V in 4.096V Reference, drop of 8.4V
5.25mA current per ADC or 42mA total
400mW total, 200mW per OPAMP

Max Output Current of OP284 is 10mA at
+/-15V supply.

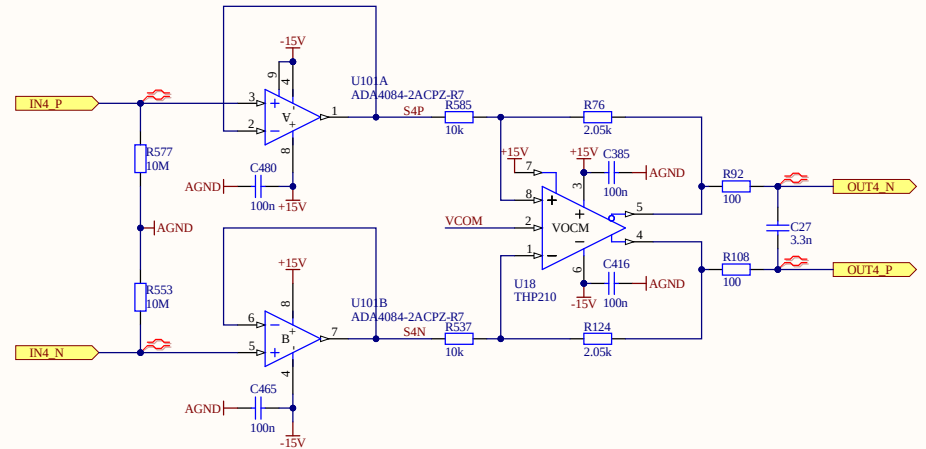
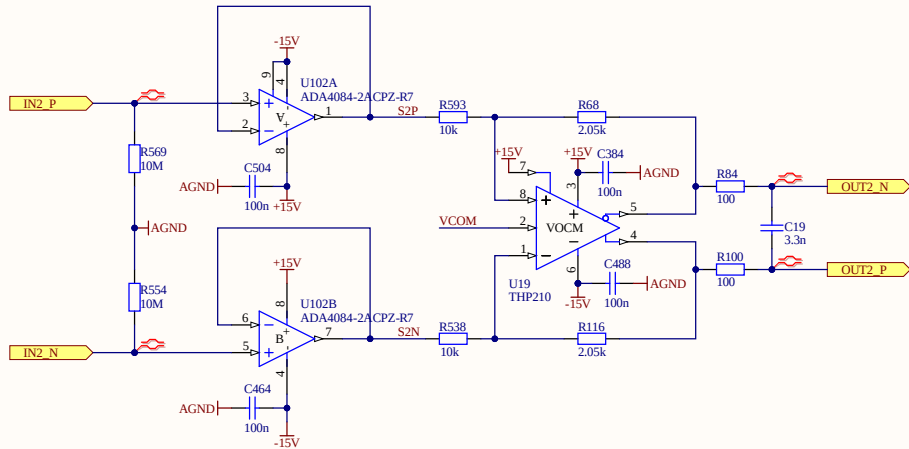
Required input current of each ADC is 5.25mA,
probably an issue here.

Project LIGO ADC 32		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
Sheet Title Converter Prototype ADC			
Size: B	DCC D2300400	Rev: 2	
Date: 6/18/2026	Time: 11:50:50 AM	Sheet: 5 of 17	Drawn By: M. Pirello, D. Siag
File: AD32_Conv.SchDoc			





Power Usage ()
OPA1612AID(32) 23V*3.6mA*2*32 = 5.15W
THP210 (32) 23V*950uA*32 = 670mW
ADA4084-2ACPZ-R7(32) 23V*2*32*0.565mA=831mW



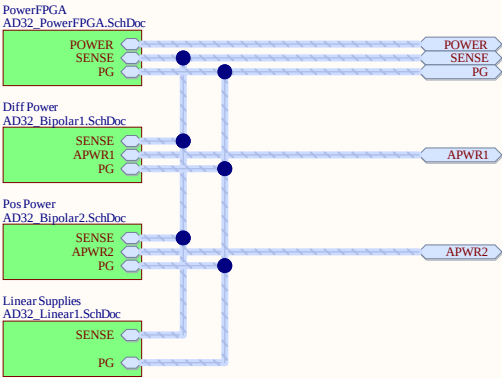
COM VCOM

Project LIGO ADC 32		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
Sheet Title Converter ADC Front End			
Size: B	DCC D2300400	Rev: 2	
Date: 6/18/2026	Time: 11:50:50 AM	Sheet: 6 of 17	Drawn By: M. Pirello, D. Siag
File: AdcDaughterFrontEnd.SchDoc			





Power Top Sheet



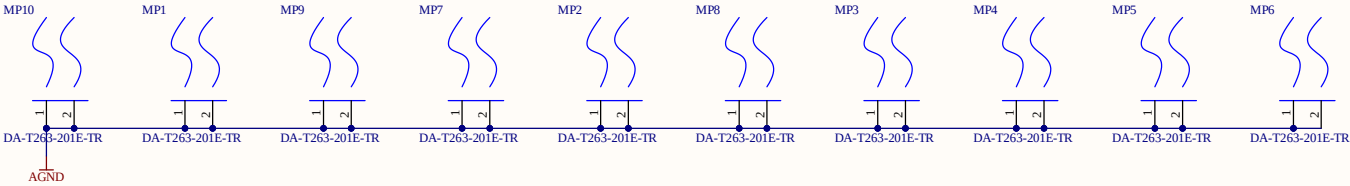
Voltage Legend:
SW+2V5=2.5V from switcher
SW+6V=6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 => P1_5V0
DVDD5V0 => P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCle
AVTT = 1.2V
AVCC = 1.0V



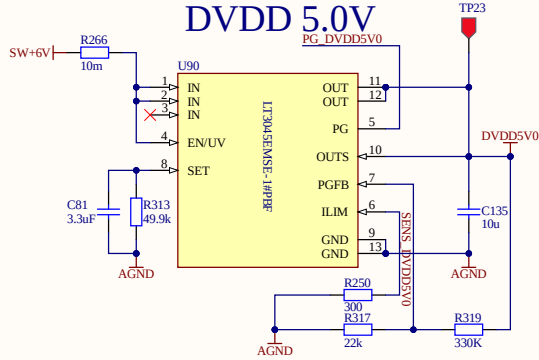
Project LIGO ADC 32			LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
Sheet Title Power Top				
Size: B	DCC D2300400	Rev: 2		
Date: 6/18/2026	Time: 11:50:50 AM	Sheet: 7 of 17	Drawn By: M. Pirello, D. Siag	
File: AD32_Power.SchDoc				



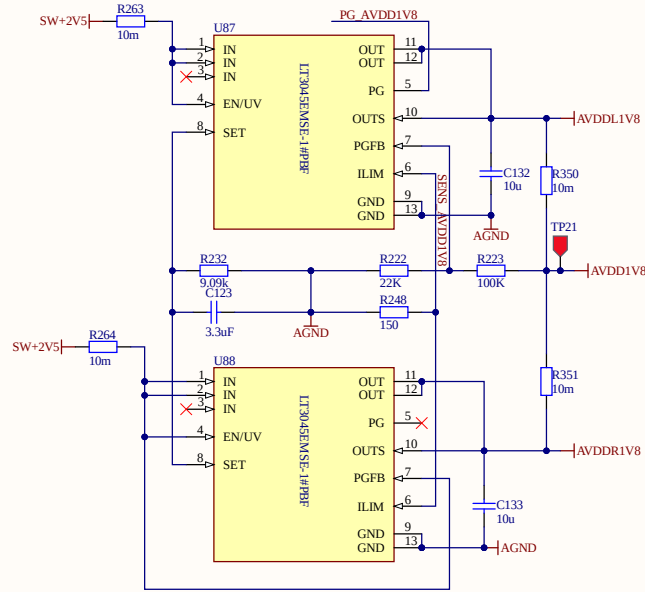


ADC Linear Power Supplies

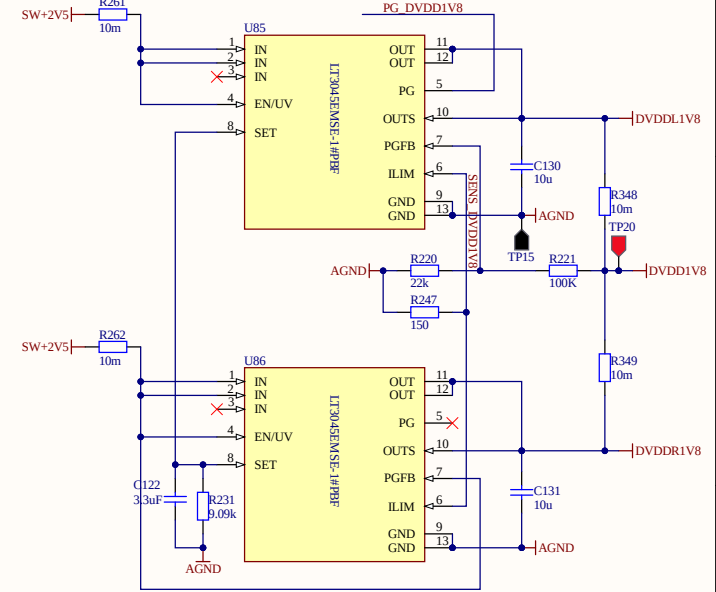
DVDD 5.0V



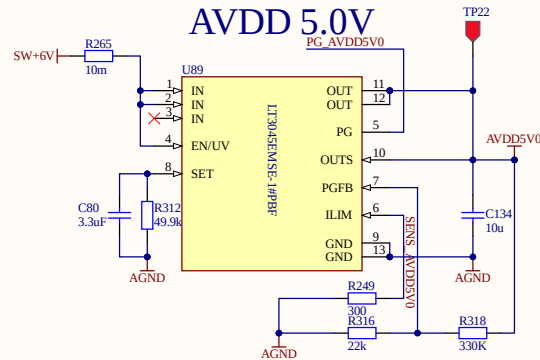
AVDD 1.8V



DVDD 1.8V



AVDD 5.0V



SENSE

SENS_33_P → SENS_33_P
SENS_33_N → SENS_33_N

SENS_25_P → SENS_25_P
SENS_25_N → SENS_25_N

SENS_18_P → SENS_18_P
SENS_18_N → SENS_18_N

SENS_10_P → SENS_10_P
SENS_10_N → SENS_10_N

SENS_120x_P → SENS_120x_P
SENS_120x_N → SENS_120x_N

SENS_120b_P → SENS_120b_P
SENS_120b_N → SENS_120b_N

Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power:
AVDDL1V8 = 1.8V ADC apwr
DVDDL1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADC VCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCle
AVTT = 1.2V
AVCC = 1.0V

SENS_AVCC → SENS_AVCC
SENS_AVTT → SENS_AVTT

• SENS_+15
• SENS_-15
• SENS_-15_N
• SENS_-15_P

POWER GOOD

PG_AVDDL1V8 → PG_AVDDL1V8
PG_AVDD5V0 → PG_AVDD5V0
PG_DVDDL1V8 → PG_DVDDL1V8
PG_DVDD5V0 → PG_DVDD5V0
PG_SW+2V5 → PG_SW+2V5
PG_SW+6V → PG_SW+6V
PWRGOOD → PG_FPGA
PG_SW+16V → PG_SW+16V
PG_SW-16V → PG_SW-16V
PG-15V → PG_L-15V
PG+15V → PG_L+15V

LT3045-1 Configs:
VCC5V0
Vset = Iset * Rset = 100uA * Rset
Rs = 50k
Vset = 50k * 100uA = 5.0V
PGFB:
Vset = 5.0V ; RPG1 = 22k
5.0V = 0.3V * (1 + RPG2/22k)
(5.0V/0.3V - 1) * 22k = RPG2
RPG2 < 345k

LT3045-1 Configs:
VDDL1V8:
Vset = Iset * Rset = 100uA * Rset
Rs = 9k * 2 (two supplies)
Vset = 9k * 2 * 100uA = 1.8V
PGFB:
Vset = 1.8V ; RPG1 = 22k
1.8V = 0.3V * (1 + RPG2/22k)
(1.8V/0.3V - 1) * 22k = RPG2
RPG2 < 110k

Project	LIGO ADC 32		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	Linear Supplies		
Size: B	DCC D2300400	Rev: 2	
Date: 6/18/2026	Time: 11:50:50 AM	Sheet: 8 of 17	Drawn By: M. Pirello, D. Siag
File: AD32_Linear1.SchDoc			





ADP505x Configs

FB1 - 1.8V 12.7k, 10k, 4.7uH

FB2 - 1.0V 10k, 40k, 3.3uH

FB3 - 2.5V 21.5k, 10k, 2.2uH

FB4 - 3.3V 31.6k, 10k, 2.2uH

FB5 - 1.8V 5k, 1.91k

Legend

VCC = 3.3V (digital voltage)

VDD = 1.8V (digital voltage)

VCCINT = 0.95V (fpga internal)

VCCAUX = 1.8V (fpga internal)

VCCADC = 1.8V (ADC ref voltage)

AVCC1V8

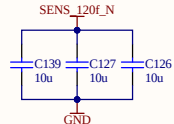
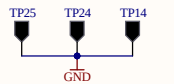
Power Up Config

1st - VCC1V0

2nd - VCC1V8

3rd - VCC3V3

4th & 5th VCC2V5 & AVCC1V8



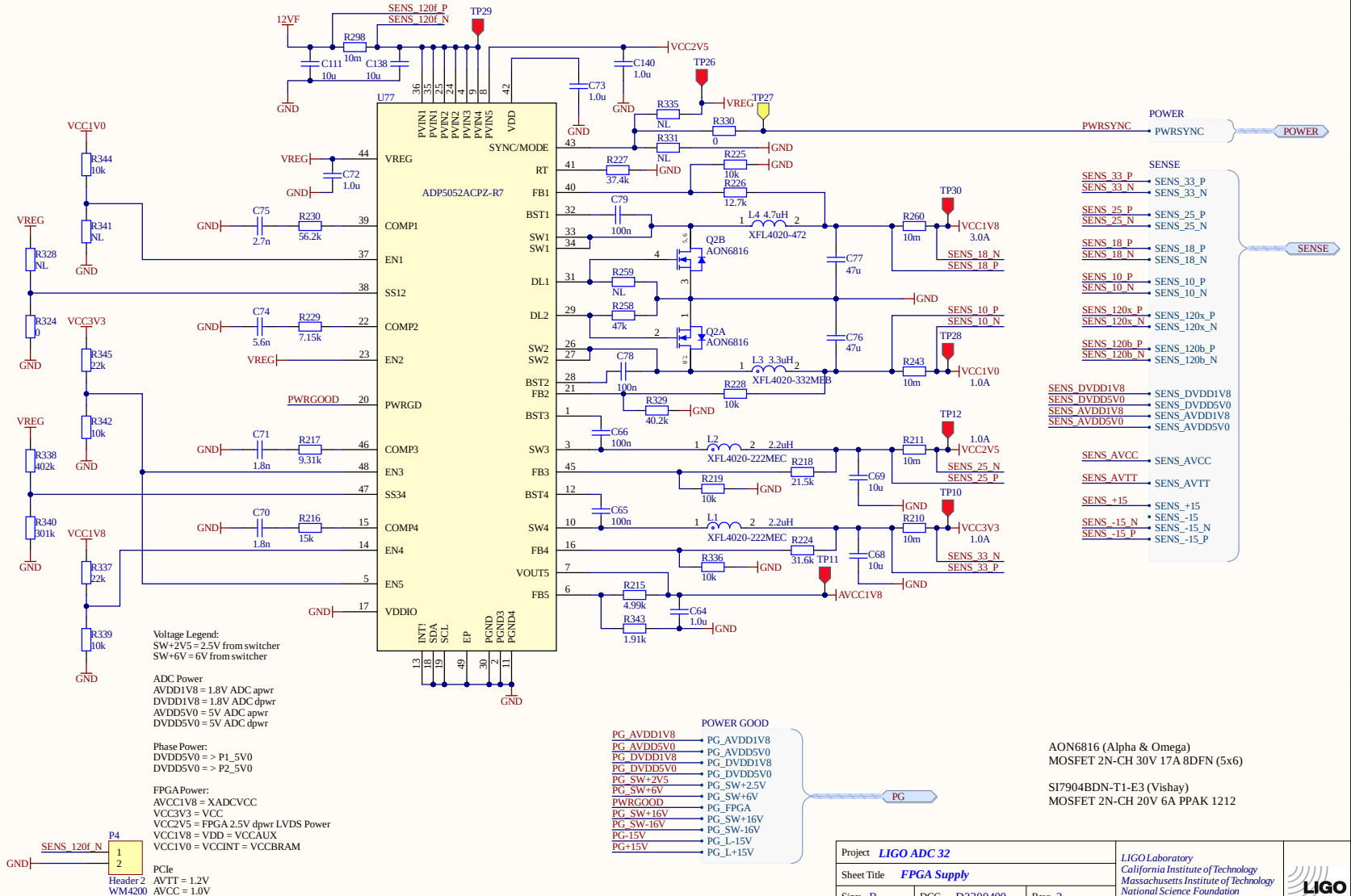
VCC Bridge



VDD Bridge



Switched FPGA Power



Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCIe
Header 2
WM4200
AVTT = 1.2V
AVCC = 1.0V

POWER GOOD
PG_AVDD1V8
PG_AVDD5V0
PG_DVDD1V8
PG_DVDD5V0
PG_SW+2V5
PG_SW+6V
PWRGOOD
PG_SW+16V
PG_SW+16V
PG_SW+16V
PG_L-15V
PG+15V

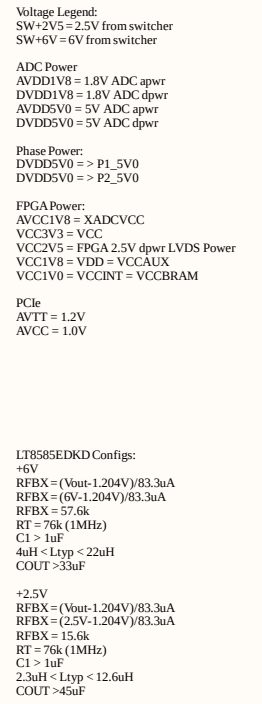
AON6816 (Alpha & Omega)
MOSFET 2N-CH 30V 17A 8DFN (5x6)

SI7904BDN-T1-E3 (Vishay)
MOSFET 2N-CH 20V 6A PPAK 1212

Project	LIGO ADC 32	LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
Sheet Title	FPGA Supply		
Size: B	DCC D2300400	Rev: 2	
Date: 6/18/2026	Time: 11:50:50 AM	Sheet: 9 of 17	
File: AD32_PowerFPGA.SchDoc		DrawnBy: M. Pirello, D. Siag	



Project <i>LIGO ADC 32</i>			
Sheet Title <i>Bipolar Analog Supply</i>			
Size: B	DCC D2300400	Rev: 2	
Date: 6/18/2026	Time: 11:50:50 AM	Sheet: 10 of 17	
File: AD32 Bipolar1SchDoc			



Project <i>LIGO ADC 32</i>			
Sheet Title <i>Dual Analog Supply</i>			
Size: B	DCC D2300400	Rev: 2	
Date: 6/18/2026	Time: 11:50:50 AM	Sheet: 11 of 17	
File: AD32_Bipolar2.SchDoc			LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation Drawn By: M. Pirello, D. Siag

A

B

C

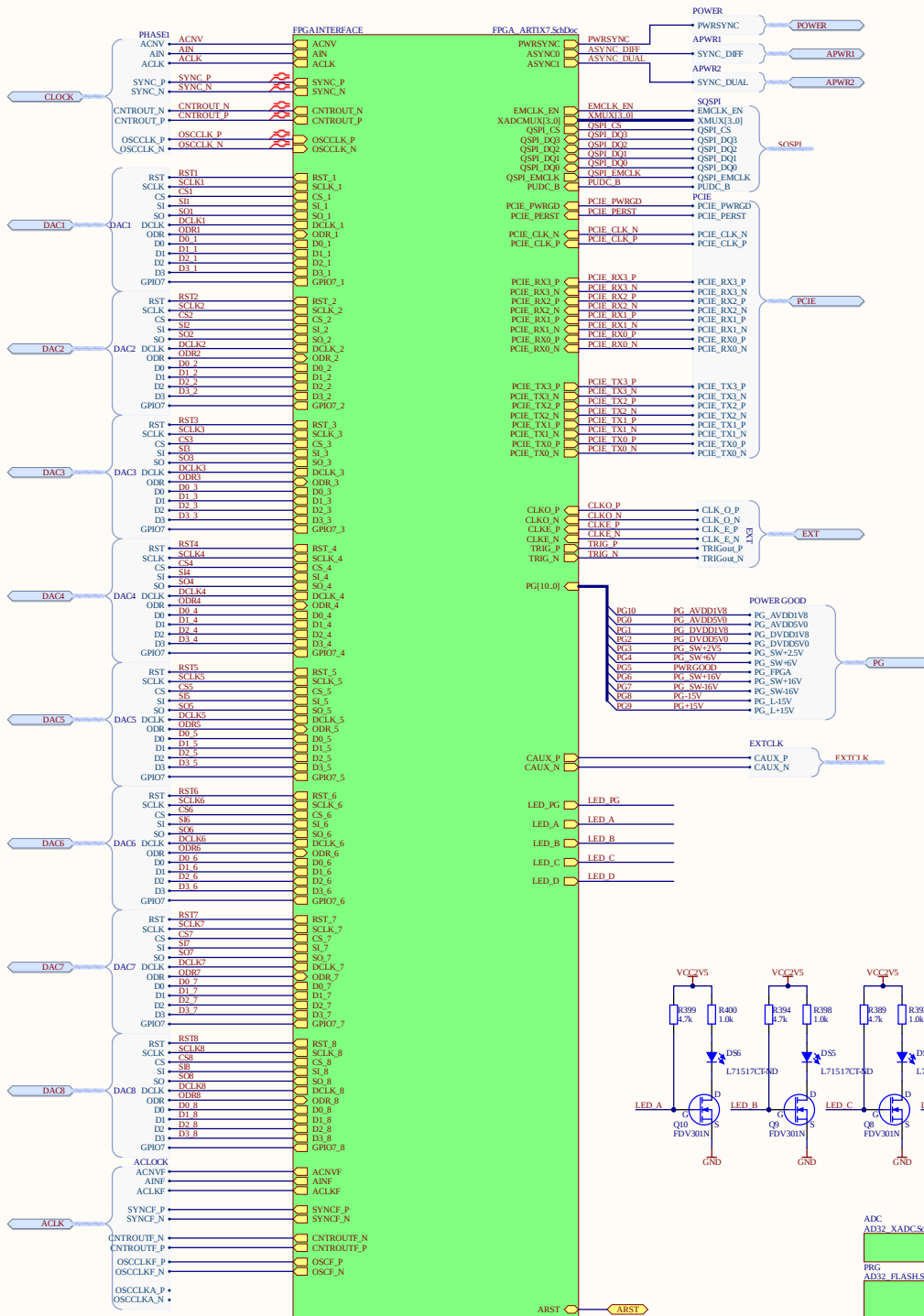
D

A

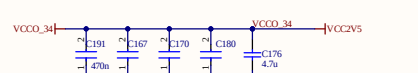
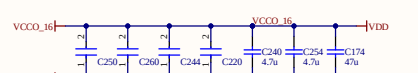
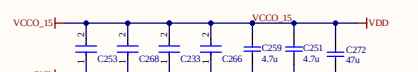
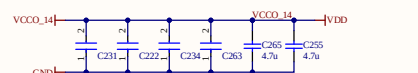
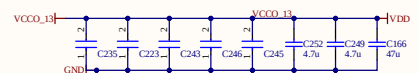
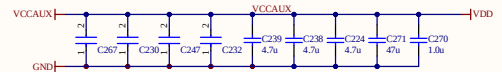
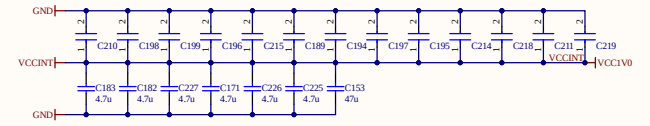
B

C

D



FPGA Decoupling Caps



Voltage Legend:
SW+2V5=2.5V from switcher
SW+6V=6V from switcher
VCCINT=1.0V
VCCAUX=1.8V
VCCBRAM=1.0V
VCCO=1.14V-3.465V (3.3V)
VIN=0.2V-3.465V
VCCAD=1.0V-1.8V
VCCAD=1.8V
VREF=1.25V
VREF=0V
VMGTAVCC=1.0V
VMGTAVTT=1.2V

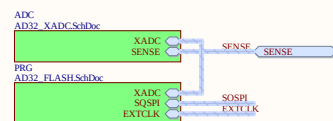
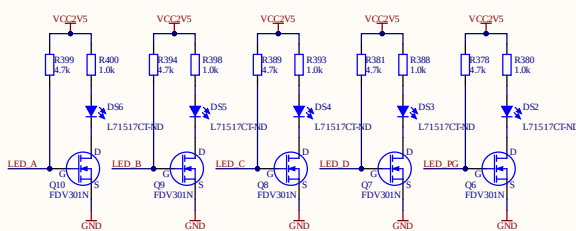
ADC Power:
AVDD1V8=1.8V ADC-apwr
DVDD1V8=1.8V ADC-dpwr
AVDD5V0=5V ADC-apwr
DVDD5V0=5V ADC-dpwr

Phase Power:
DVDD5V0=+PL_5V0
DVDD5V0=+PL_5V0
DVDD5V0=+PL_5V0

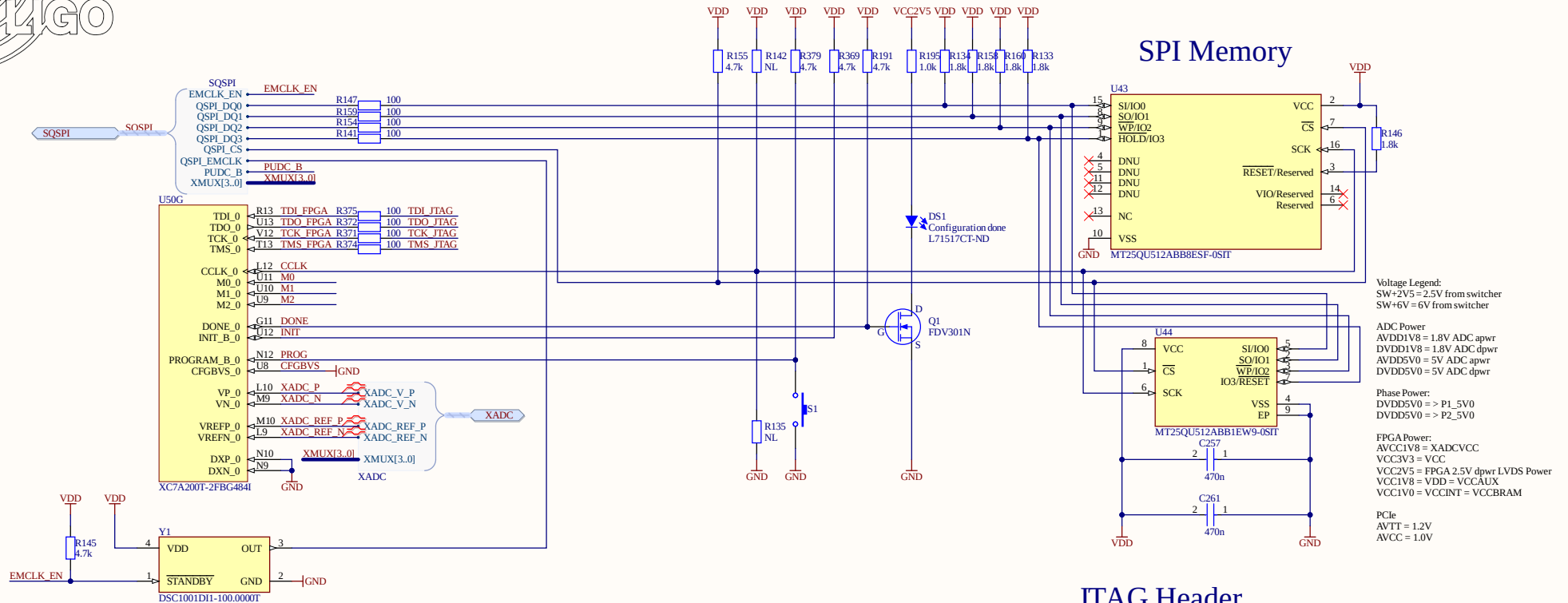
FPGA Power:
AVCC1V8=XADC/VCC
VCC3V3=VCC
VCC2V5=FGA 2.5V dper LVDS Power
VCC1V8=VDD=VCCAUX
VCC1V8=VCCINT=VCCBRAM

LVDSDC Specification
VCCO=2.5
VOH=1.675V
VOL=0.7V

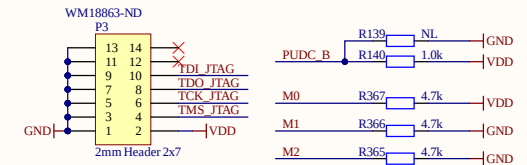
PCle
AVTT=1.2V
AVCC=1.0V



JTAG and SPI Flash



JTAG Header



Project <i>LIGO ADC 32</i>				<i>LIGO Laboratory</i> <i>California Institute of Technology</i> <i>Massachusetts Institute of Technology</i> <i>National Science Foundation</i>	
Sheet Title <i>JTAG & SPI Flash</i>					
Size: B	DCC	D2300400	Rev: 2		
Date: 6/18/2026	Time: 11:50:51 AM	Sheet: 13 of 17	Drawn By: <i>M. Pirello, D. Siag</i>		
File: AD32_FLASH.SchDoc					



INA210 configuration
VCC = VCC2 = 3.3V
Vout = (I x 10mohm) * 200
I = Vout / (200 * 10mohm)

12.5mOhm sense R
2A range
Gain 200 V/V

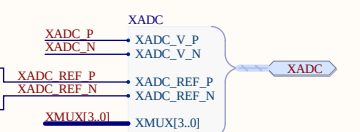
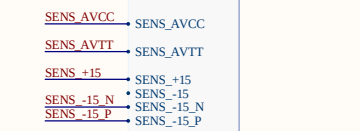
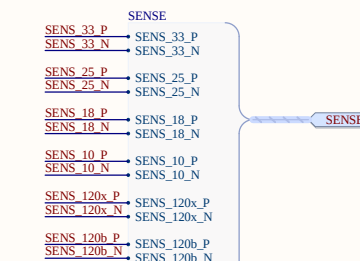
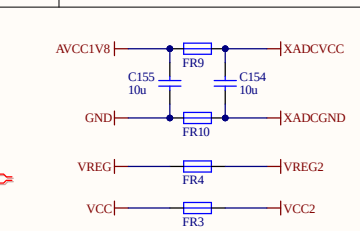
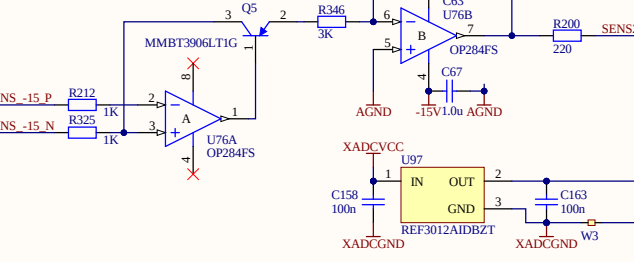
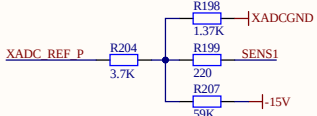
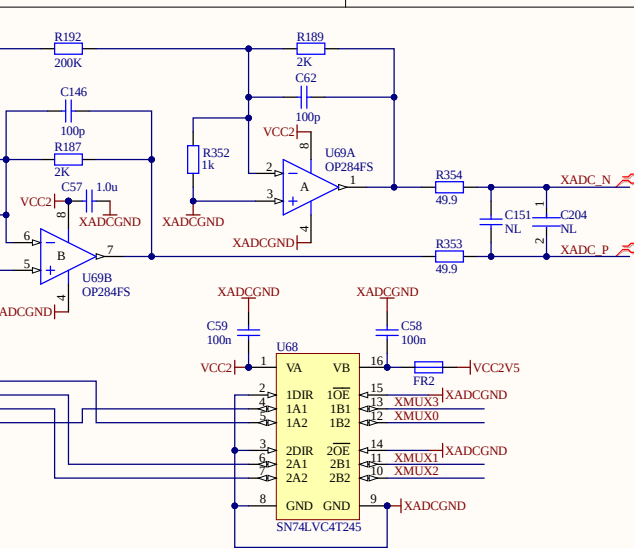
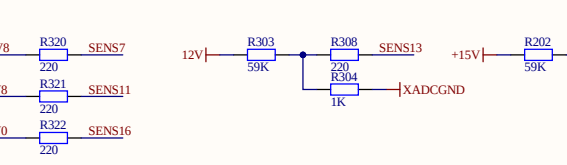
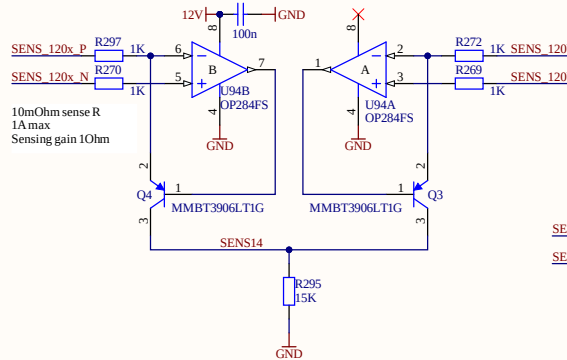
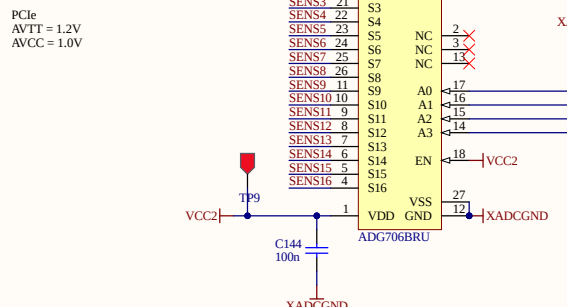
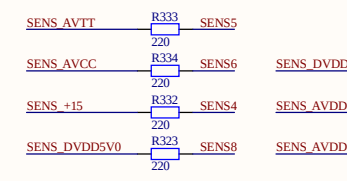
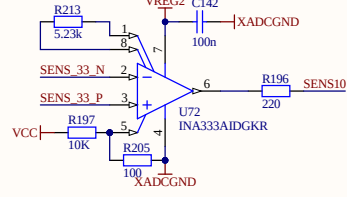
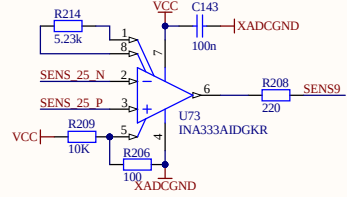
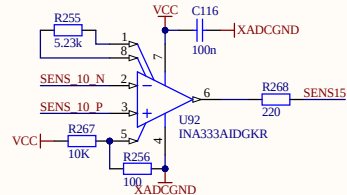
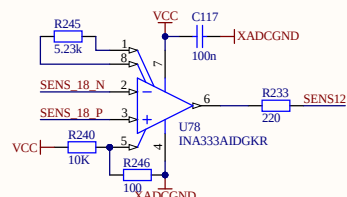
Voltage Legend:
SW+2V5=2.5V from switcher
SW+6V=6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 => P1_5V0
DVDD5V0 => P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCIe
AVTT = 1.2V
AVCC = 1.0V



Project	LIGO ADC 32	LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	XADC	
Size:	B	DCC D2300400 Rev: 2
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File:	AD32_XADC.SchDoc	Sheet: 14 of 17 Drawn By: M. Pirello, D. Siag







PCIe 4x Slot

