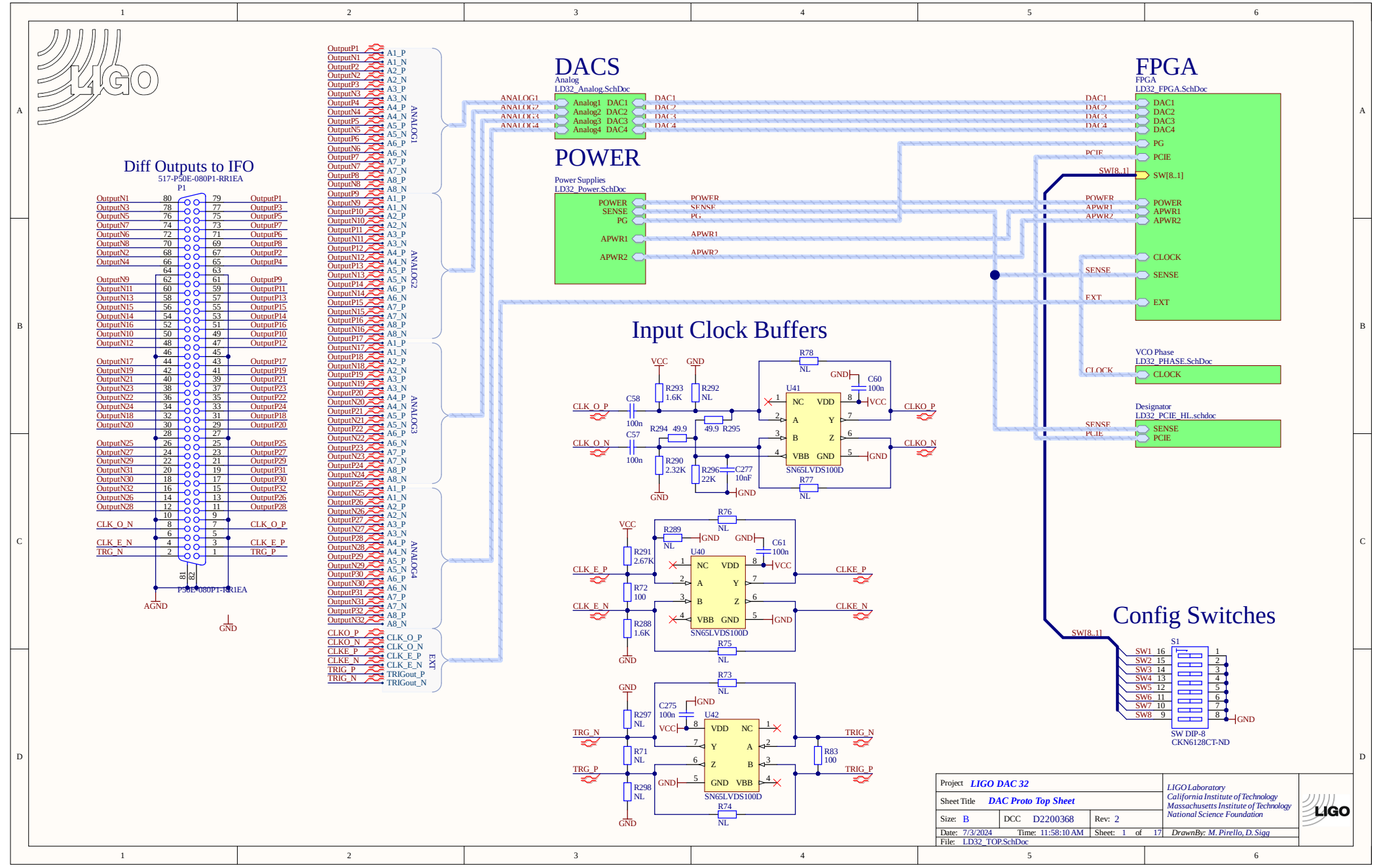
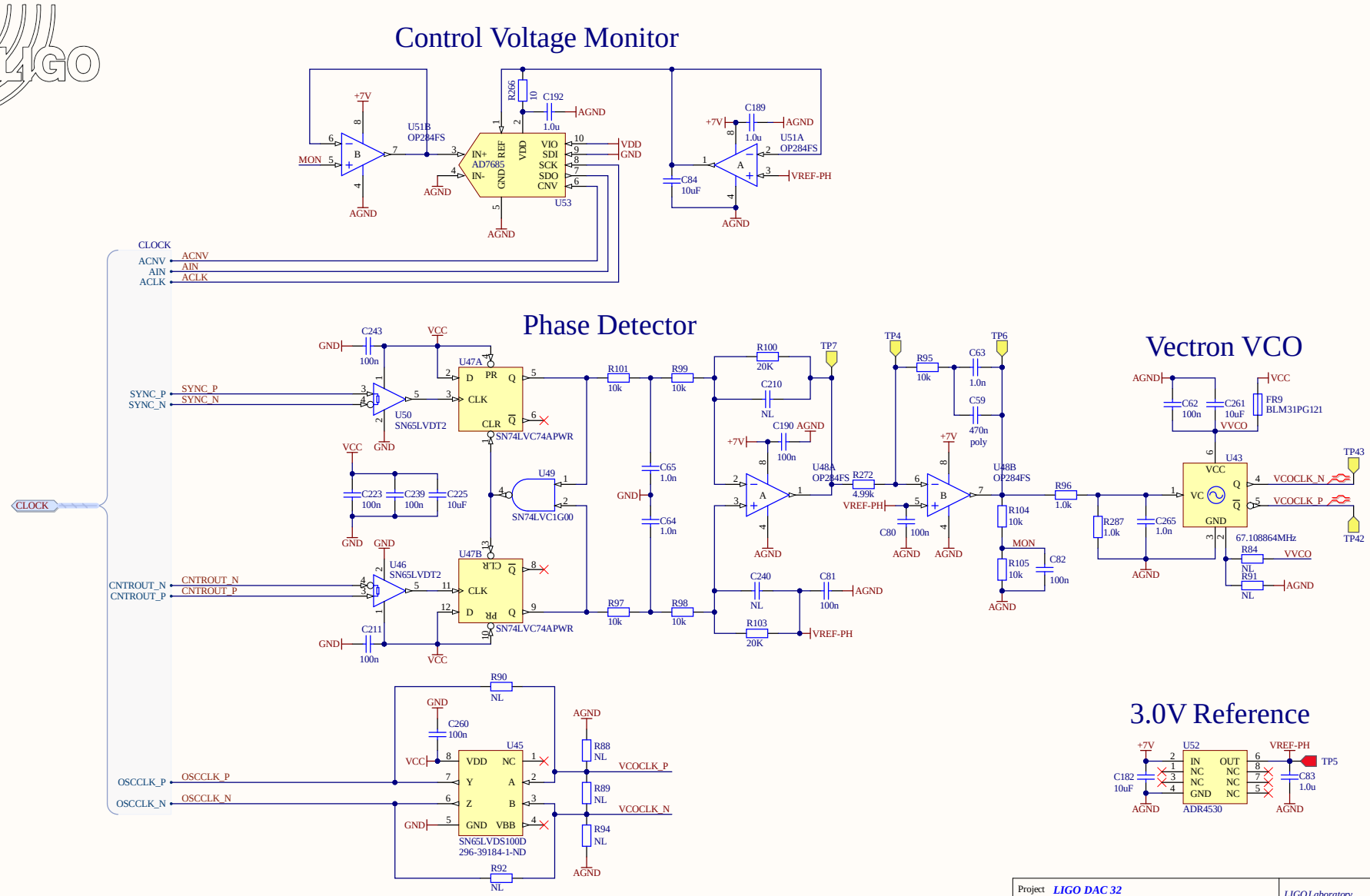

DACS
Analog
LD32_Analog.SchDoc
POWER
Power Supplies
LD32_Power.SchDoc
FPGA
FPGA
LD32_FPGA.SchDoc
Input Clock Buffers
Diff Outputs to IFO
517-P50E-080P1-RR1EA
P1
P50E-080P1-RR1EA
AGND
GND
SN65LVDS100D
U41
U40
U42
VCO Phase
LD32_PHASE.SchDoc
Designator
LD32_PCIE_HL.schdoc
Config Switches
SW DIP-8
CKN6128CT-ND
Project LIGO DAC 32
Sheet Title DAC Proto Top Sheet
Size: B
DCC D2200368
Rev: 2
Date: 7/3/2024
Time: 11:58:10 AM
Sheet: 1 of 17
File: LD32_TOP.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg


Control Voltage Monitor
U51B
OP284FS
U53
AD7685
U51A
OP284FS
Phase Detector
U47A
U47B
U50
SN65LVDT2
U46
SN65LVDT2
SN74LVC74APWR
SN74LVC74APWR
SN74LVC1G00
U48A
OP284FS
U48B
OP284FS
Vectron VCO
U43
67.108864MHz
Optional LVPECL-LVDS Translator
U45
SN65LVDS100D
296-39184-1-ND
3.0V Reference
U52
ADR4530
CLOCK
ACNV
AIN
ACLK
SYNC_P
SYNC_N
CNTROUT_N
CNTROUT_P
OSCCLK_P
OSCCLK_N
VCOCLK_P
VCOCLK_N
VREF-PH
AGND
GND
VCC
+7V
MON
VVCO
Project LIGO DAC 32
Sheet Title VCO & Phase Detector
Size: B
DCC D2200368
Rev: 2
Date: 7/3/2024
Time: 11:58:10 AM
Sheet: 2 of 17
File: LD32_PHASE.SchDoc
LIGO Laboratory
California Institute of Technology
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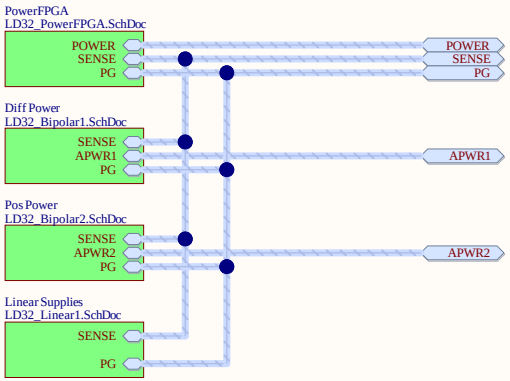
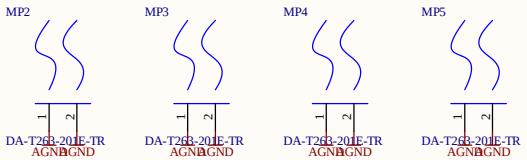
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

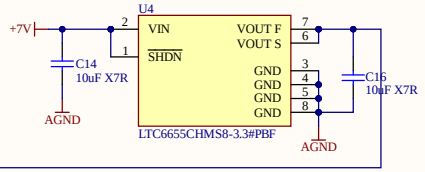
Power Top Sheet

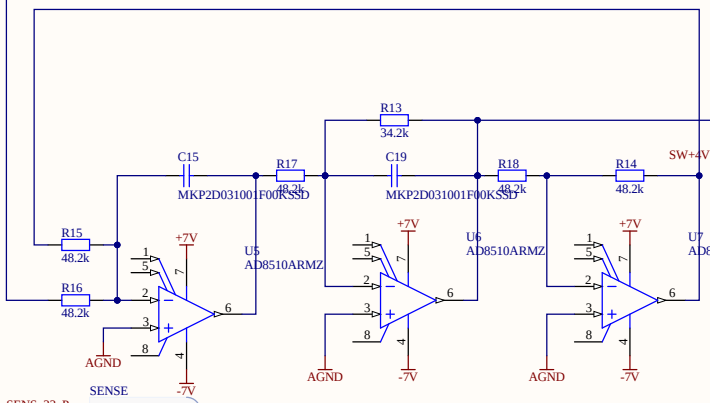




Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Power Top*			
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024 Time: 11:58:11 AM		Sheet: 3 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Power.SchDoc			

DAC Linear Power Supplies





SENSE

SENS_33_P → SENS_33_P
SENS_33_N → SENS_33_N
SENS_25_P → SENS_25_P
SENS_25_N → SENS_25_N
SENS_18_P → SENS_18_P
SENS_18_N → SENS_18_N
SENS_10_P → SENS_10_P
SENS_10_N → SENS_10_N
SENS_120x_P → SENS_120x_P
SENS_120x_N → SENS_120x_N
SENS_120b_P → SENS_120b_P
SENS_120b_N → SENS_120b_N
SENS_VCCA3.3V → SENS_VCCA3.3V
SENS_AVCC3.3V → SENS_AVCC3.3V
SENS_DVDD1.2V → SENS_DVDD1.2V
SENS_AVCC → SENS_AVCC
SENS_AVTT → SENS_AVTT
SENS_+7 → SENS_+7
SENS_-7_N → SENS_-7_N
SENS_-7_P → SENS_-7_P

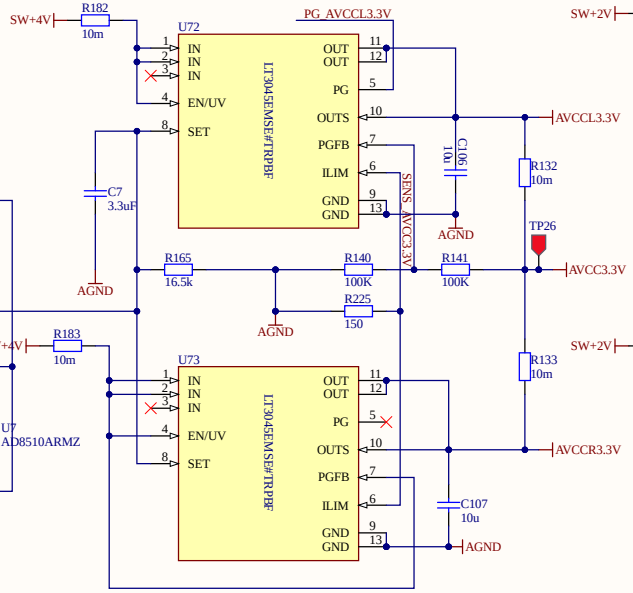
→ SENSE

LT3045-1 Configs:
VCCA3V3
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k *100uA = 3.3V
PGFB:
Vset = 3.3V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

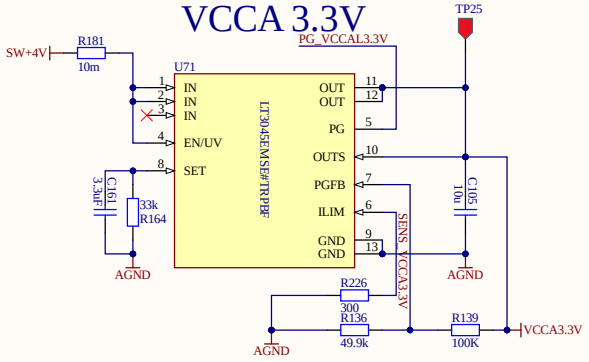
AVCC3V3:
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k *100uA = 3.3V
PGFB:
Vset = 3.3V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

LT3045-1 Configs:
DVDD1V2:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k

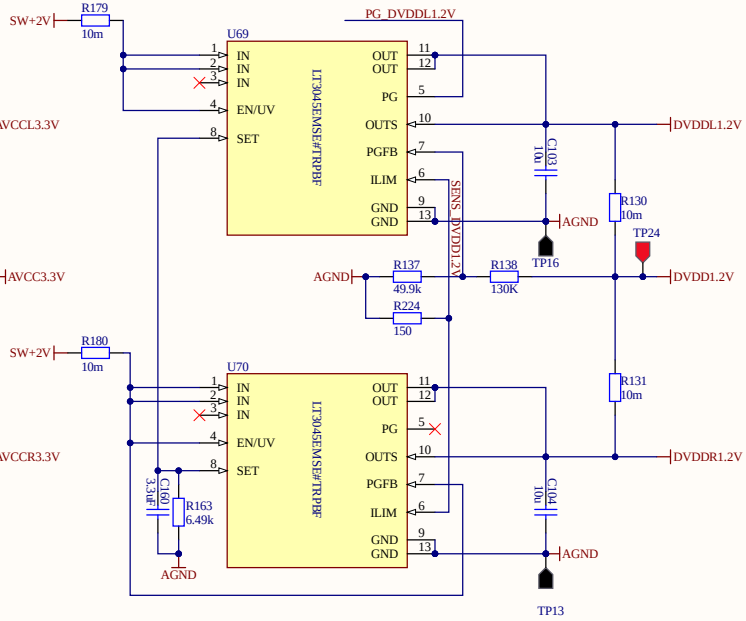
AVCC 3.3V



VCCA 3.3V



DVDD 1.2V Core



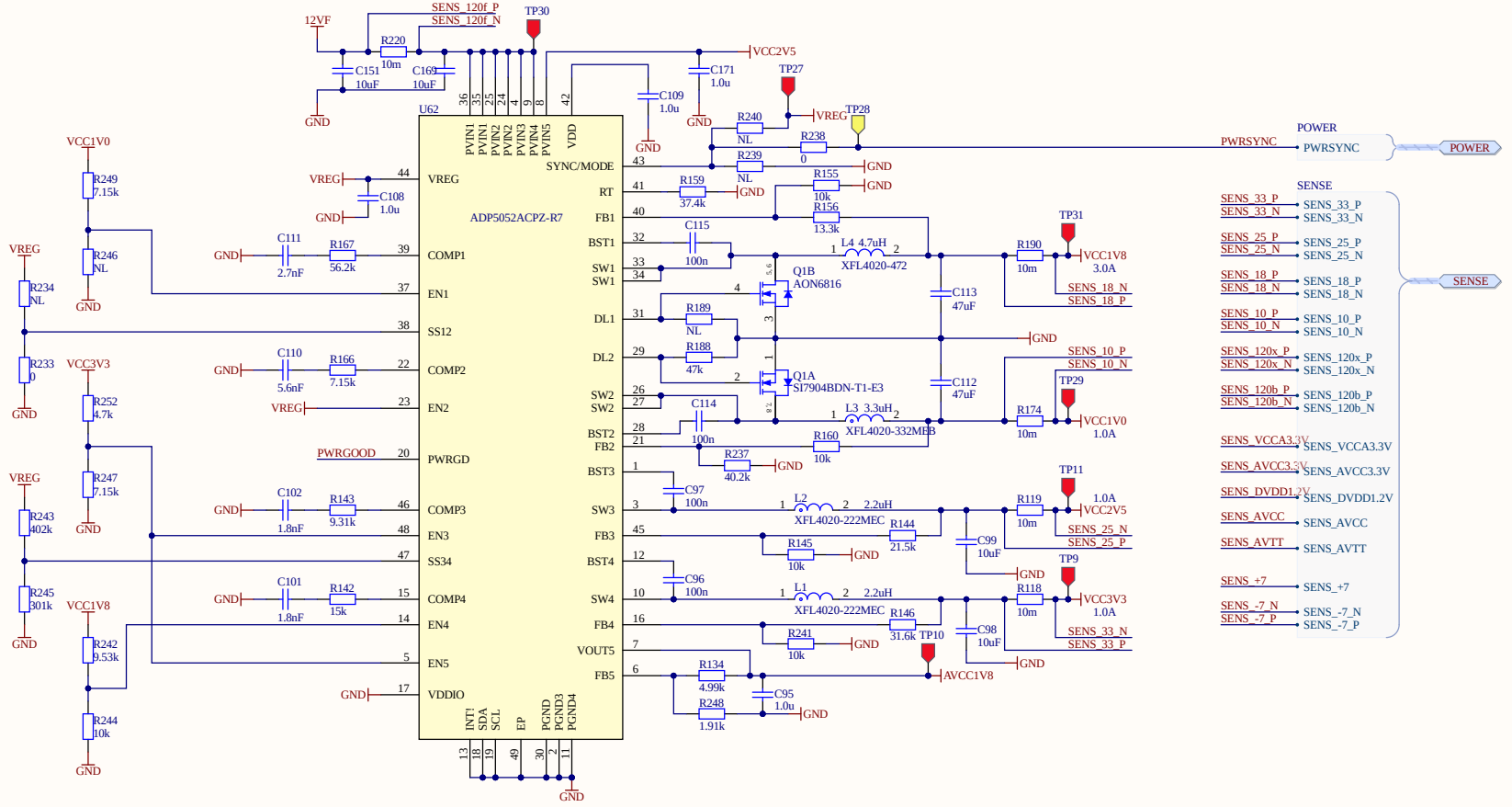
POWER GOOD

PG_VCCAL3.3V → PG_VCCAL3.3V
PG_AVCCL3.3V → PG_AVCCL3.3V
PG_DVDDL1.2V → PG_DVDDL1.2V
PG_SW+2V → PG_SW+2V
PG_SW+4V → PG_SW+4V
PWRGOOD → PG_FPGA
PG_SW+8V → PG_SW+8
PG_SW-8V → PG_SW-8
PG-7 → PG_L-7v
PG+7 → PG_L+7v

→ PG

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Linear Supplies*		
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024	Time: 11:58:11 AM	Sheet: 4 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Linear1.SchDoc			

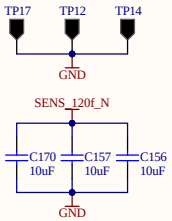
Switched FPGA Power



ADP505x Configs
FB1 - 1.8V 12.7k, 10k, 4.7uH
FB2 - 1.0V 10k. 40k, 3.3uH
FB3 - 2.5V 21.5k, 10k, 2.2uH
FB4 - 3.3V 31.6k, 10k, 2.2uH
FB5 - 1.8V 5k, 1.91k

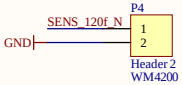
Legend
VCC = 3.3V (digital votlage)
VDD = 1.8V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Power Up Config
1st - VCC1V0
2nd - VCC1V8
3rd - VCC3V3
4th & 5th VCC2V5 & AVCC1V8

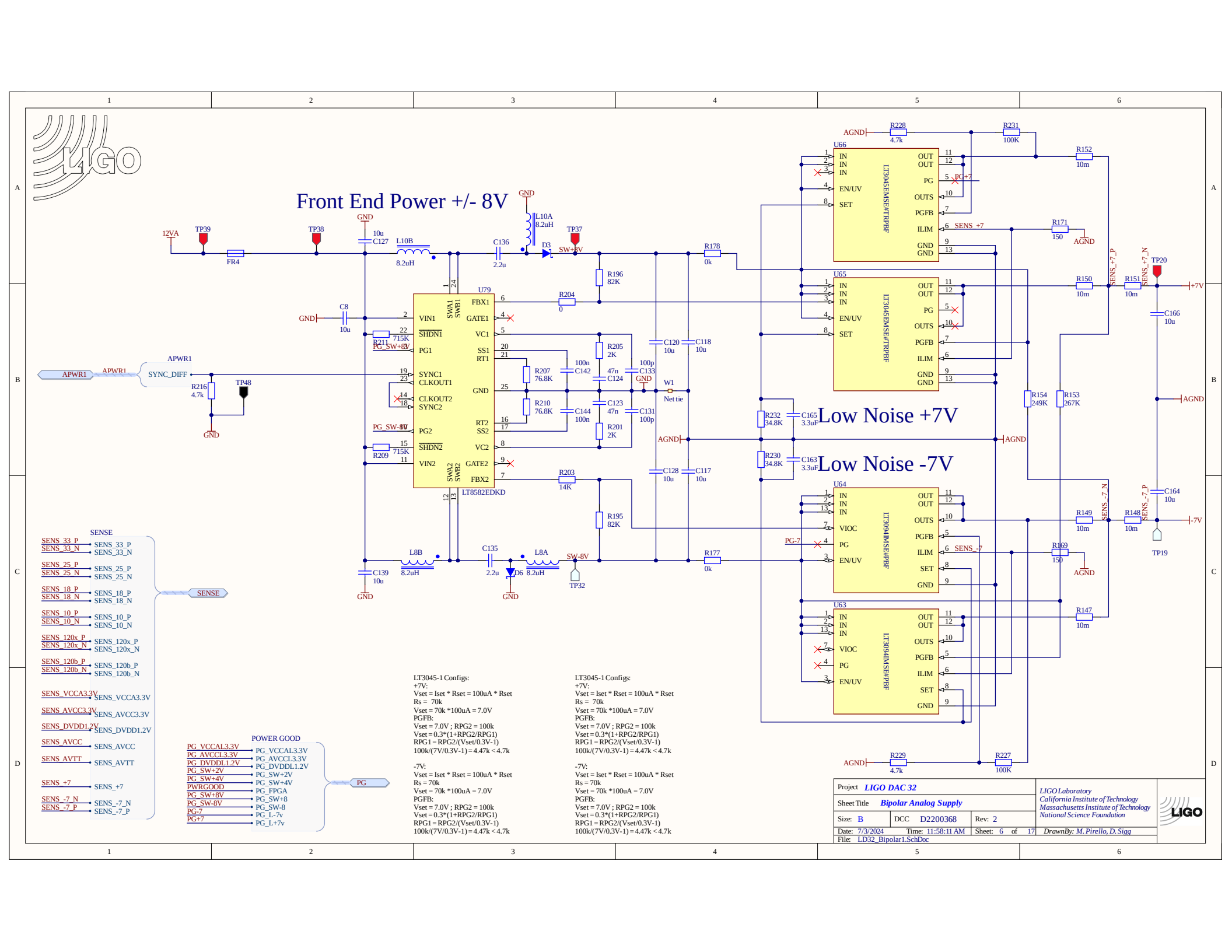


VCC Bridge

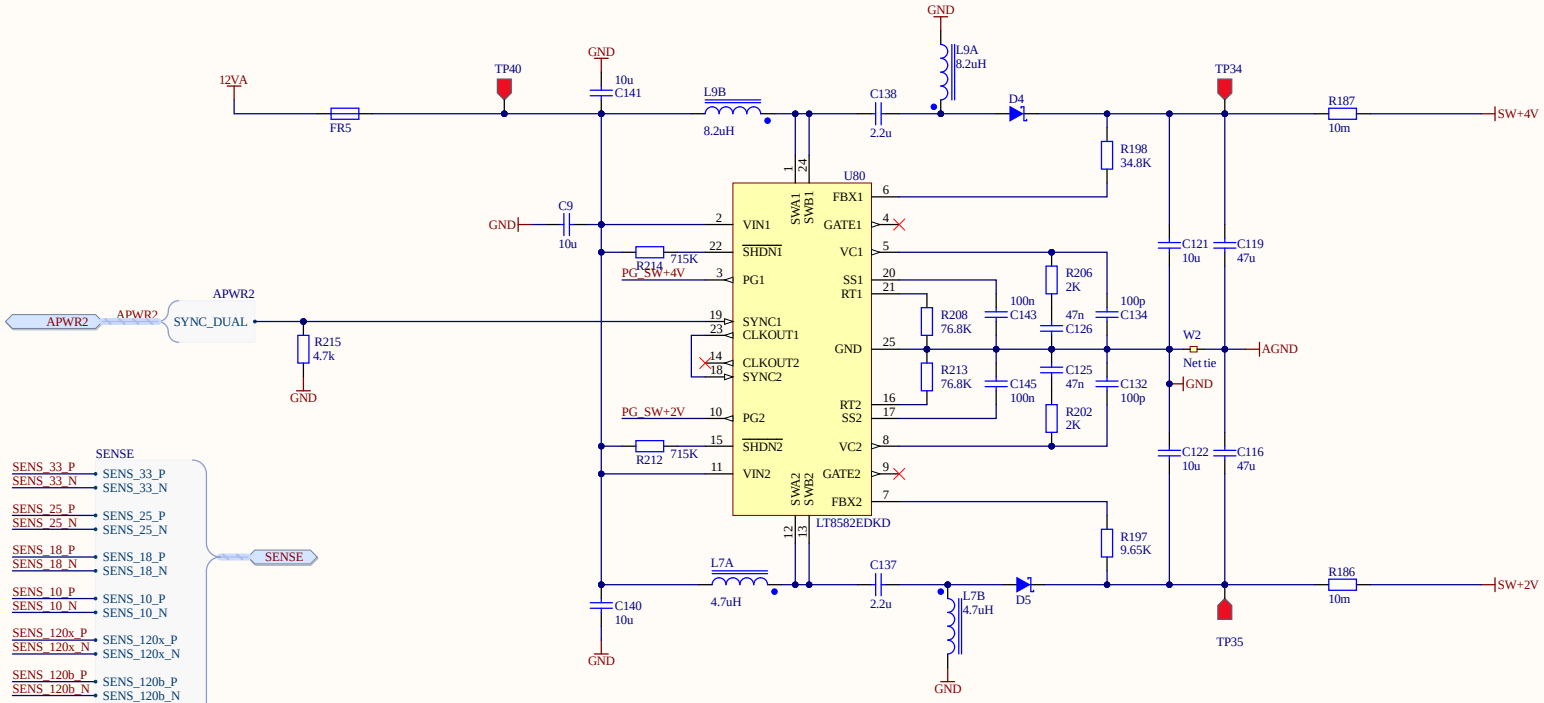
VDD Bridge



Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*FPGA Supply*		
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024	Time: 11:58:11 AM	Sheet: 5 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_PowerFPGA.SchDoc			


Front End Power +/- 8V
Low Noise +7V
Low Noise -7V
LT3045-1 Configs:
+7V:
Vset = Iset * Rset = 100uA * Rset
Rs = 70k
Vset = 70k *100uA = 7.0V
PGFB:
Vset = 7.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(7V/0.3V-1) = 4.47k < 4.7k
-7V:
Vset = Iset * Rset = 100uA * Rset
Rs = 70k
Vset = 70k *100uA = 7.0V
PGFB:
Vset = 7.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(7V/0.3V-1) = 4.47k < 4.7k
SENSE
POWER GOOD
Project LIGO DAC 32
Sheet Title Bipolar Analog Supply
Size: B
DCC D2200368
Rev: 2
Date: 7/3/2024
Time: 11:58:11 AM
Sheet: 6 of 17
File: LD32_Bipolar1.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

DAC Switcher



SENSE

SENS_33_P — SENS_33_P
SENS_33_N — SENS_33_N
SENS_25_P — SENS_25_P
SENS_25_N — SENS_25_N
SENS_18_P — SENS_18_P
SENS_18_N — SENS_18_N
SENS_10_P — SENS_10_P
SENS_10_N — SENS_10_N
SENS_120x_P — SENS_120x_P
SENS_120x_N — SENS_120x_N
SENS_120b_P — SENS_120b_P
SENS_120b_N — SENS_120b_N
SENS_VCCA3.3V — SENS_VCCA3.3V
SENS_AVCC3.3V — SENS_AVCC3.3V
SENS_DVDD1.2V — SENS_DVDD1.2V
SENS_AVCC — SENS_AVCC
SENS_AVTT — SENS_AVTT
SENS_+7 — SENS_+7
SENS_-7_N — SENS_-7_N
SENS_-7_P — SENS_-7_P

→ SENSE

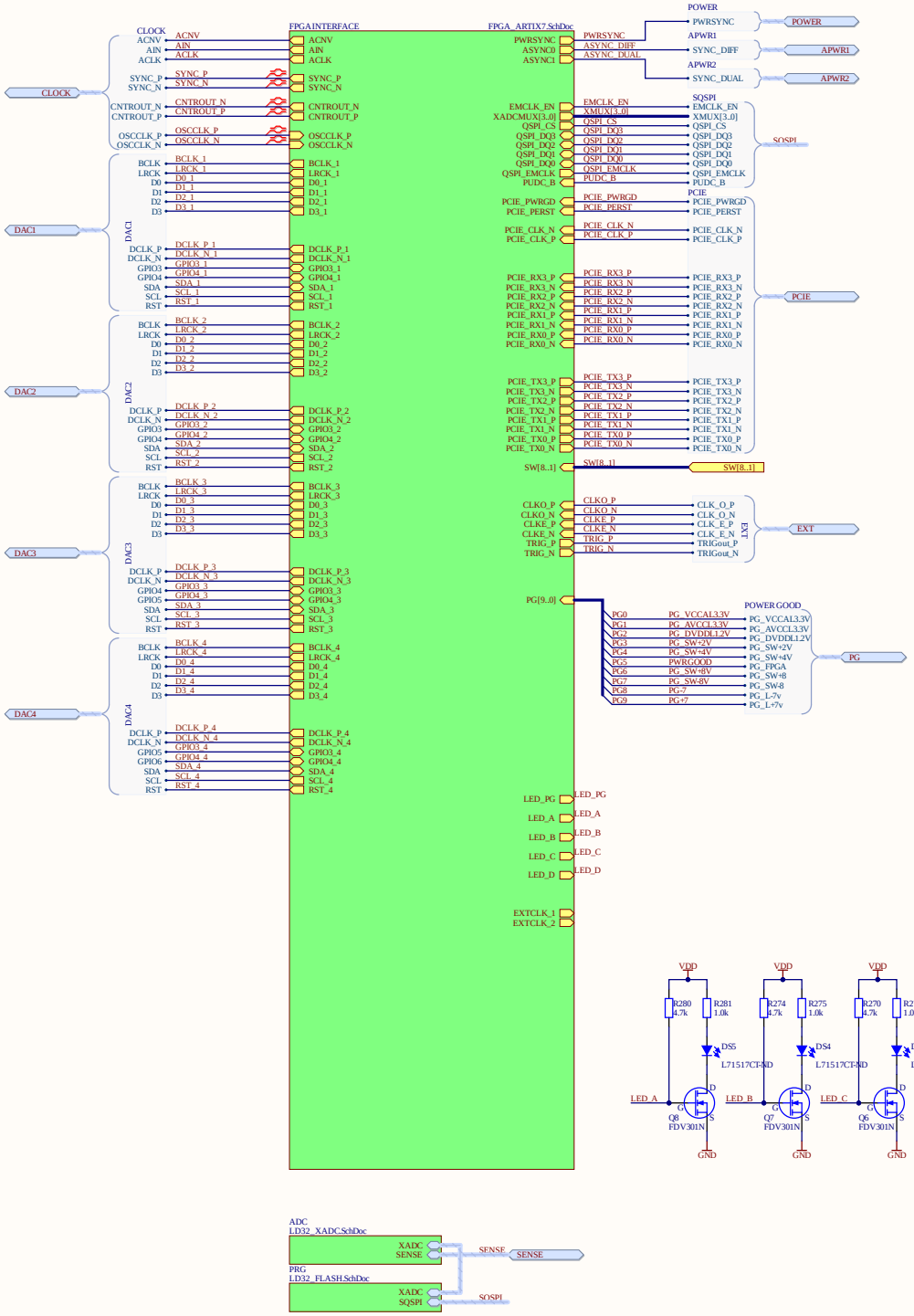
POWER GOOD

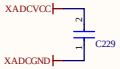
PG_VCCAL3.3V — PG_VCCAL3.3V
PG_AVCCL3.3V — PG_AVCCL3.3V
PG_DVDDL1.2V — PG_DVDDL1.2V
PG_SW+2V — PG_SW+2V
PG_SW+4V — PG_SW+4V
PWRGOOD — PG_FPGA
PG_SW+8V — PG_SW+8
PG_SW-8V — PG_SW-8
PG-7 — PG_L-7v
PG+7 — PG_L+7v

→ PG

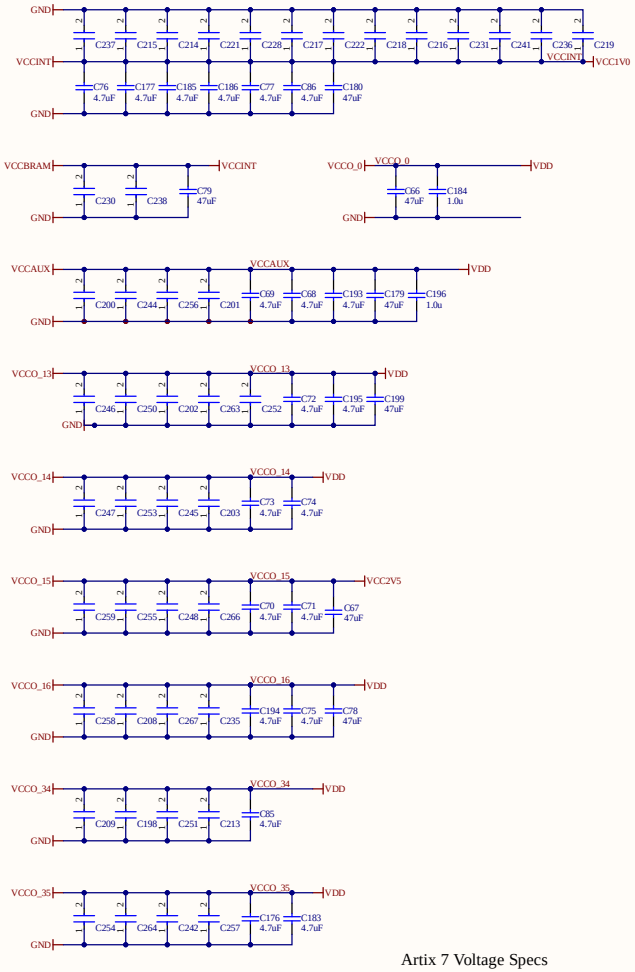
Front End Power +/- 7V
QC per channel 5.5mA * 64 = 352mA so single supplies are sufficient
DVDD 1.2V 128 * 4 = 512mA > 500mA so two supplies
VCCA 3.3V one supply
AVDD 1.8V one suppply
AVCC_R 3.3V 90*4 = 360mA one supply
AVCC_L 3.3V 90*4 = 360mA one supply
VDD_R, VDD_L 3.3V 128 per DAC * 4 = 512mA > 500mA is two supplies

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Dual Analog Supply*		
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024	Time: 11:58:12 AM	Sheet: 7 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Bipolar2.SchDoc			





FPGA Decoupling Caps



Artix 7 Voltage Specs
For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V

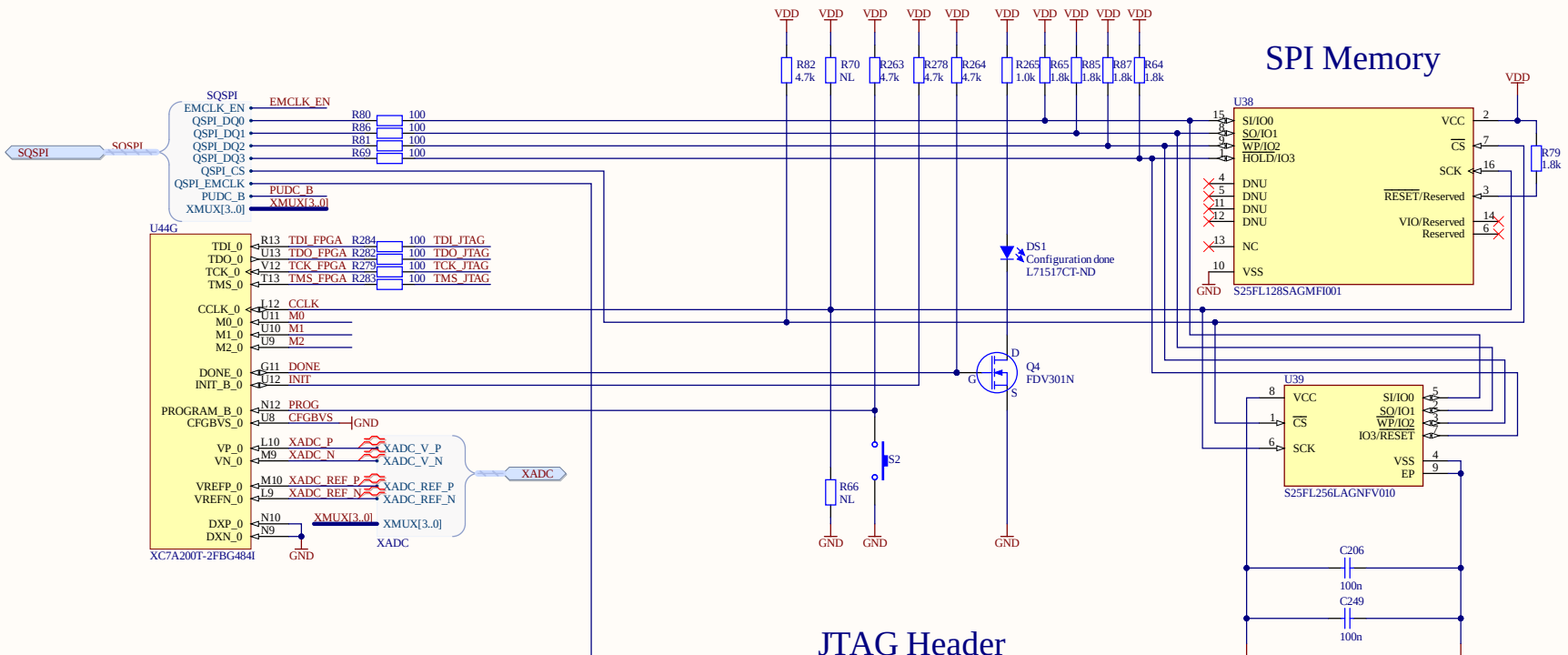
LVDS DC Specification
VCCO = 2.5
VOH = 1.675V
VOL = 0.7V

Project: LIGO DAC 32			LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title: FPGA Top			
Size: B	DCC: D2200368	Rev: 2	
Date: 7/3/2024	Time: 11:58:12 AM	Sheet 8 of 17	Drawn By: M. Pirello, D. Sigg
File: LD32_FPGA.SchDoc			

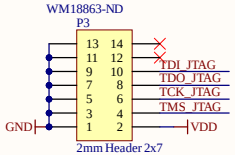
JTAG and SPI Flash

VDD is 1.8V for this design

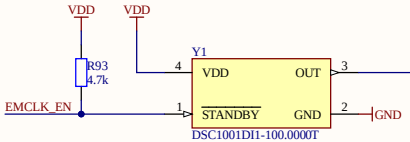
SPI Memory

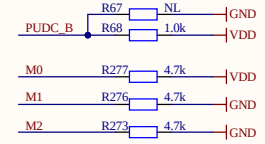


JTAG Header

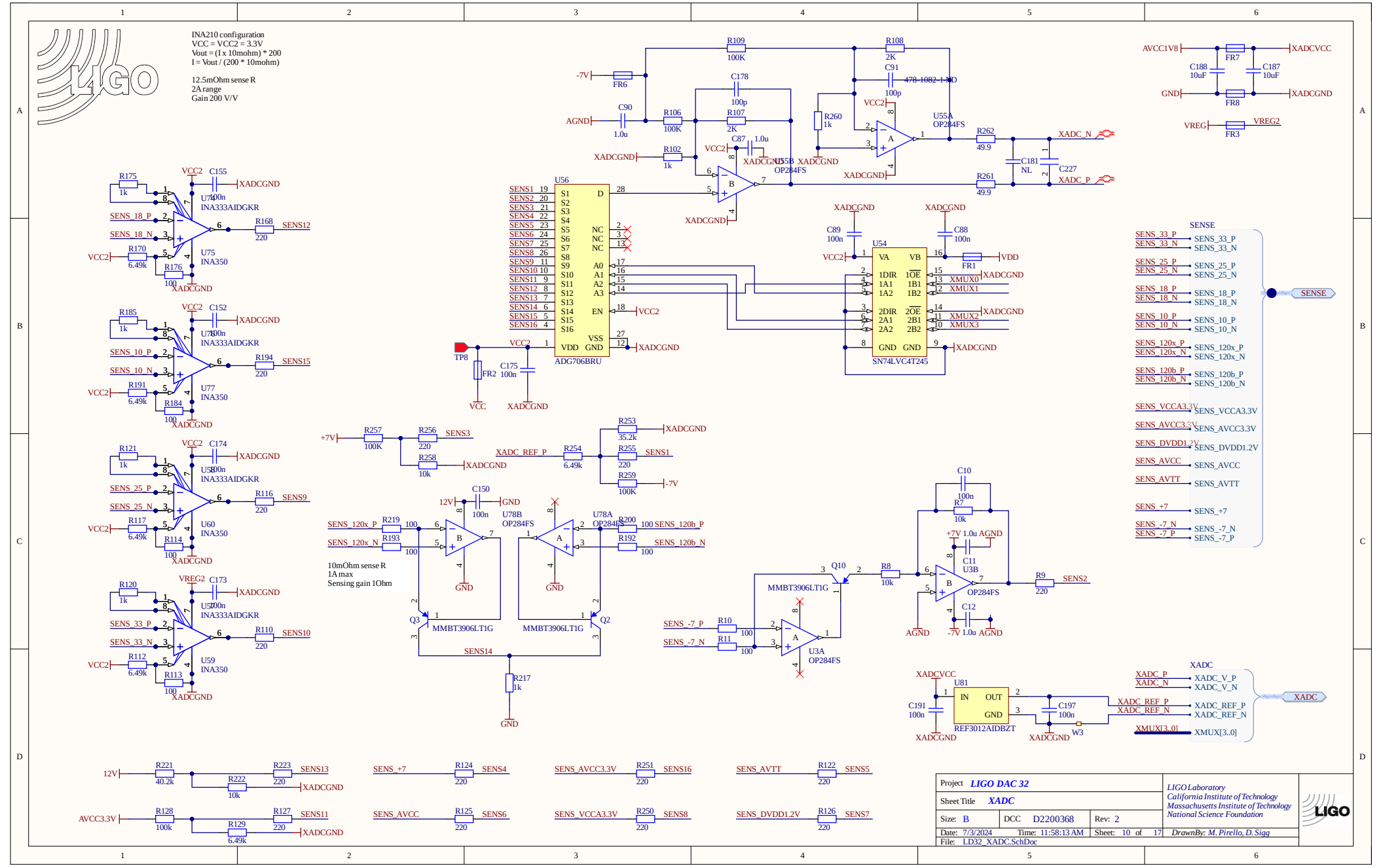


100 MHz Program Clock





Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*JTAG & SPI Flash*		
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024	Time: 11:58:12 AM	Sheet: 9 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FLASH.SchDoc			



Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*XADC*		
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024	Time: 11:58:13 AM	Sheet: 10 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_XADC.SchDoc			

DAC 1

BCLK_1 — DAC1_BCLK
LRCK_1 — DAC1_LRCK
D0_1 — DAC1_D0
D1_1 — DAC1_D1
D2_1 — DAC1_D2
D3_1 — DAC1_D3
DCLK_P_1 — DAC1_DCLK_P
DCLK_N_1 — DAC1_DCLK_N
GPIO3_1
GPIO4_1
SDA_1 — DAC1_SDA
SCL_1 — DAC1_SCL
RST_1 — DAC1_RST

DAC2

BCLK_2 — DAC2_BCLK
LRCK_2 — DAC2_LRCK
D0_2 — DAC2_D0
D1_2 — DAC2_D1
D2_2 — DAC2_D2
D3_2 — DAC2_D3
DCLK_P_2 — DAC2_DCLK_P
DCLK_N_2 — DAC2_DCLK_N
GPIO3_2
GPIO4_2
SDA_2 — DAC2_SDA
SCL_2 — DAC2_SCL
RST_2 — DAC2_RST

FPGA xADC

XADCMUX[3..0] — XADCMUX[3..0]

FPGA Config

SW[8..1] — SW8..1

FPGA Flash

QSPI_DQ0 — QSPI_DQ0
QSPI_DQ1 — QSPI_DQ1
QSPI_DQ2 — QSPI_DQ2
QSPI_DQ3 — QSPI_DQ3
QSPI_CS — QSPI_CS
EMCLK_EN — EMCLK_EN
QSPI_EMCLK — QSPI_EMCLK
PUDC_B — PUDC_B

PCIe Connector

PCIE_RX3_N — PCIE_RX3_N
PCIE_RX3_P — PCIE_RX3_P
PCIE_RX2_N — PCIE_RX2_N
PCIE_RX2_P — PCIE_RX2_P
PCIE_RX1_N — PCIE_RX1_N
PCIE_RX1_P — PCIE_RX1_P
PCIE_RX0_N — PCIE_RX0_N
PCIE_RX0_P — PCIE_RX0_P
PCIE_TX3_N — PCIE_TX3_N
PCIE_TX3_P — PCIE_TX3_P
PCIE_TX2_N — PCIE_TX2_N
PCIE_TX2_P — PCIE_TX2_P
PCIE_TX1_N — PCIE_TX1_N
PCIE_TX1_P — PCIE_TX1_P
PCIE_TX0_N — PCIE_TX0_N
PCIE_TX0_P — PCIE_TX0_P
PCIE_CLK_N — PCIE_CLK_N
PCIE_CLK_P — PCIE_CLK_P
PCIE_PERST — PCIE_PERST
PCIE_PWRGD — PCIE_PWRGD

Phase Detector

ACNV — ACNV
AIN — AIN
ACLK — ACLK
SYNC_P — SYNC_P
SYNC_N — SYNC_N
CNTROUT_N — CNTROUT_N
CNTROUT_P — CNTROUT_P
OSCCLK_P — OSCCLK_P
OSCCLK_N — OSCCLK_N

DAC3

BCLK_3 — DAC3_BCLK
LRCK_3 — DAC3_LRCK
D0_3 — DAC3_D0
D1_3 — DAC3_D1
D2_3 — DAC3_D2
D3_3 — DAC3_D3
DCLK_P_3 — DAC3_DCLK_P
DCLK_N_3 — DAC3_DCLK_N
GPIO3_3
GPIO4_3
SDA_3 — DAC3_SDA
SCL_3 — DAC3_SCL
RST_3 — DAC3_RST

DAC4

BCLK_4 — DAC4_BCLK
LRCK_4 — DAC4_LRCK
D0_4 — DAC4_D0
D1_4 — DAC4_D1
D2_4 — DAC4_D2
D3_4 — DAC4_D3
DCLK_P_4 — DAC4_DCLK_P
DCLK_N_4 — DAC4_DCLK_N
GPIO3_4
GPIO4_4
SDA_4 — DAC4_SDA
SCL_4 — DAC4_SCL
RST_4 — DAC4_RST

CLKO_P — CLKO_P
CLKO_N — CLKO_N
CLKE_P — CLKE_P
CLKE_N — CLKE_N
TRIG_P — TRIG_P
TRIG_N — TRIG_N

PWRSYNC — PWRSYNC
ASYNC0 — ASYNC0
ASYNC1 — ASYNC1

PG[9..0] — PG[9..0]

LED_PG — LED_PG
LED_A — LED_A
LED_B — LED_B
LED_C — LED_C
LED_D — LED_D

Optional External Clock

EXTCLK_1 — EXTCLK_1
EXTCLK_2 — EXTCLK_2

U44B — BANK 14 — XC7A200T-2FBG484I
U44C — BANK 15 — XC7A200T-2FBG484I
U44E — BANK 34 — XC7A200T-2FBG484I
U44D — BANK 16 — XC7A200T-2FBG484I
U44F — BANK 35 — XC7A200T-2FBG484I
U44A — BANK 13 — XC7A200T-2FBG484I

U44J — XC7A200T-2FBG484I
U44K — XC7A200T-2FBG484I
U44I — XC7A200T-2FBG484I
U44H — XC7A200T-2FBG484I

Project	LIGO DAC 32
Sheet Title	FPGA
Size	B
DCC	D2200368
Rev	2
Date	7/3/2024
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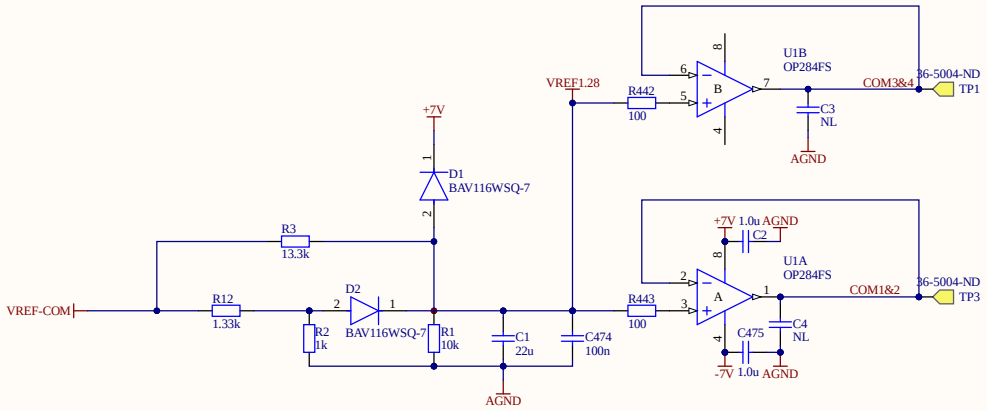
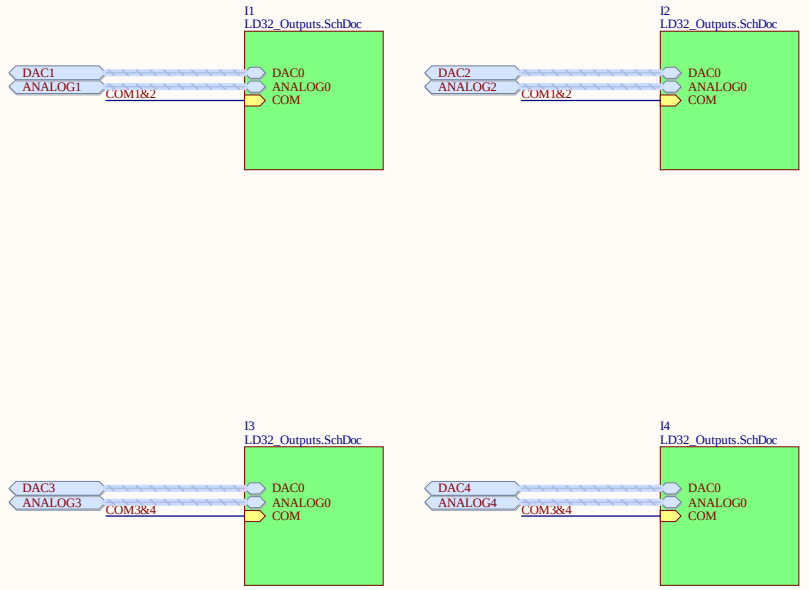
Sheet	11 of 17
File	FPGA_ARTIX7.SchDoc
Drawn By	M. Pirello, D. Sigg

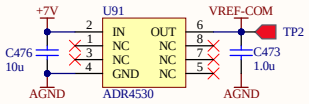
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation

Multiple DAC's COM Distro





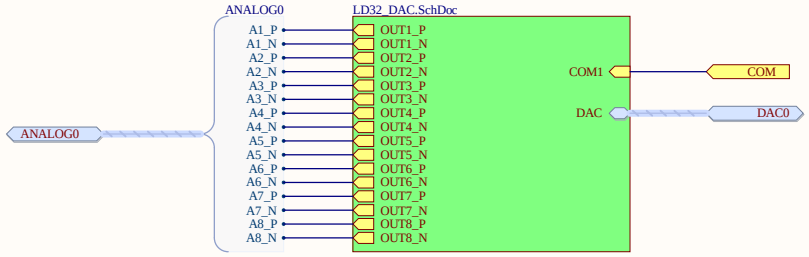
3.0V COM Reference



Parts Checked for =Value and Consistency

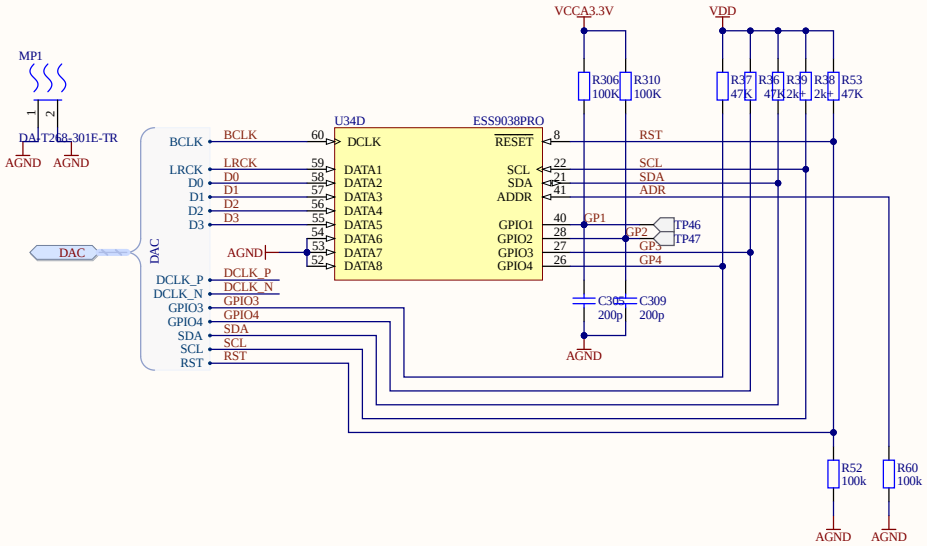
Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *DAC Top*			
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024 Time: 11:58:13 AM		Sheet: 12 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Analog.SchDoc			

DAC Overview

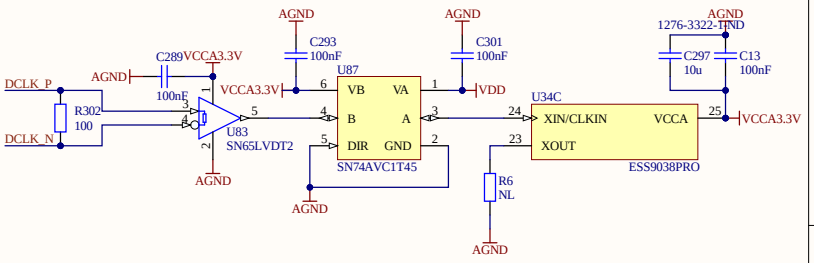


Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *DAC Overview*			
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024 Time: 11:58:13 AM		Sheet: 13 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Outputs.SchDoc			

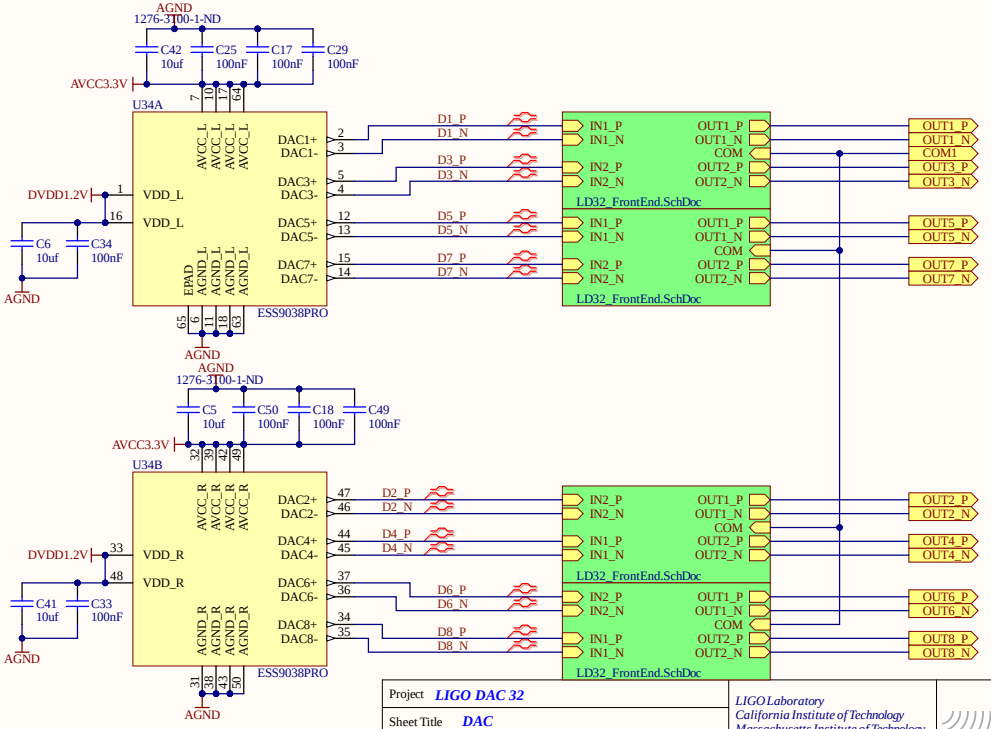
DAC Inputs



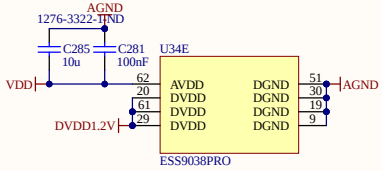
Main Clock



DAC Outputs



Core Power



Clock lines and reset could be shared in principle.

You also routed more lines than we really need.

1 fast clock (LVDS, SN65LVDS104 for FO)
1 BCLK
1 LRCLK
4 D lines
2 I2C lines
is needed per DAC.

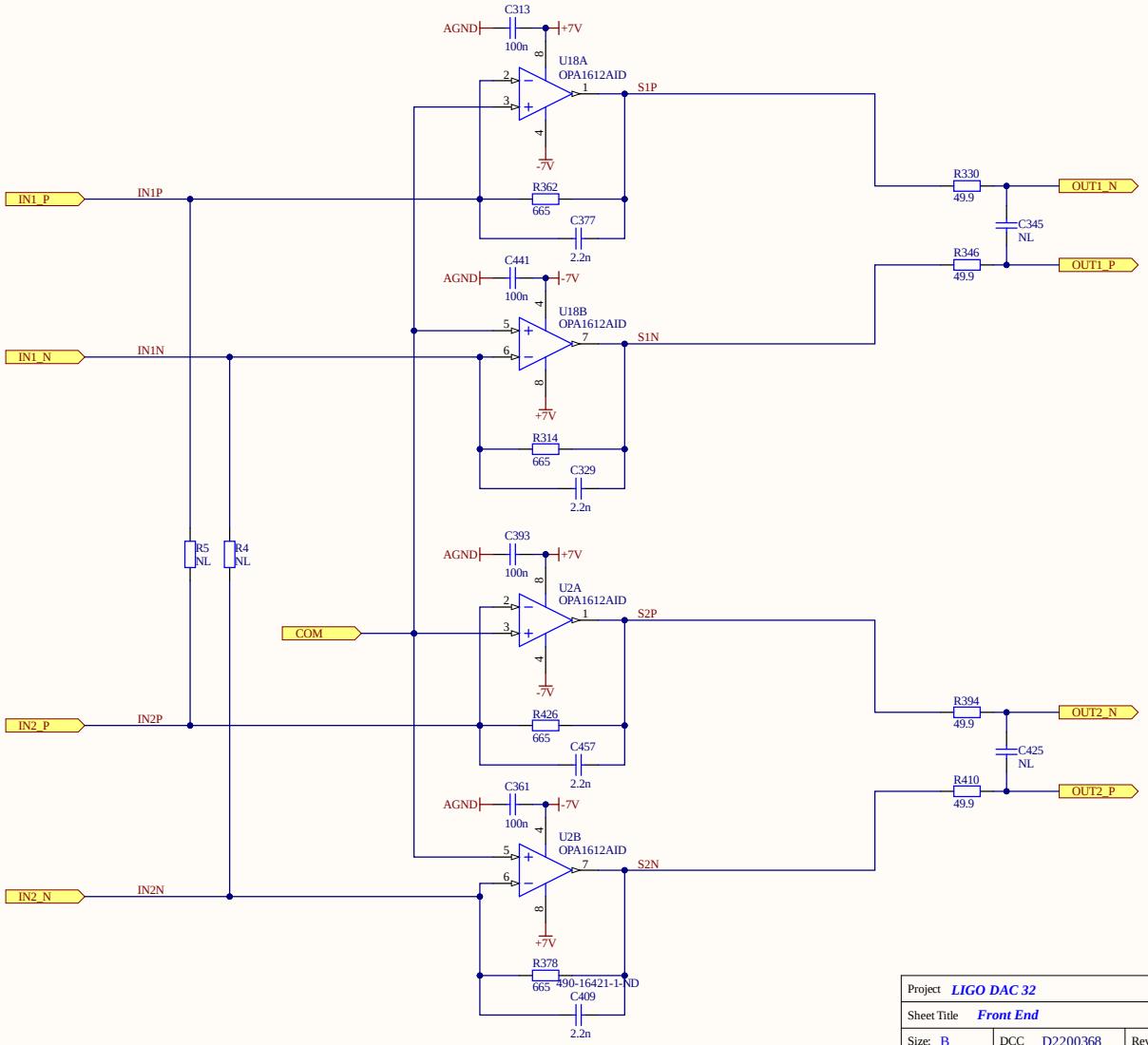
There will be a difference between Artix-7 and Artix Ultrascale with later only supporting 1.8V.

Daniel

Parts Checked for =Value and Consistency

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC*		
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024	Time: 11:58:14 AM	Sheet: 14 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_DAC.SchDoc			

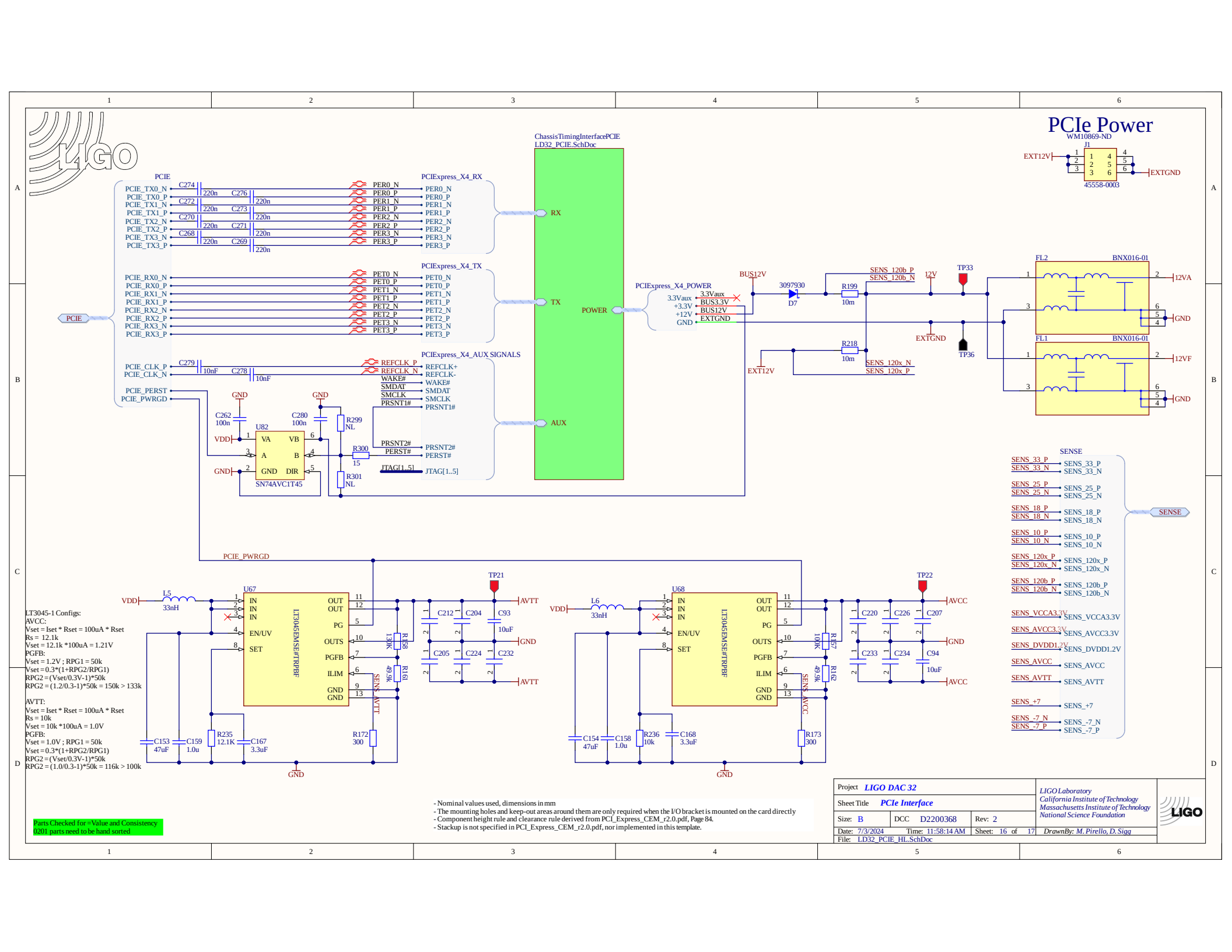
Front End Amplifiers



Parts Checked for =Value and Consistency

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Front End*		
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024 Time: 11:58:14 AM		Sheet: 15 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

PCIe Power



LT3045-1 Configs:
AVCC:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k

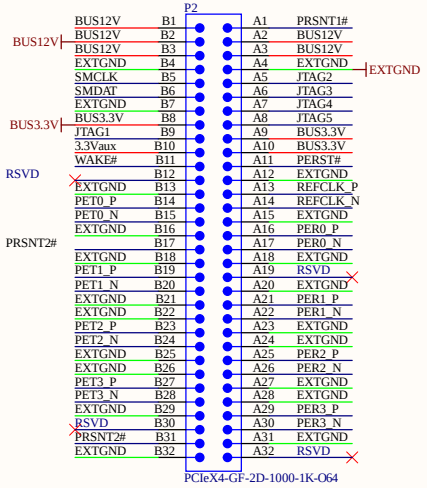
AVTT:
Vset = Iset * Rset = 100uA * Rset
Rs = 10k
Vset = 10k *100uA = 1.0V
PGFB:
Vset = 1.0V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.0/0.3-1)*50k = 116k > 100k

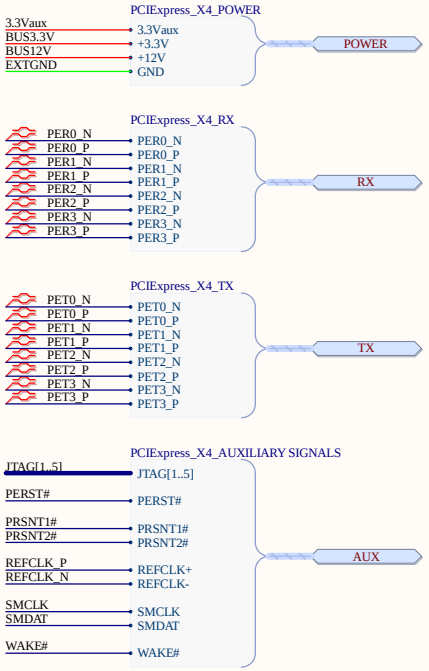
Parts Checked for =Value and Consistency
0201 parts need to be hand sorted

- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

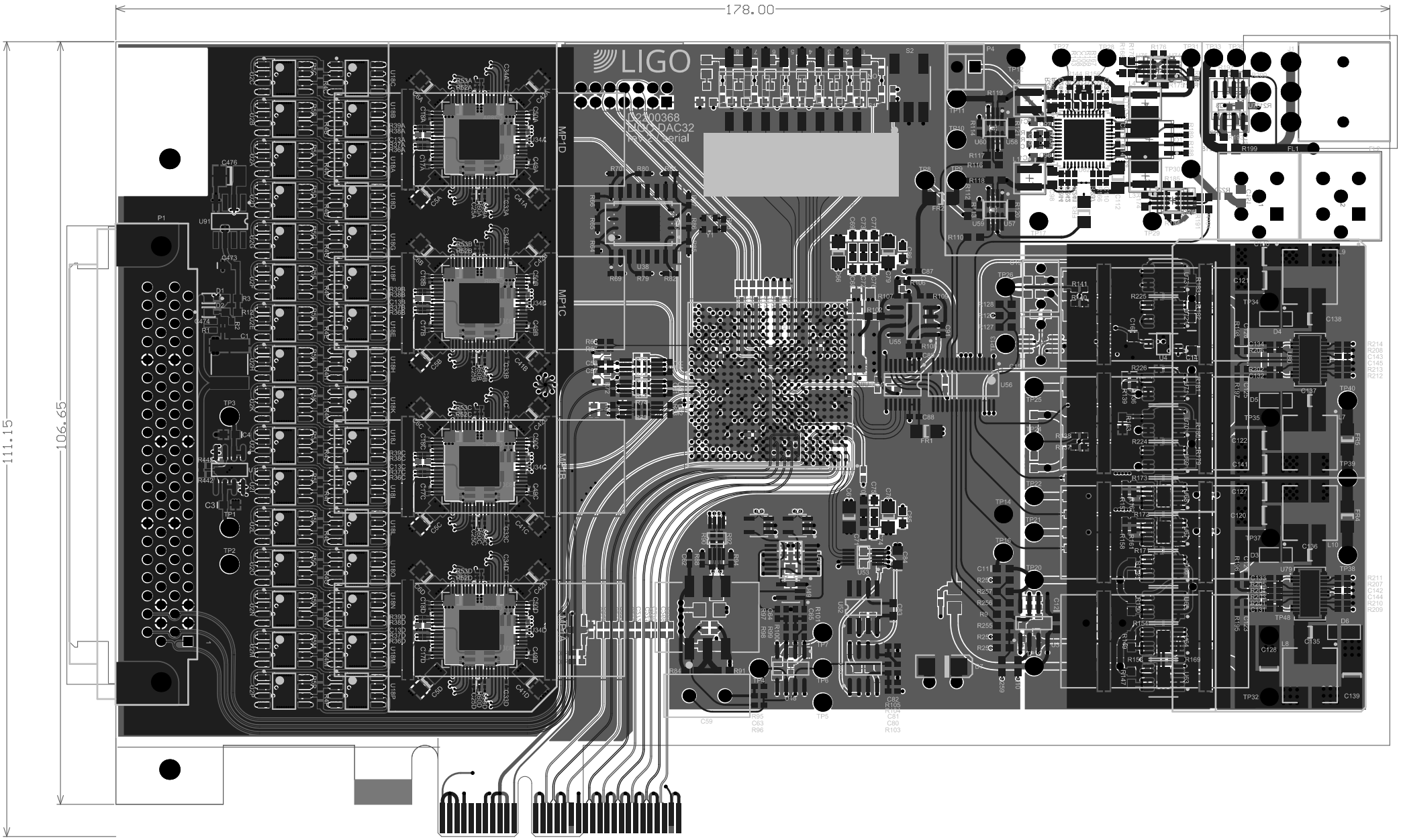
Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*PCIe Interface*		
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024	Time: 11:58:14 AM	Sheet: 16 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_PCIE_HL.SchDoc			

PCIe 4x Slot





Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *PCIe*			
Size: B	DCC D2200368	Rev: 2	
Date: 7/3/2024 Time: 11:58:14 AM		Sheet: 17 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_PCIE.SchDoc			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111.15
106.65
LIGO
D2200368
ISC_DAC32
rev A serial
MP1D
MP1C
MP1B
MP1A