



Diff Outputs to IFO

517-P50E-080P1-RR1EA
P1

OutputN1	80	79	OutputP1
OutputN3	78	77	OutputP3
OutputN5	76	75	OutputP5
OutputN7	74	73	OutputP7
OutputN6	72	71	OutputP6
OutputN8	70	69	OutputP8
OutputN2	68	67	OutputP2
OutputN4	66	65	OutputP4
OutputN9	64	63	OutputP9
OutputN11	62	61	OutputP11
OutputN13	60	59	OutputP13
OutputN15	58	57	OutputP15
OutputN14	56	55	OutputP14
OutputN16	54	53	OutputP16
OutputN10	52	51	OutputP10
OutputN12	50	49	OutputP12
OutputN17	48	47	OutputP17
OutputN19	46	45	OutputP19
OutputN21	44	43	OutputP21
OutputN23	42	41	OutputP23
OutputN22	40	39	OutputP22
OutputN24	38	37	OutputP24
OutputN18	36	35	OutputP18
OutputN20	34	33	OutputP20
OutputN25	32	31	OutputP25
OutputN27	30	29	OutputP27
OutputN29	28	27	OutputP29
OutputN31	26	25	OutputP31
OutputN30	24	23	OutputP30
OutputN32	22	21	OutputP32
OutputN26	20	19	OutputP26
OutputN28	18	17	OutputP28
OutputN33	16	15	OutputP33
OutputN34	14	13	OutputP34
OutputN35	12	11	OutputP35
OutputN36	10	9	OutputP36
OutputN37	8	7	OutputP37
OutputN38	6	5	OutputP38
OutputN39	4	3	OutputP39
OutputN40	2	1	OutputP40

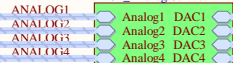
CLK_O_N	8	7	CLK_O_P
CLK_E_N	6	5	CLK_E_P
TRG_N	4	3	TRG_P

AGND AGND

OutputP1 A1_P
OutputN1 A1_N
OutputP2 A2_P
OutputN2 A2_N
OutputP3 A3_P
OutputN3 A3_N
OutputP4 A4_P
OutputN4 A4_N
OutputP5 A5_P
OutputN5 A5_N
OutputP6 A6_P
OutputN6 A6_N
OutputP7 A7_P
OutputN7 A7_N
OutputP8 A8_P
OutputN8 A8_N
OutputP9 A1_P
OutputN9 A1_N
OutputP10 A2_P
OutputN10 A2_N
OutputP11 A3_P
OutputN11 A3_N
OutputP12 A4_P
OutputN12 A4_N
OutputP13 A5_P
OutputN13 A5_N
OutputP14 A6_P
OutputN14 A6_N
OutputP15 A7_P
OutputN15 A7_N
OutputP16 A8_P
OutputN16 A8_N
OutputP17 A1_P
OutputN17 A1_N
OutputP18 A2_P
OutputN18 A2_N
OutputP19 A3_P
OutputN19 A3_N
OutputP20 A4_P
OutputN20 A4_N
OutputP21 A5_P
OutputN21 A5_N
OutputP22 A6_P
OutputN22 A6_N
OutputP23 A7_P
OutputN23 A7_N
OutputP24 A8_P
OutputN24 A8_N
OutputP25 A1_P
OutputN25 A1_N
OutputP26 A2_P
OutputN26 A2_N
OutputP27 A3_P
OutputN27 A3_N
OutputP28 A4_P
OutputN28 A4_N
OutputP29 A5_P
OutputN29 A5_N
OutputP30 A6_P
OutputN30 A6_N
OutputP31 A7_P
OutputN31 A7_N
OutputP32 A8_P
OutputN32 A8_N
CLK_O_P CLK_O_P
CLK_O_N CLK_O_N
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TRIG_P TRIG_P
TRIG_N TRIG_N
TRIGout_N TRIGout_N

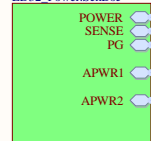
DACS

Analog
LD32_Analog.SchDoc



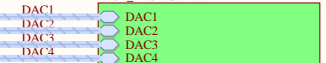
POWER

Power Supplies
LD32_Power.SchDoc



FPGA

FPGA
LD32_FPGA.SchDoc



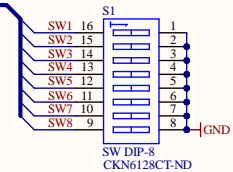
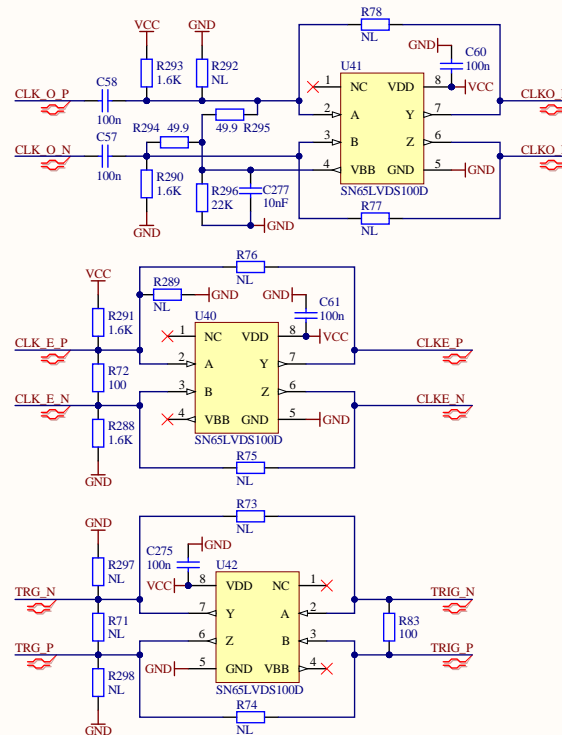
VCO Phase

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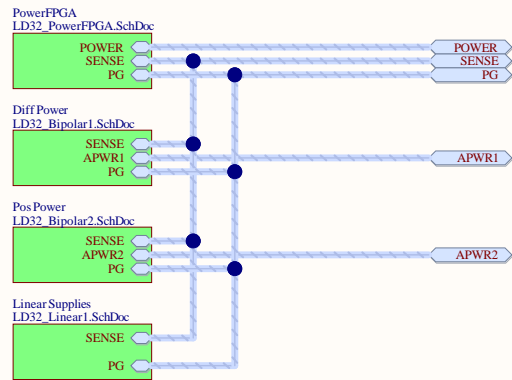



Designator

LD32_PCIE_HL.schdoc



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Sheet Title	DAC Proto Top Sheet		Rev: 2	
Size: B	DCC	D2200092	Sheet: 1 of 5	DrawnBy: M. Pirello
Date: 11/1/2022	Time: 1:23:04 PM			
File: LD32_TOP.SchDoc				



Project <i>DAC Daughter Prototype</i>			LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation		
Sheet Title <i>DAC Proto Top Sheet</i>					
Size: B	DCC D2200092	Rev: 2			
Date: 11/1/2022	Time: 1:23:04 PM	Sheet: 1 of 5	DrawnBy: <i>M. Pirello</i>		
File: LD32_Power.SchDoc					



B

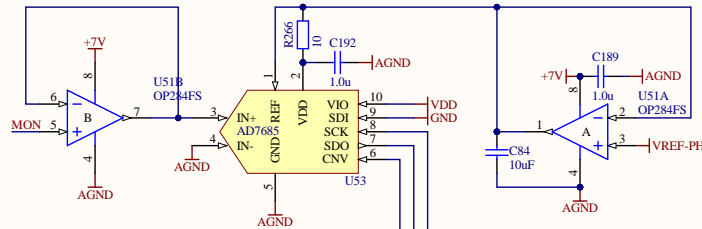
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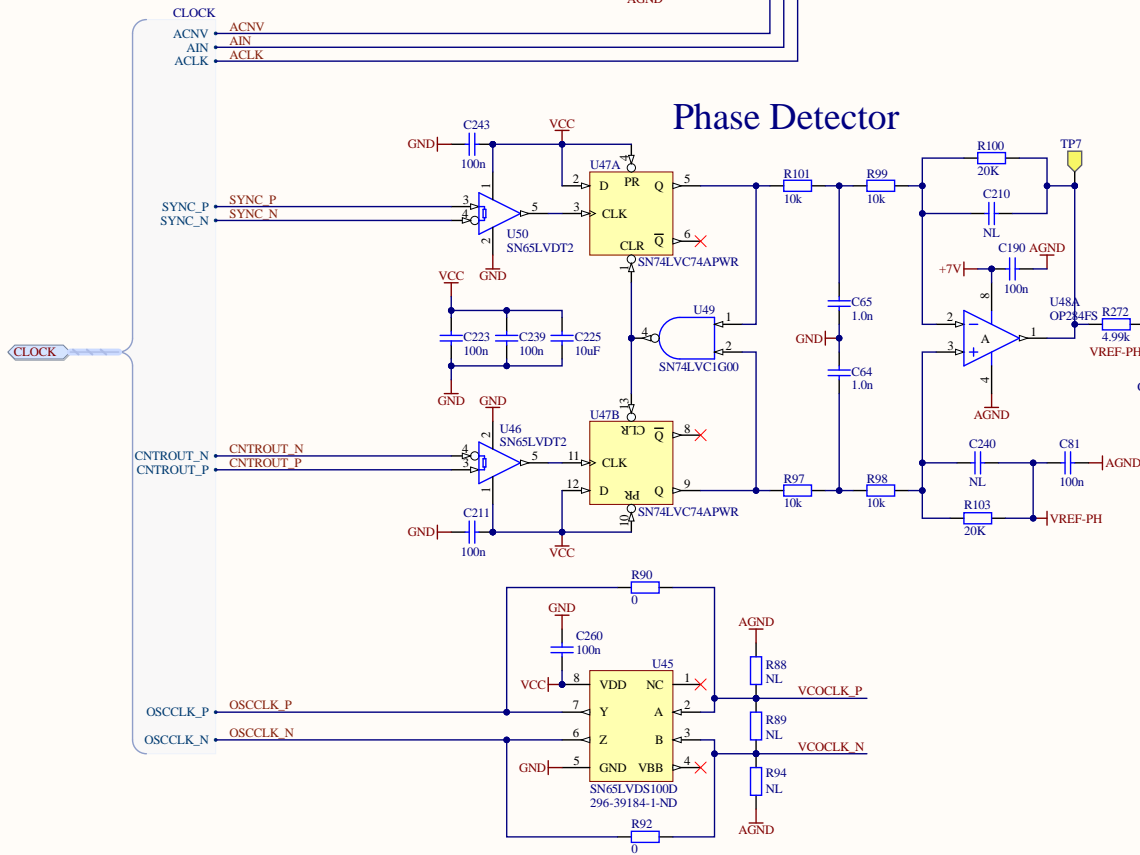
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graph TD
    POWER --> PWRSYNC
    PWRSYNC --> SENSE_33_P[SENSE_33_P]
    PWRSYNC --> SENSE_33_N[SENSE_33_N]
    PWRSYNC --> SENSE_25_P[SENSE_25_P]
    PWRSYNC --> SENSE_25_N[SENSE_25_N]
    PWRSYNC --> SENSE_18_P[SENSE_18_P]
    PWRSYNC --> SENSE_18_N[SENSE_18_N]
    PWRSYNC --> SENSE_10_P[SENSE_10_P]
    PWRSYNC --> SENSE_10_N[SENSE_10_N]
    PWRSYNC --> SENSE_120x_P[SENSE_120x_P]
    PWRSYNC --> SENSE_120x_N[SENSE_120x_N]
    PWRSYNC --> SENSE_120b_P[SENSE_120b_P]
    PWRSYNC --> SENSE_120b_N[SENSE_120b_N]
    PWRSYNC --> SENSE_VCCA3.3V[SENSE_VCCA3.3V]
    PWRSYNC --> SENSE_AVCC3.3V[SENSE_AVCC3.3V]
    PWRSYNC --> SENSE_DVDD1.2V[SENSE_DVDD1.2V]
    PWRSYNC --> SENSE_AVCC[SENSE_AVCC]
    PWRSYNC --> SENSE_AVTT[SENSE_AVTT]
    PWRSYNC --> SENSE_+7[SENSE_+7]
    PWRSYNC --> SENSE_-7[SENSE_-7]
    PWRSYNC --> SENSE_A[SENSE_A]
    PWRSYNC --> SENSE_B[SENSE_B]
    PWRSYNC --> SENSE_C[SENSE_C]
  
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Control Voltage Monitor

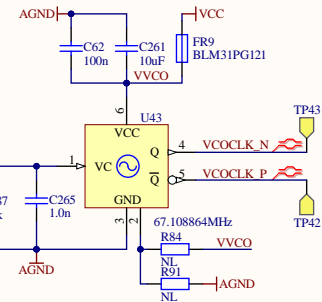


Phase Detector

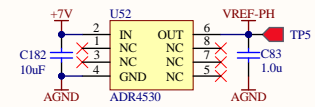


Optional LVPECL-LVDS Translator

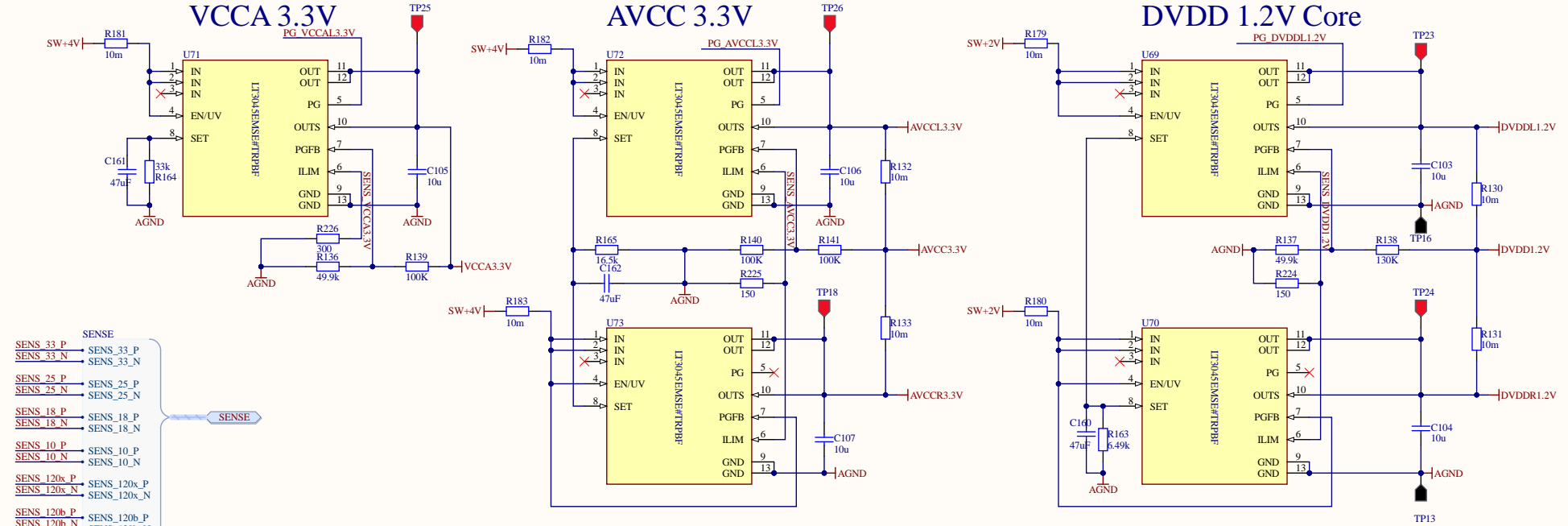
Vectron VCO



3.0V Reference



Project DAC Daughter Prototype			LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
Sheet Title VCO & Phase Detector				
Size: B	DCC D2200092	Rev: 2		
Date: 11/1/2022	Time: 1:23:07 PM	Sheet: 2 of 12	Drawn By: M. Pirello	
File: LD32_PHASE.SchDoc				



- SENSE
- SENS_33_P
SENS_33_N
- SENS_25_P
SENS_25_N
- SENS_18_P
SENS_18_N
- SENS_10_P
SENS_10_N
- SENS_120x_P
SENS_120x_N
- SENS_120b_P
SENS_120b_N
- SENS_VCCA3.3V
SENS_AVCC3.3V
- SENS_DVDDL1.2V
SENS_AVCC
- SENS_AVTT
SENS_AVTT
- SENS_+7
SENS_+7
- SENS_-7
SENS_-7
- SENS_A
SENS_B
SENS_C

LT3045-1 Configs:
VCCA3V3
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k * 100uA = 3.3V
PGFB:
Vset = 3.3V ; RGP2 = 100k
Vset = 0.3*(1+RGP2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

AVCC3V3:
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k * 100uA = 3.3V
PGFB:
Vset = 3.3V ; RGP2 = 100k
Vset = 0.3*(1+RGP2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

LT3045-1 Configs:
DVDDL1V2:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k * 100uA = 1.21V
PGFB:
Vset = 1.2V ; RGP1 = 50k
Vset = 0.3*(1+RGP2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k

- POWER GOOD
- PG_VCCA3.3V
PG_AVCC3.3V
PG_DVDDL1.2V
PG_SW+2V
PG_SW+4V
PWRGOOD
PG_SW+8V
PG_SW-8V
PG-7
PG+7
- PG_VCCA3.3V
PG_AVCC3.3V
PG_DVDDL1.2V
PG_SW+2V
PG_SW+4V
PG_FPGA
PG_SW+8
PG_SW-8
PG_L-7V
PG_L+7V

Project	DAC Daughter Prototype	LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	DAC Proto Linear Supplies	
Size: B	DCC D2200092	Rev: 2
Date: 11/1/2022	Time: 1:23:08 PM	Sheet: 2 of 19
File: LD32_Linear1.SchDoc		Drawn By: M. Pirello





B



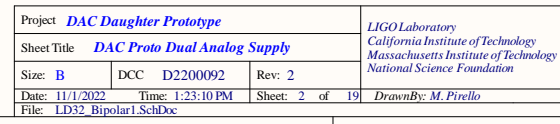
A

B

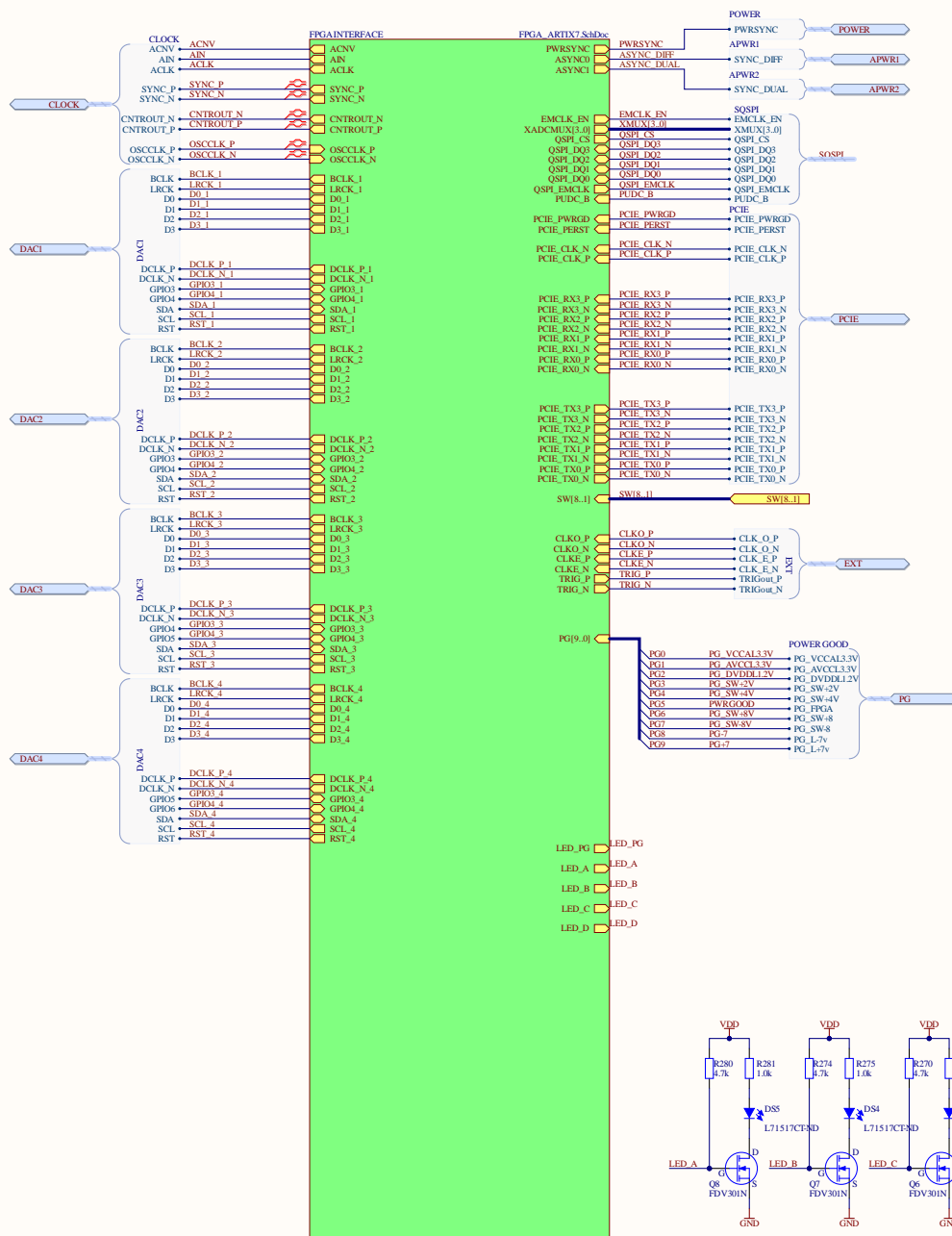
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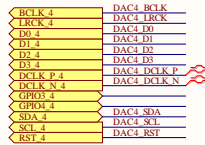
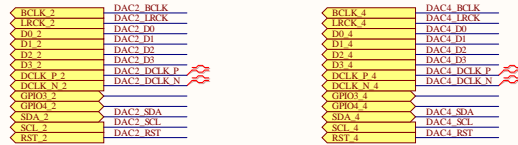
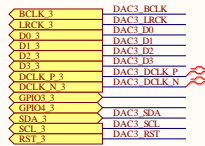
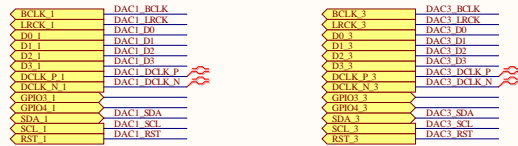
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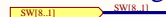


Project	<i>DAC Daughter Prototype</i>			<i>LJGO Laboratory</i> <i>California Institute of Technology</i> <i>Massachusetts Institute of Technology</i> <i>National Science Foundation</i>
Sheet Title	<i>DAC Proto Dual Analog Supply</i>			
Size:	B	DCC D2200092	Rev: 2	
Date:	11/1/2022	Time: 1:23:10 PM	Sheet: 2 of 19	
File:	LD32 Bipolar1.SchDoc			<i>DrawnBy: M. Pirello</i>





XADCMUX[3..0] XADCMUX[3..0]

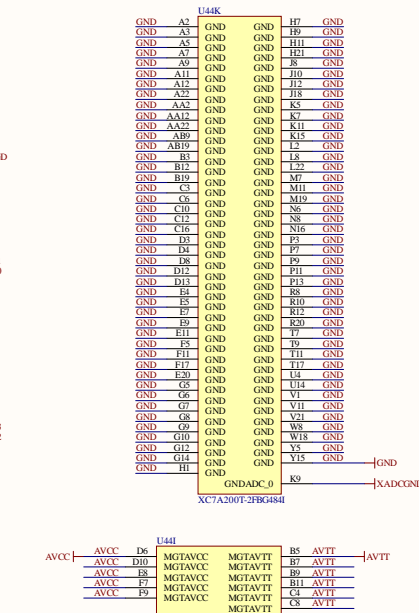
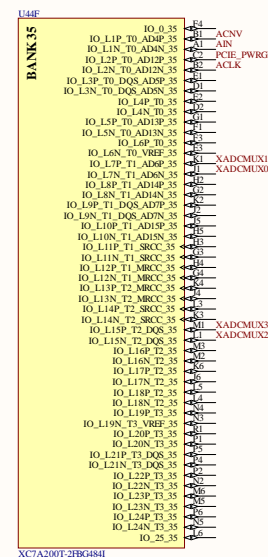
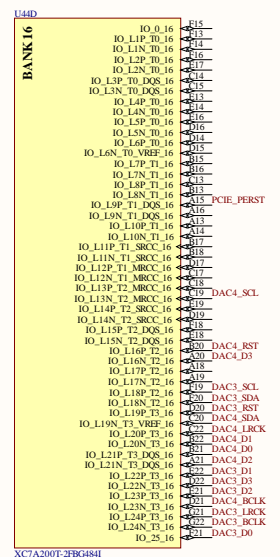
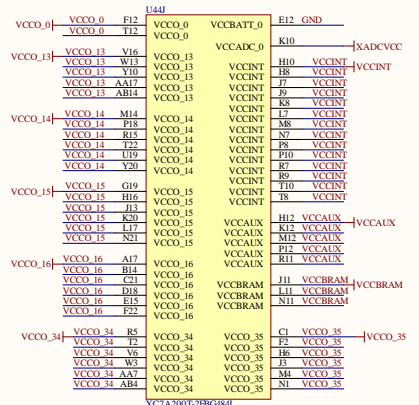
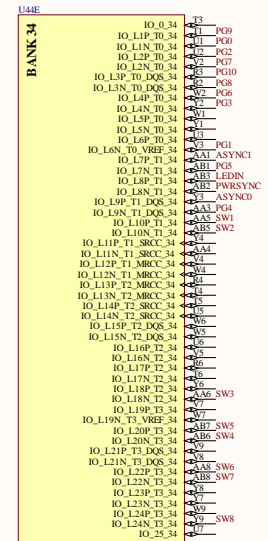
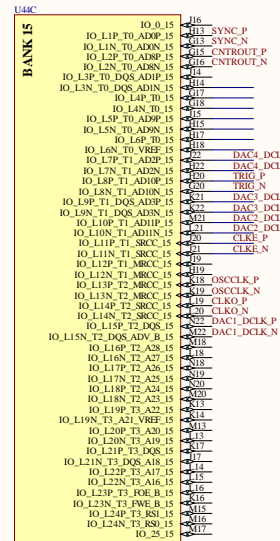
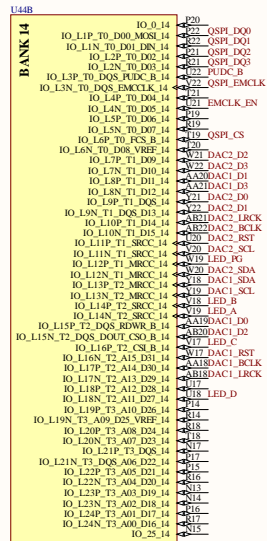


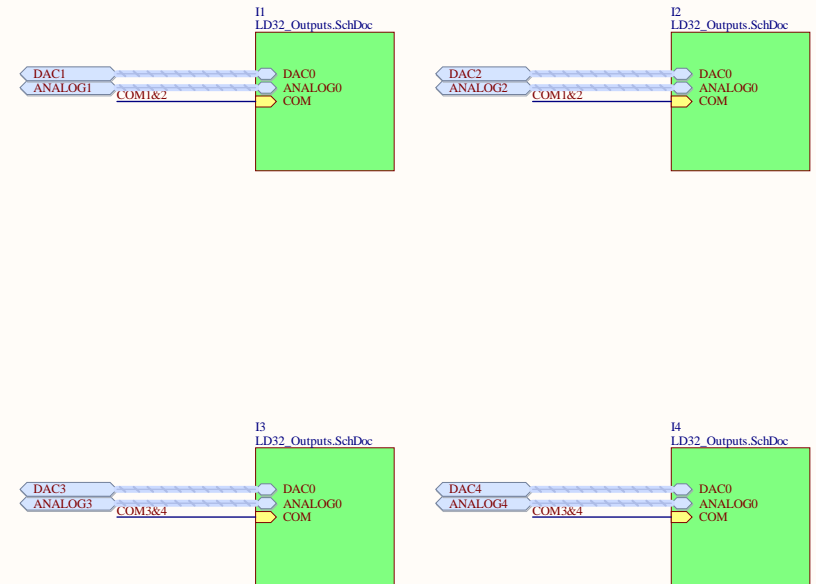
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QSPI D01	QSPI D01		
QSPI D02	QSPI D02		
QSPI D03	QSPI D03		
QSPI CS	QSPI CS	CLKO_P	CLKO_P
EMCLK_EN	EMCLK_EN	CLKO_N	CLKO_N
QSPI_EMCLK	QSPI_EMCLK	CLKE_P	CLKE_P
		CLKE_N	CLKE_N
PUDC_B	PUDC_B	CLKE_N	TRIG_P
		TRIG_P	TRIG_N



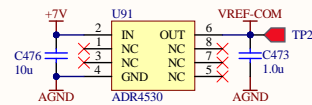
Figure 1: Schematic diagram of the proposed 16-channel 100-Gbit/s optical OFDM system. The diagram illustrates the system architecture, showing the connection between the PCIE (Peripheral Component Interconnect Express) and the LED (Light Emitting Diode) components. The system is divided into two main sections: the top section for PCIE signals and the bottom section for LED signals. The top section shows a 16-channel system with 16 input/output ports, labeled PCIE_RX3_N, PCIE_RX3_P, PCIE_RX2_N, PCIE_RX2_P, PCIE_RX1_N, PCIE_RX1_P, PCIE_RX0_N, PCIE_RX0_P, PCIE_TX3_N, PCIE_TX3_P, PCIE_TX2_N, PCIE_TX2_P, PCIE_TX1_N, PCIE_TX1_P, PCIE_TX0_N, and PCIE_TX0_P. The bottom section shows a 16-channel system with 16 input/output ports, labeled LED_PG, LED_A, LED_B, LED_C, and LED_D. The system is connected to a 16-channel 100-Gbit/s optical OFDM system, which is represented by a large yellow box labeled PCIE_PWRGD and PCIE_PERST. The system is also connected to a 16-channel 100-Gbit/s optical OFDM system, which is represented by a large yellow box labeled PCIE_PWRGD and PCIE_PERST.

ACNV	AINV
AIN	AIN
ACLK	ACLK
SYNC_P	SYNC_P
SYNC_N	SYNC_N
CNTRROUT_N	CNTRROUT_N
CNTRROUT_P	CNTRROUT_P
OSCLK_P	OSCLK_P
OSCLK_N	OSCLK_N





3.0V COM Reference

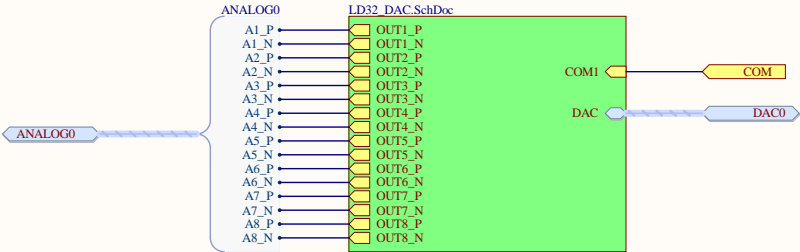


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Sheet Title <i>DAC Proto DAC Outputs</i>			
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:15 PM	Sheet: 9 of 19	
File: LD32_Analog_SchDoc			
			<i>DrawnBy: M. Pirello</i>





DAC Overview

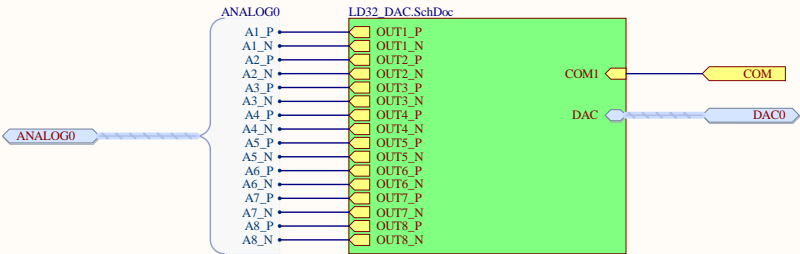


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Sheet Title DAC Proto DAC Outputs				
Size: B	DCC	D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:16 PM	Sheet: 9 of 19	Drawn By: M. Pirello	
File: LD32_Outputs.SchDoc				





DAC Overview

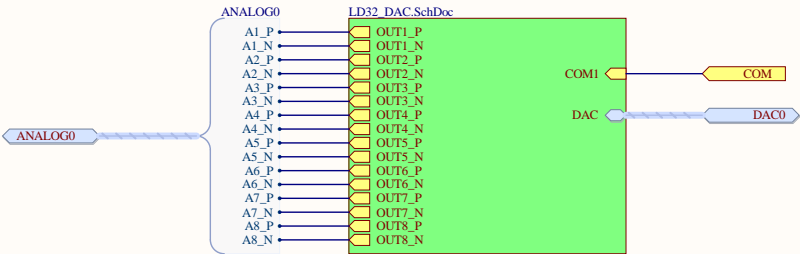


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Size: B	DCC	D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:16 PM	Sheet: 9 of 19	Drawn By: M. Pirello	
File: LD32_Outputs.SchDoc				





DAC Overview

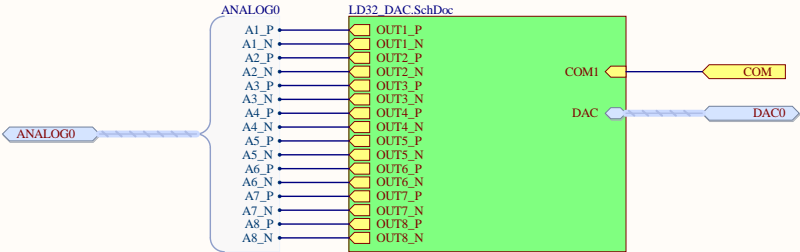


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Sheet Title DAC Proto DAC Outputs					
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File: LD32_Outputs.SchDoc					



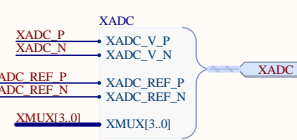
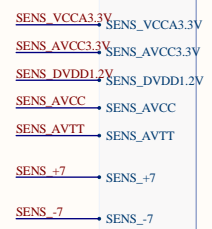
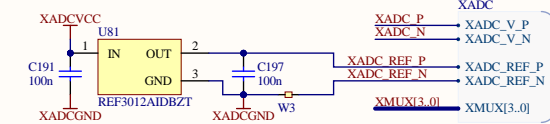
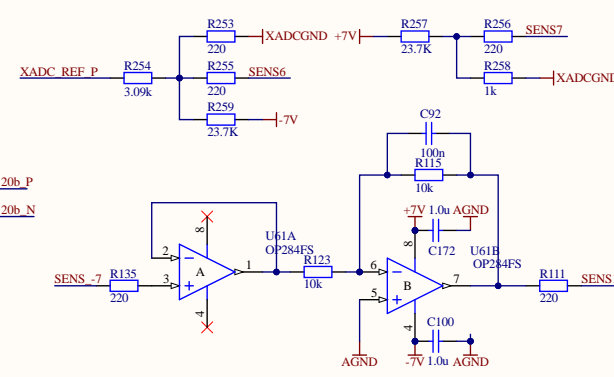
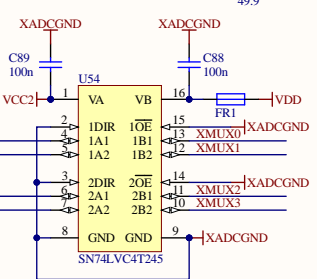
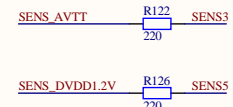
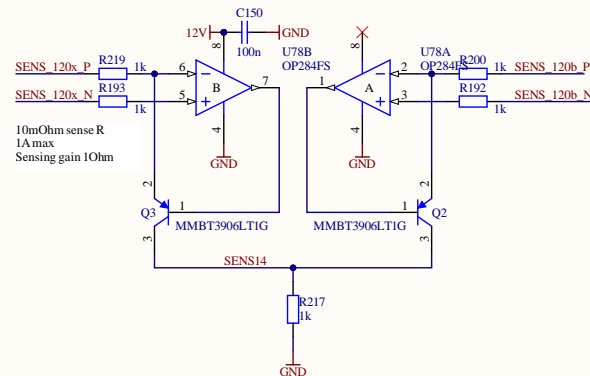
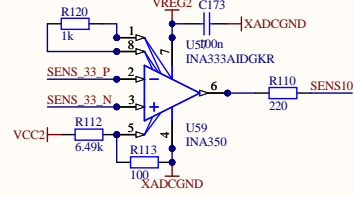
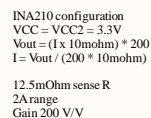


DAC Overview



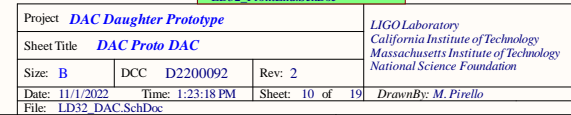
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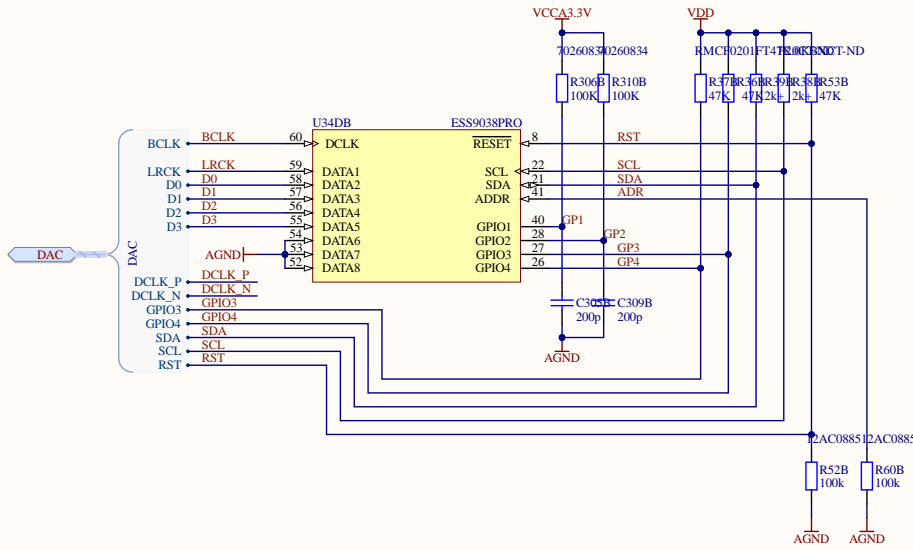
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Date: <i>11/1/2022</i>	Time: <i>1:23:18 PM</i>	Sheet: 10 of 12	DrawnBy: <i>M. Pirello</i>	
File: <i>1.D32_XADC_SchDoc</i>				



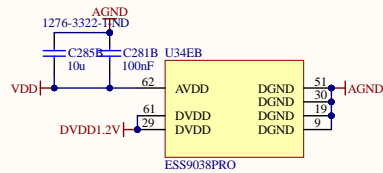




DAC Inputs



Core Power



Clock lines and reset could be shared in principle.

You also routed more lines than we really need.

1 fast clock (LVDS, SN65LVDS104 for FO)

1 BCLK

1 LRCLK

4 D lines

2 I2C lines

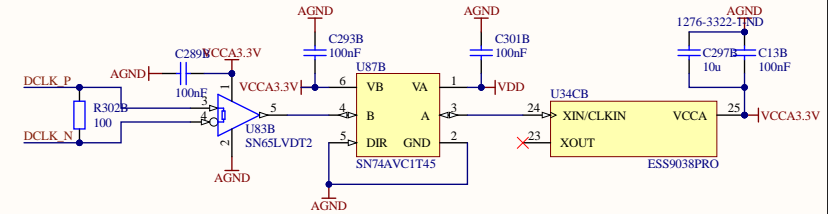
is needed per DAC.

There will be a difference between Artix-7 and Artix Ultrascale with later only supporting 1.8V.

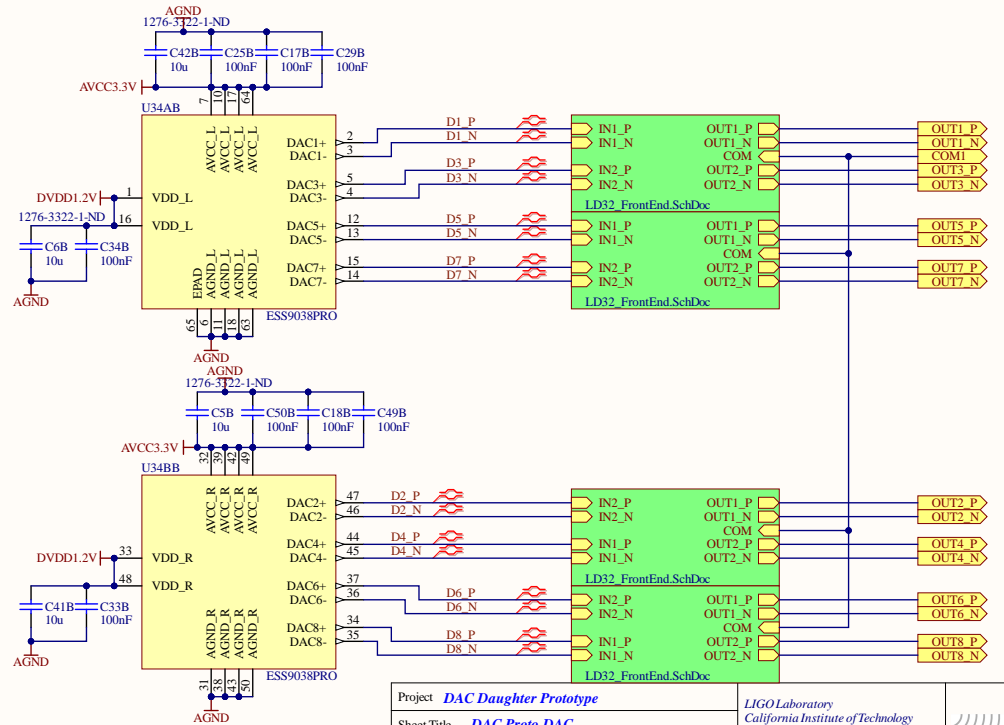
Daniel

Parts Checked for Value and Consistency

Main Clock



DAC Outputs

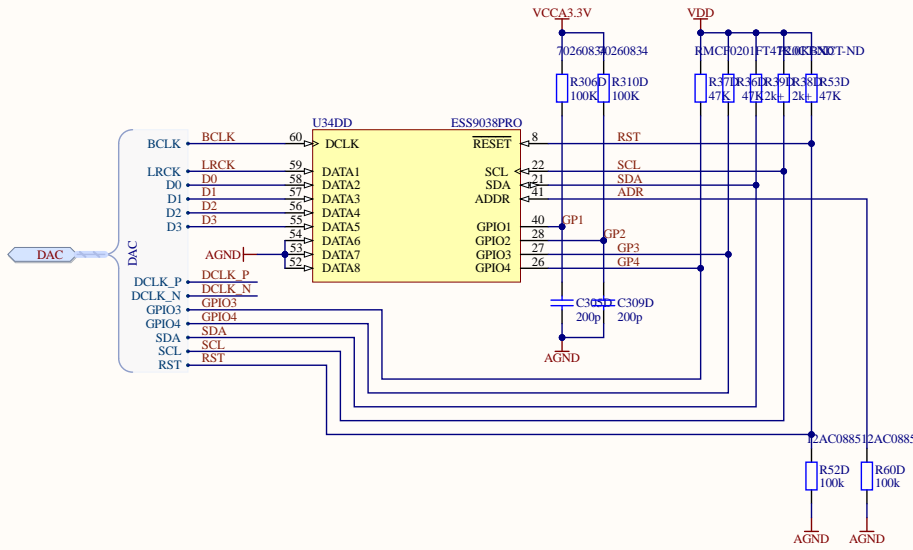


Project	DAC Daughter Prototype		LIGO Laboratory	
Sheet Title	DAC Proto DAC		California Institute of Technology	
Size:	B	DCC D2200092	Rev: 2	Massachusetts Institute of Technology
Date:	11/1/2022	Time: 1:23:19 PM	Sheet: 10 of 19	National Science Foundation
File:	LD32_DAC.SchDoc	DrawnBy: M. Pirello		

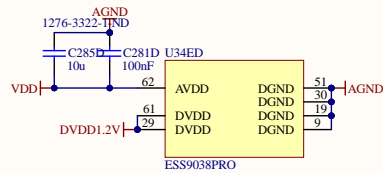




DAC Inputs



Core Power



Clock lines and reset could be shared in principle.

You also routed more lines than we really need.

1 fast clock (LVDS, SN65LVDS104 for FO)

1 BCLK

1 LRCLK

4 D lines

2 I2C lines

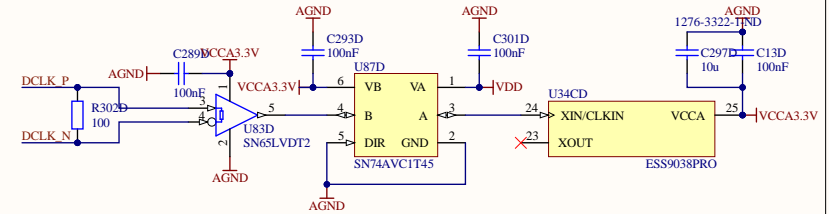
is needed per DAC.

There will be a difference between Artix-7 and Artix Ultrascale with later only supporting 1.8V.

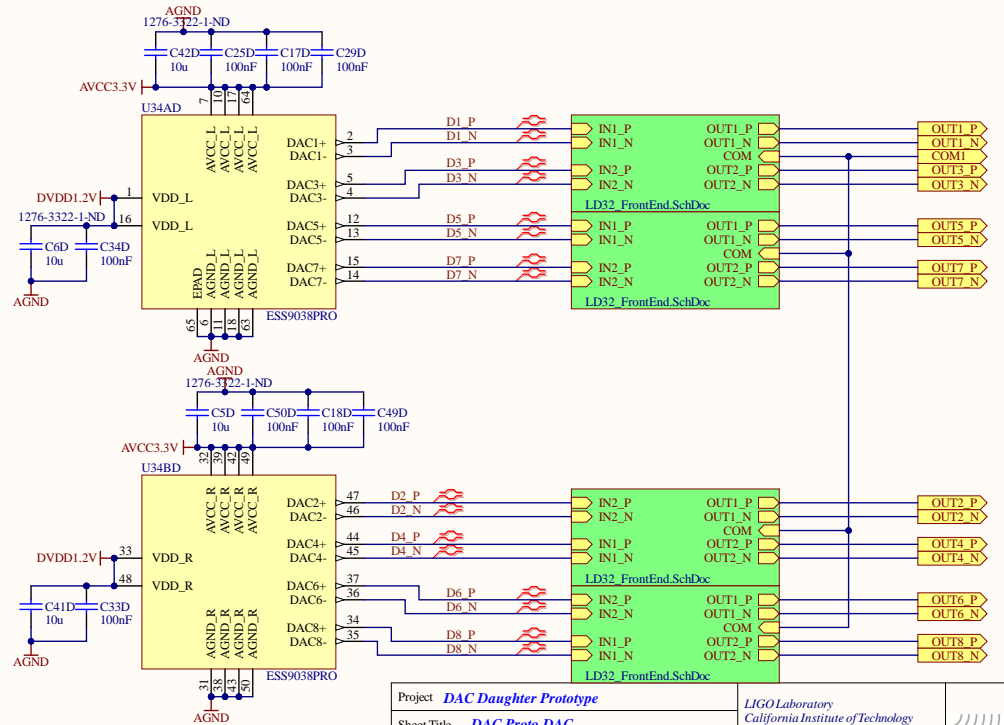
Daniel


Parts Checked for Value and Consistency

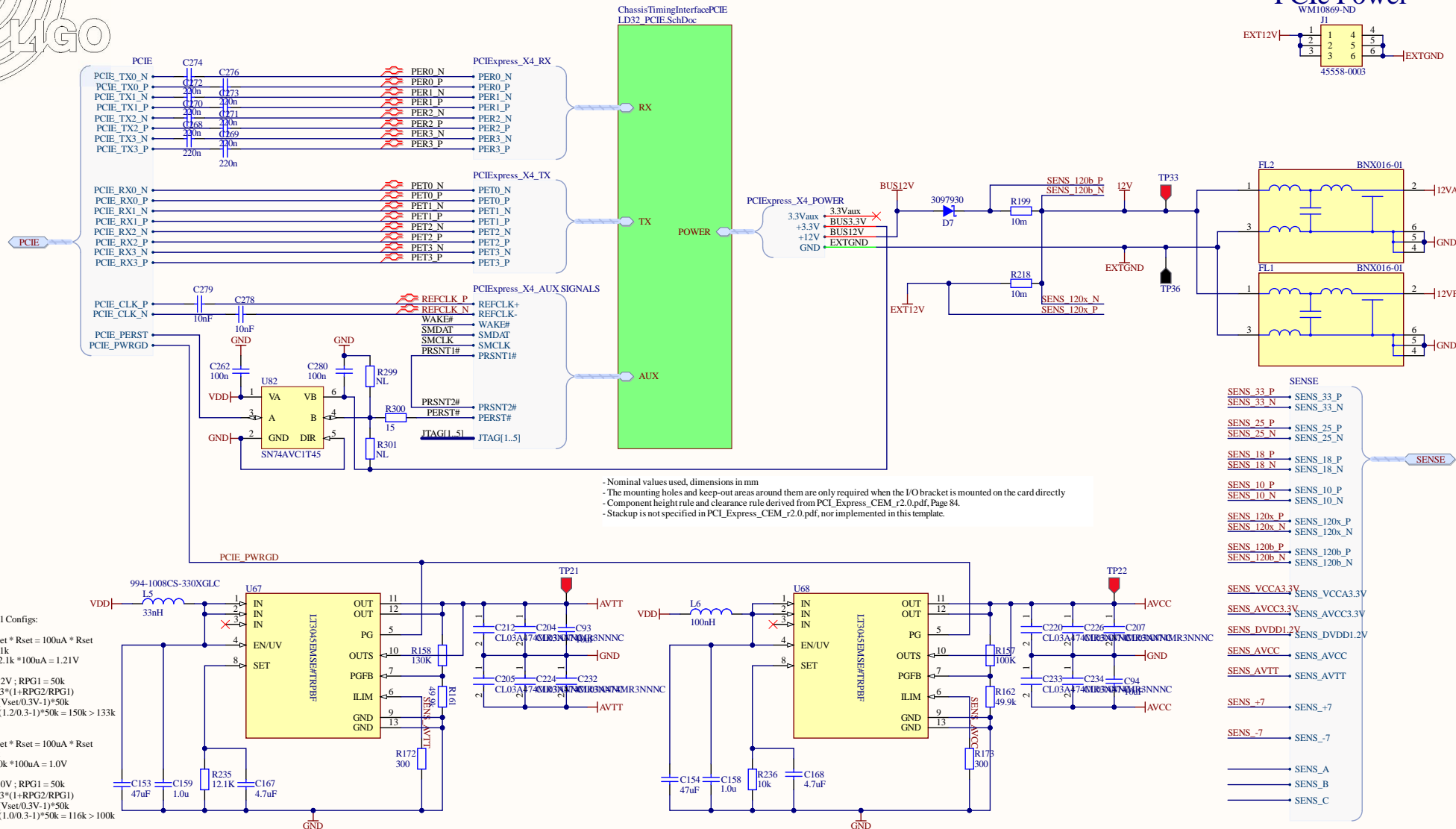
Main Clock



DAC Outputs

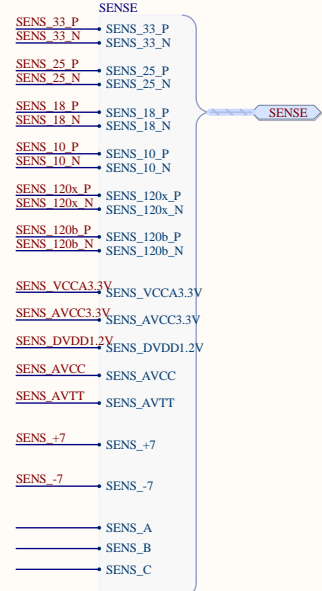
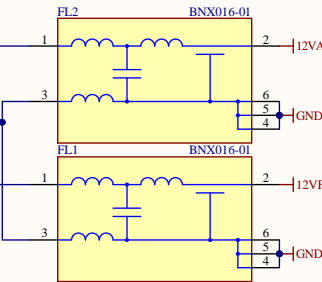
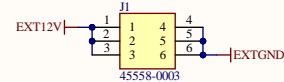


Project <i>DAC Daughter Prototype</i>			<div>LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation</div> 
Sheet Title <i>DAC Proto DAC</i>			
Size: B	DCC D22000092	Rev: 2	
Date: 11/1/2022	Time: 1:23:20 PM	Sheet: 10 of 19	
File: LD32_DAC.SchDoc		DrawnBy: <i>M. Pirello</i>	



PCIe Power

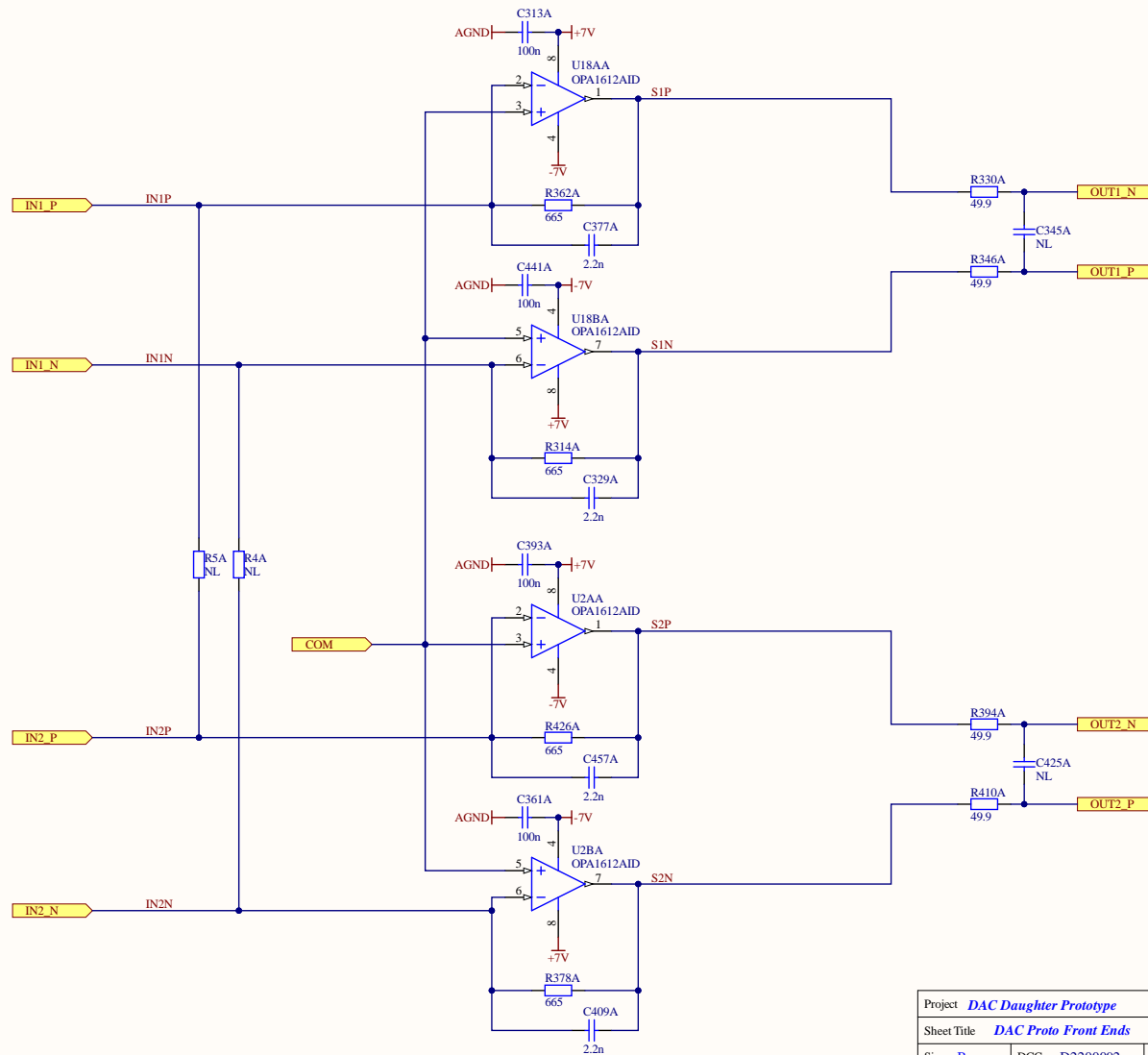
WM10869-ND



- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

Project	DAC Daughter Prototype		LIGO Laboratory	
Sheet Title	PCIe Interface		California Institute of Technology	
Size:	B	DCC	D22000092	Rev: 2
Date:	11/1/2022	Time:	1:23:21 PM	Sheet: 11 of 12
File:	LD32_PCIE_HL_SchDoc		Drawn By: M. Pirello	

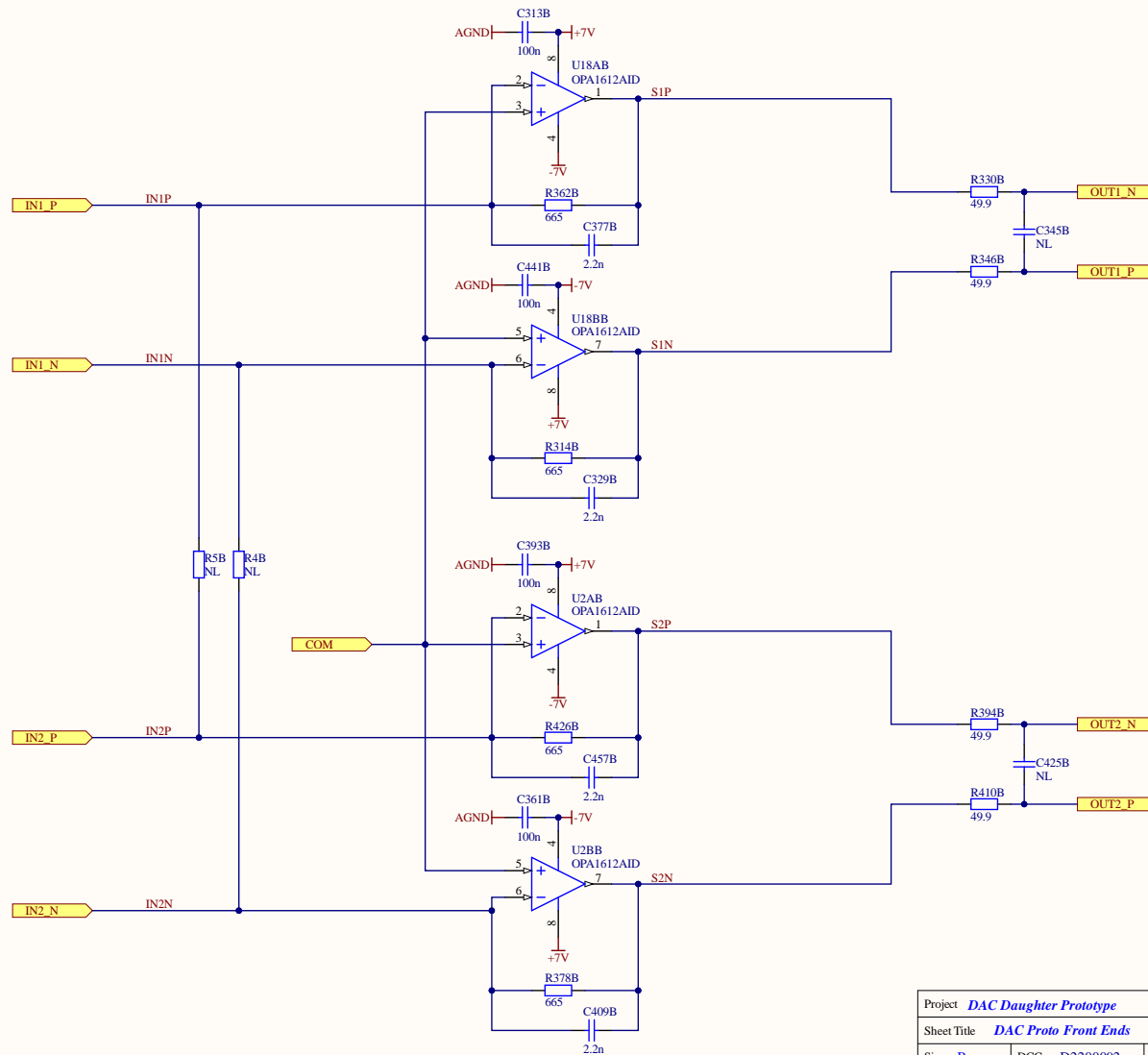




Parts Checked For Value and Consistency

Project <i>DAC Daughter Prototype</i>			<i>LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation</i>
Sheet Title <i>DAC Proto Front Ends</i>			
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:22 PM	Sheet: 11 of 19	
File: LD32_FrontEnd.SchDoc			<i>Drawn By: M. Pirello</i>

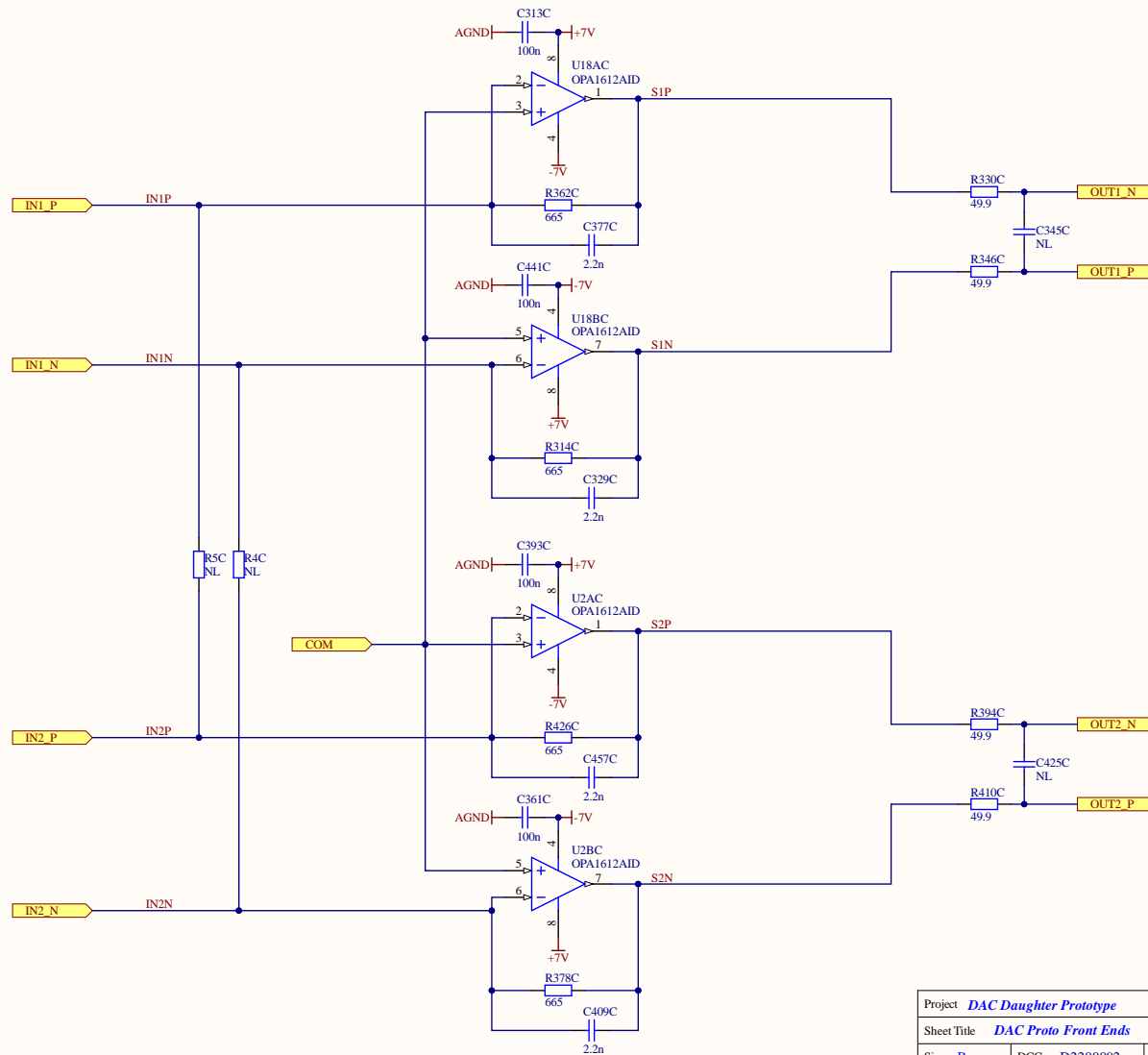




Parts Checked For Value and Consistency

Project DAC Daughter Prototype		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
Sheet Title DAC Proto Front Ends			
Size: B	DCC D22000092	Rev: 2	
Date: 11/1/2022	Time: 1:23:22 PM	Sheet: 11 of 19	Drawn By: M. Pirello
File: LD32_FrontEnd.SchDoc			

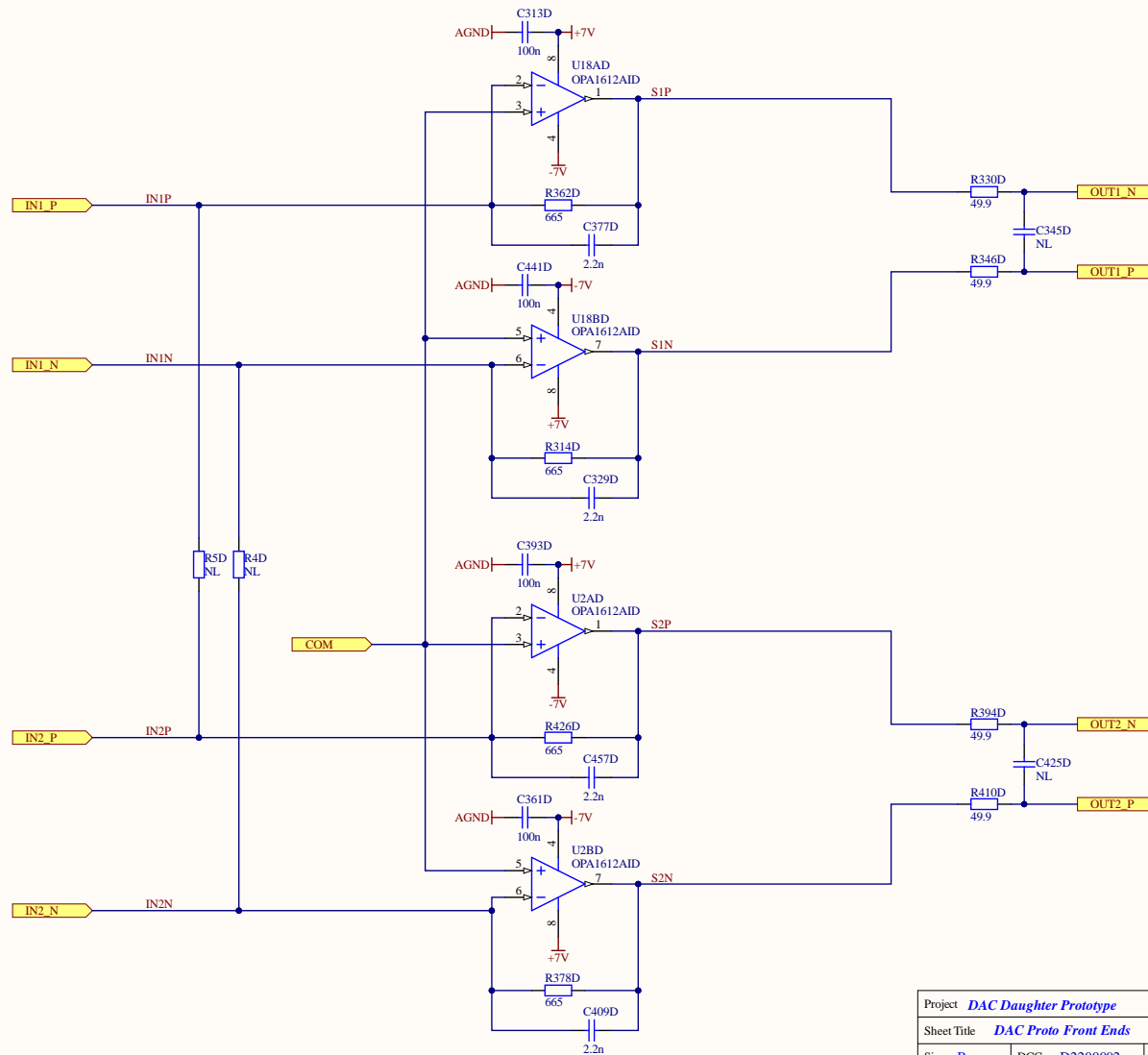




Parts Checked For Value and Consistency

Project DAC Daughter Prototype		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
Sheet Title DAC Proto Front Ends			
Size: B	DCC D22000092	Rev: 2	
Date: 11/1/2022	Time: 1:23:22 PM	Sheet: 11 of 19	Drawn By: M. Pirello
File: LD32_FrontEnd.SchDoc			

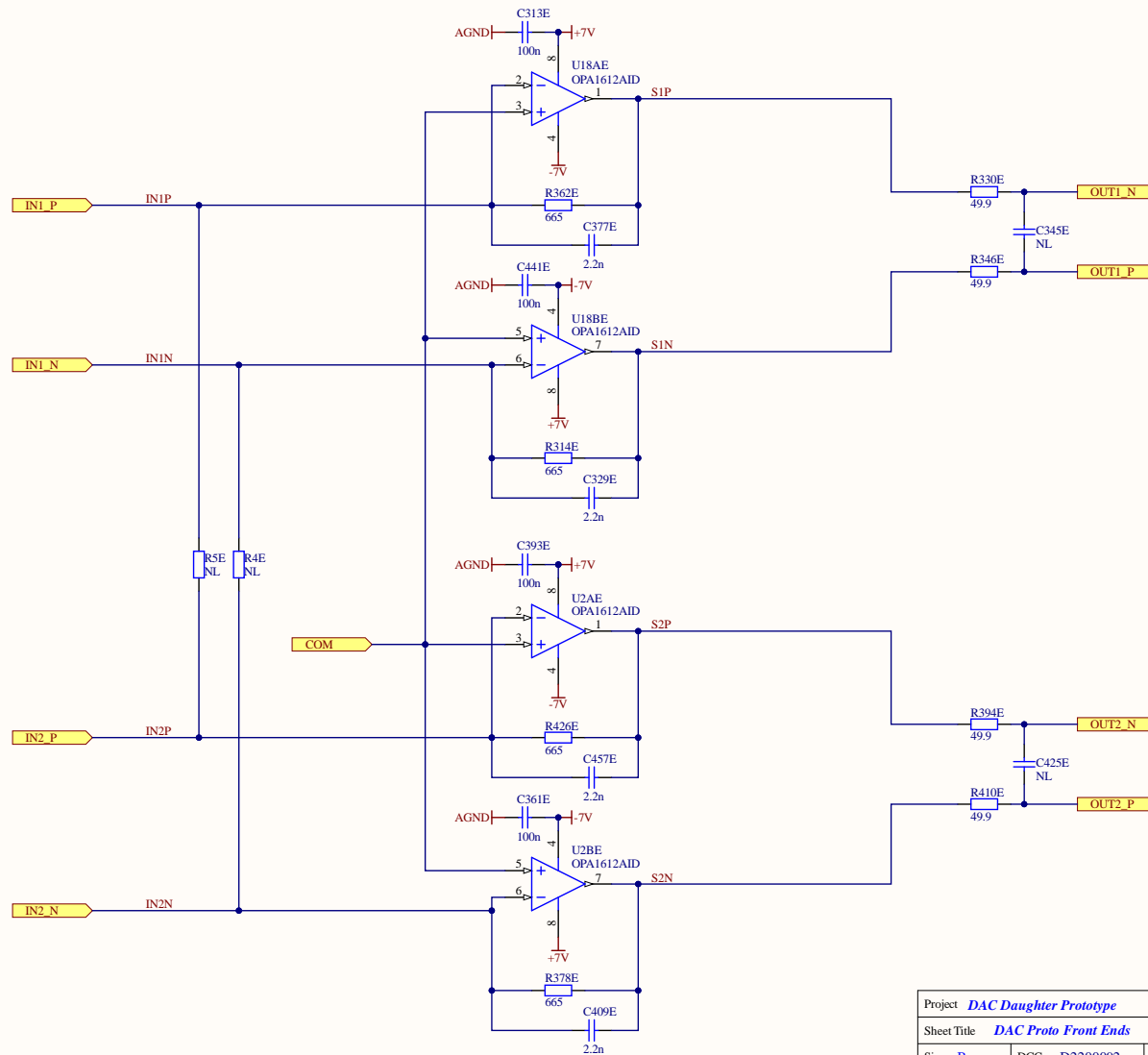





Parts Checked for Value and Consistency

Project DAC Daughter Prototype		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
Sheet Title DAC Proto Front Ends			
Size: B	DCC D22000092	Rev: 2	
Date: 11/1/2022	Time: 1:23:23 PM	Sheet: 11 of 19	Drawn By: M. Pirello
File: LD32_FrontEnd.SchDoc			

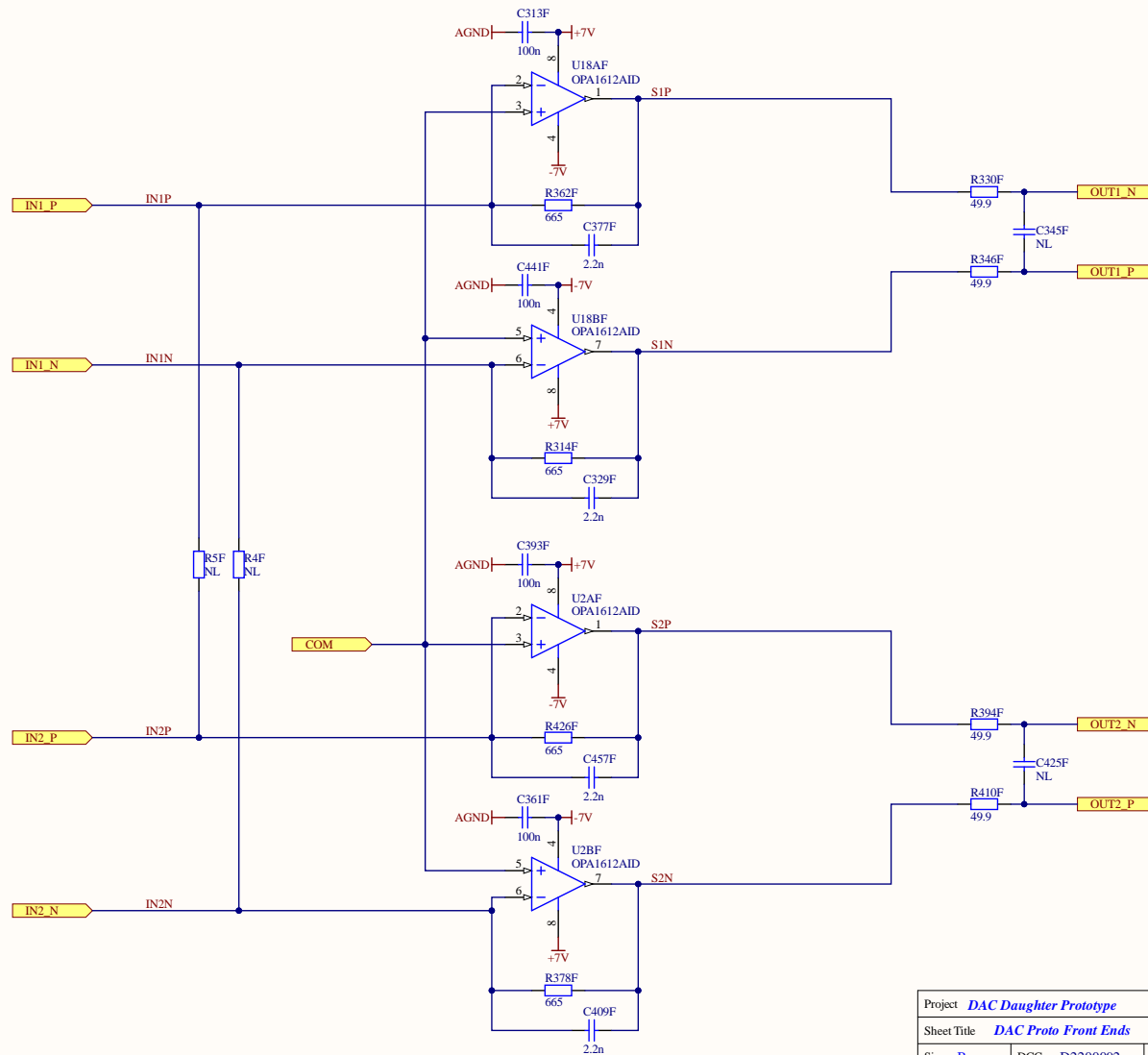





Parts Checked For Value and Consistency

Project <i>DAC Daughter Prototype</i>			<i>LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation</i>	
Sheet Title <i>DAC Proto Front Ends</i>				
Size: B	DCC D22000092	Rev: 2		
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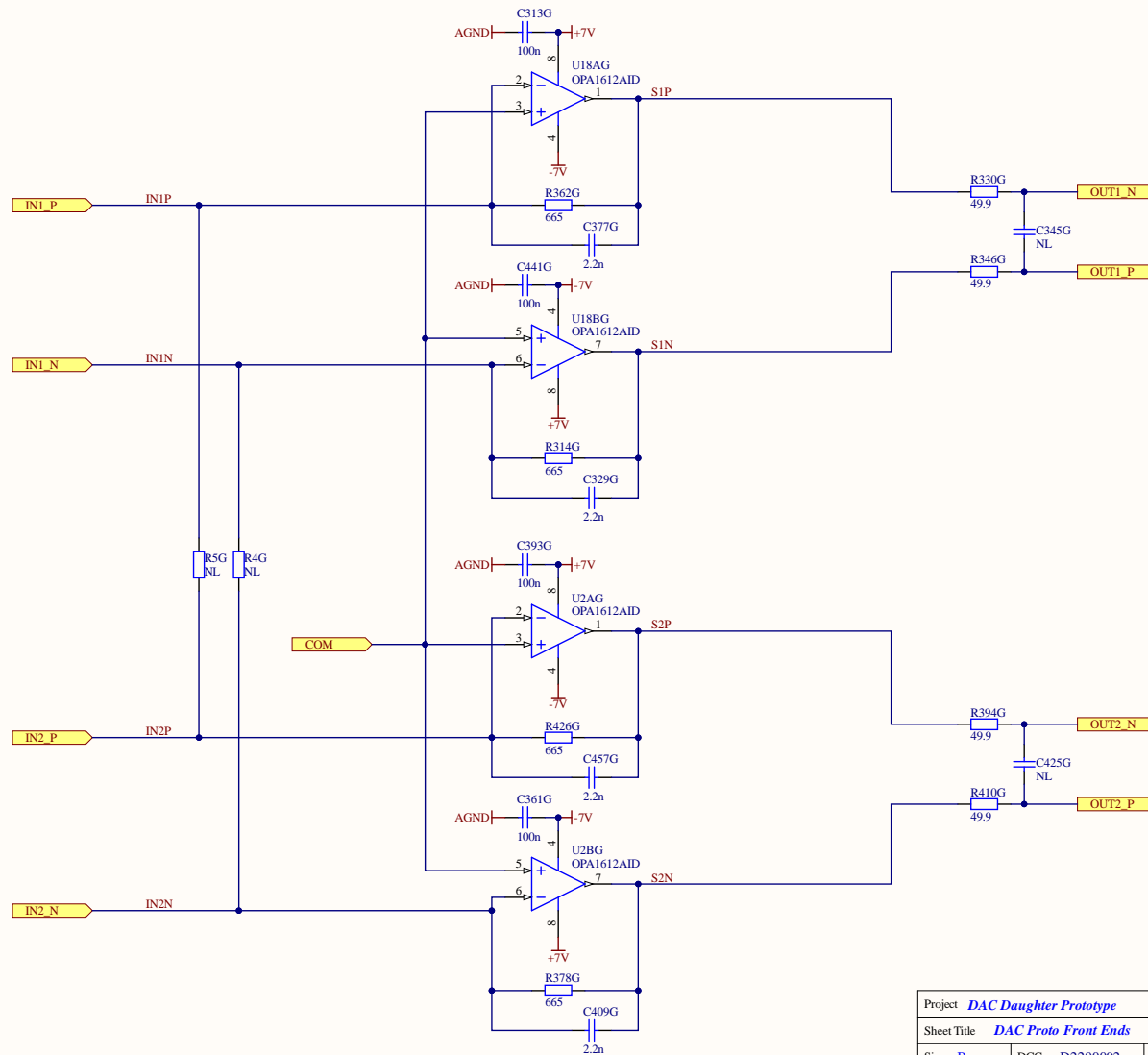





Parts Checked For Value and Consistency

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Sheet Title <i>DAC Proto Front Ends</i>				
Size: B	DCC D22000092	Rev: 2		
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File: LD32_FrontEnd.SchDoc			DrawnBy: <i>M. Pirello</i>	

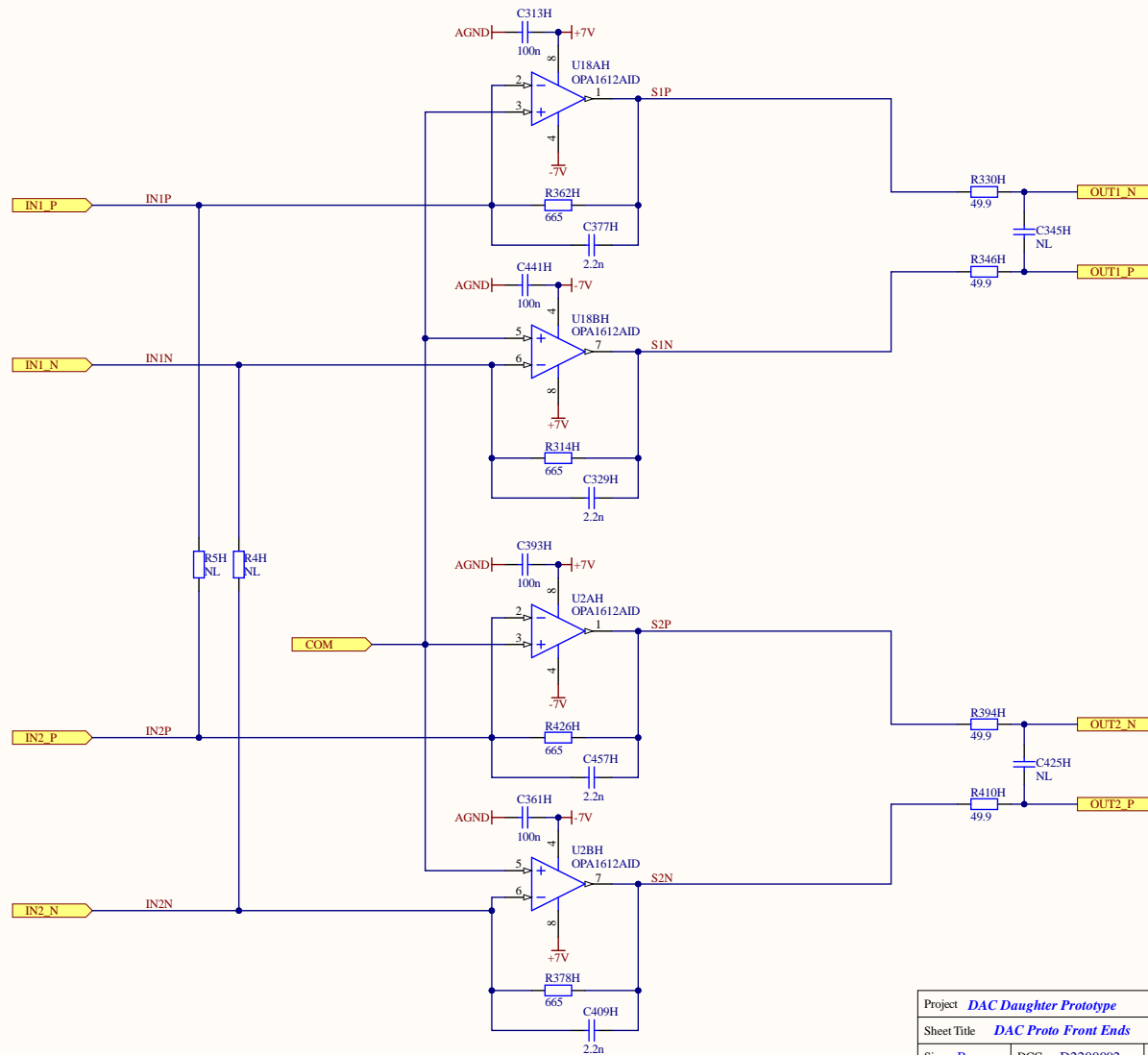




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Project <i>DAC Daughter Prototype</i>			<i>LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation</i>	
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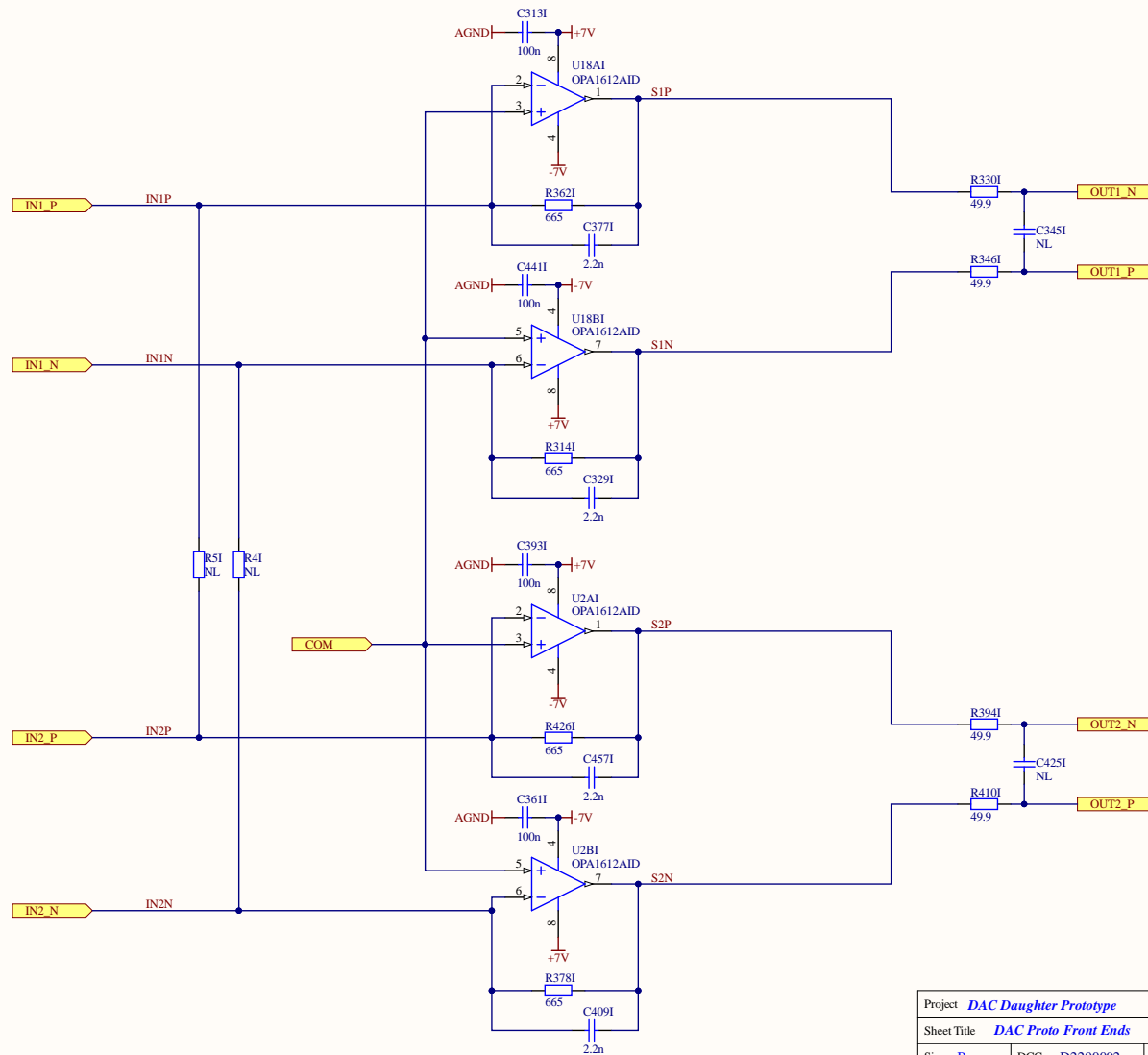




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Project DAC Daughter Prototype		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
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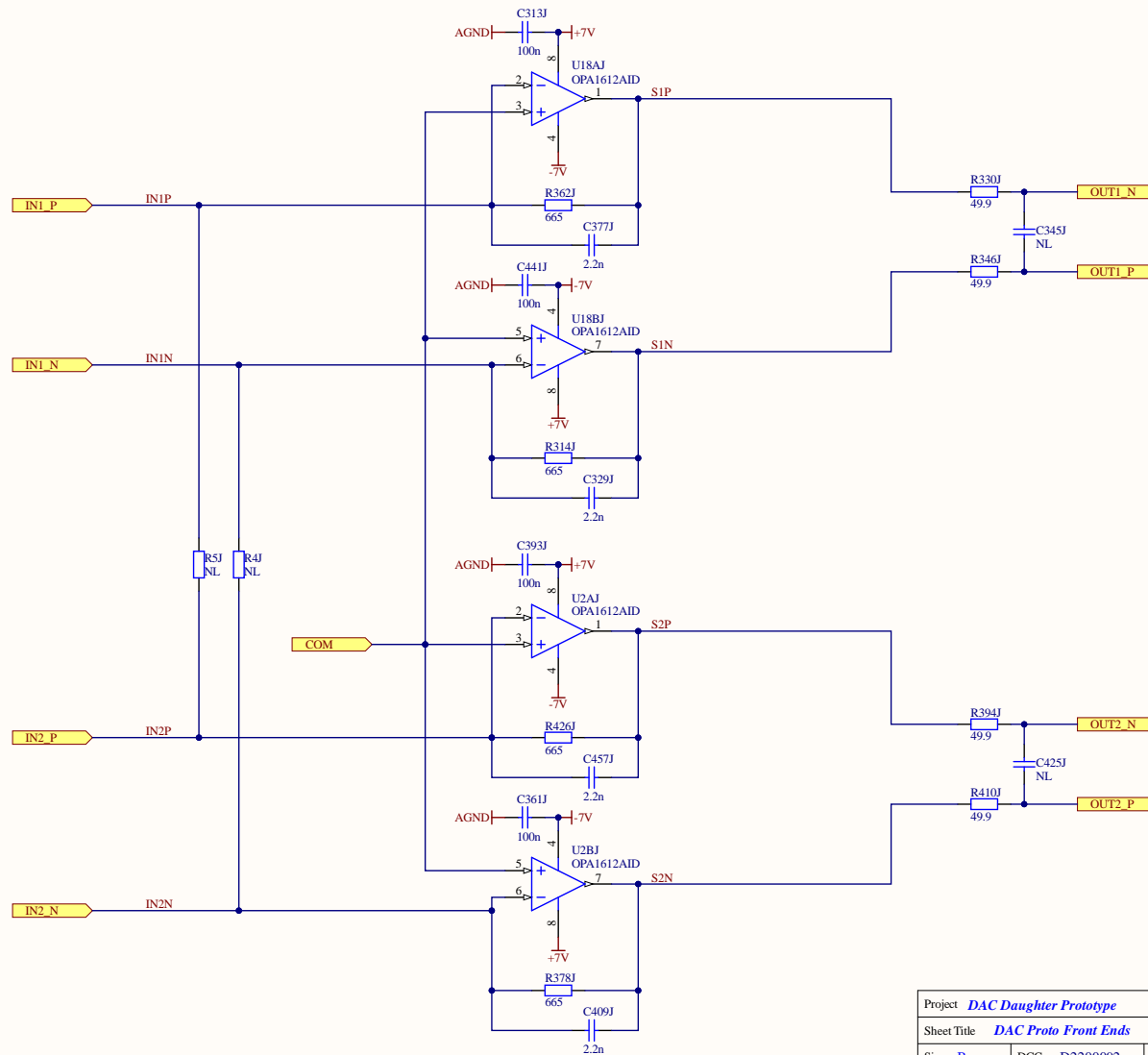




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Project DAC Daughter Prototype		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
Sheet Title DAC Proto Front Ends			
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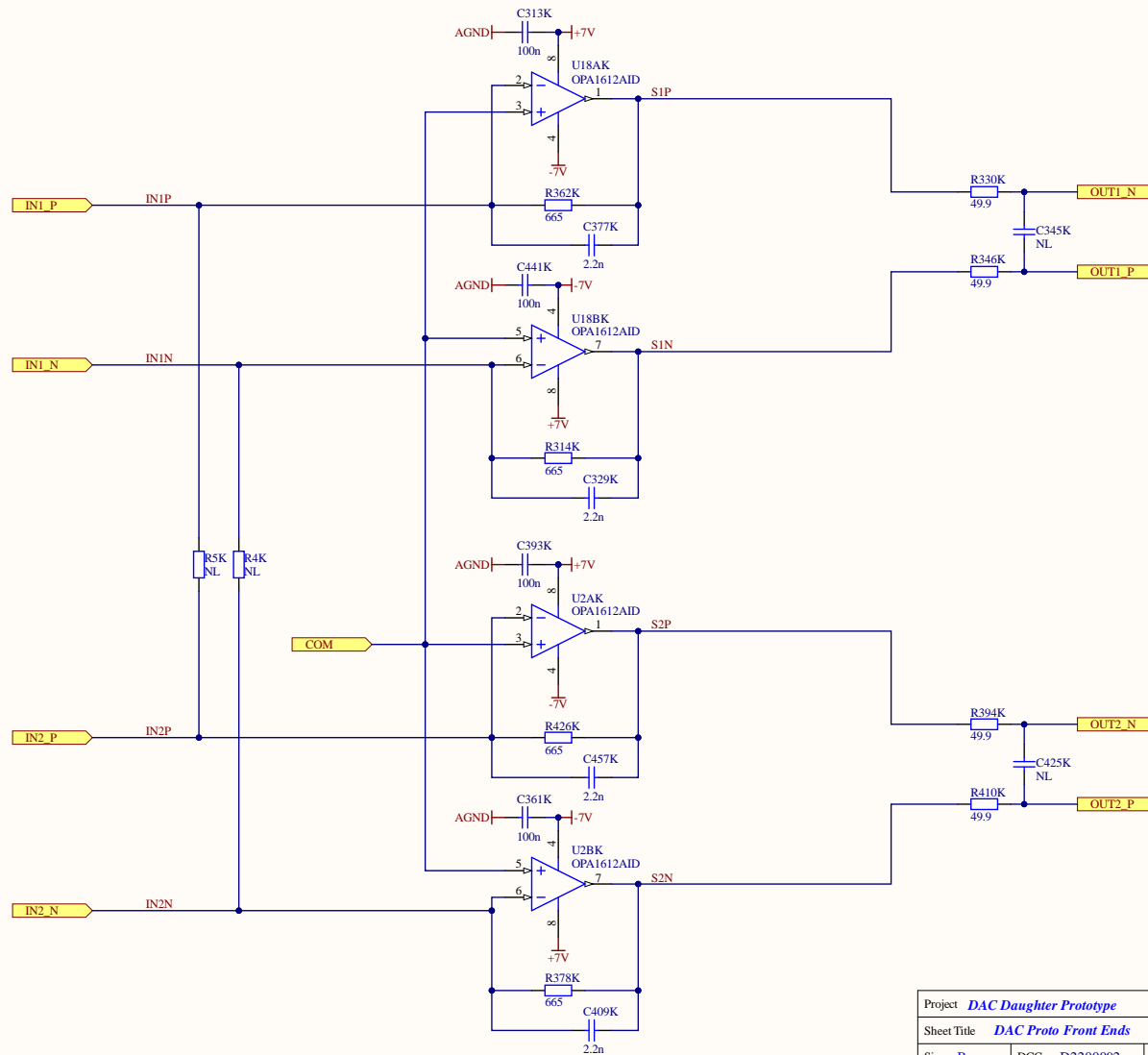




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Project DAC Daughter Prototype		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	
Sheet Title DAC Proto Front Ends			
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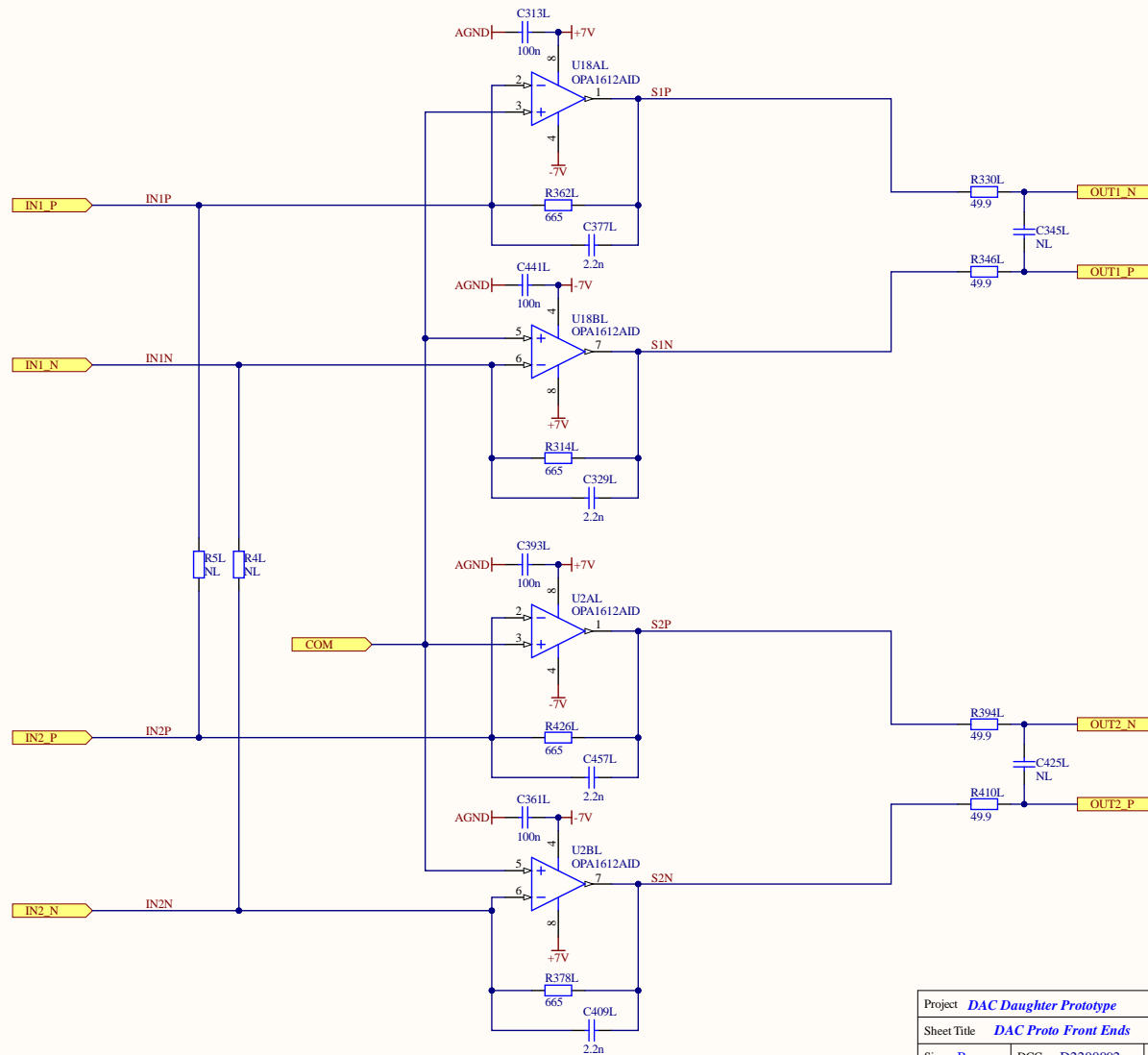





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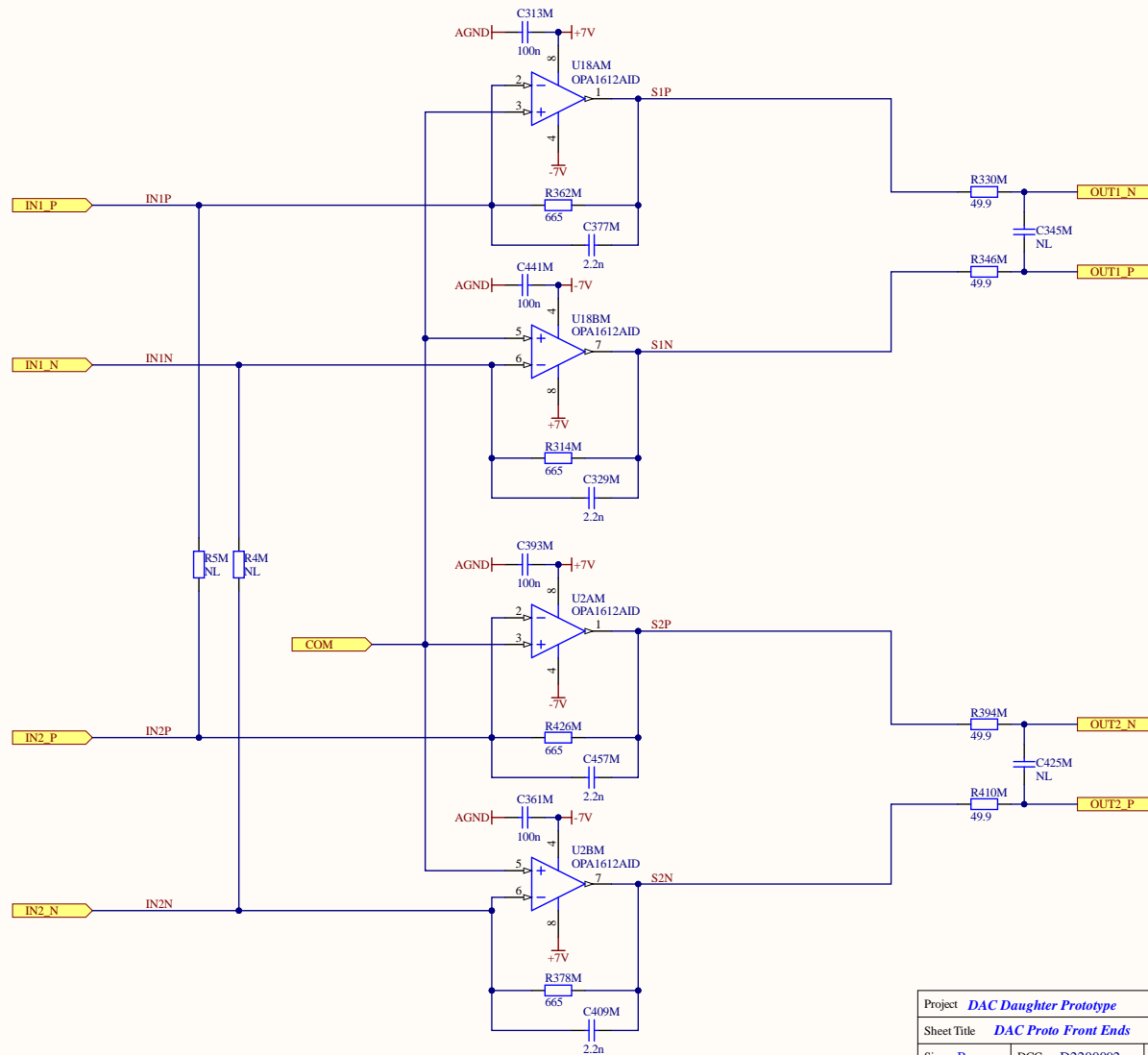
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Sheet Title <i>DAC Proto Front Ends</i>			
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:26 PM	Sheet: 11 of 19	
File: LD32_FrontEnd_SchDoc			<i>DrawnBy: M. Pirello</i>






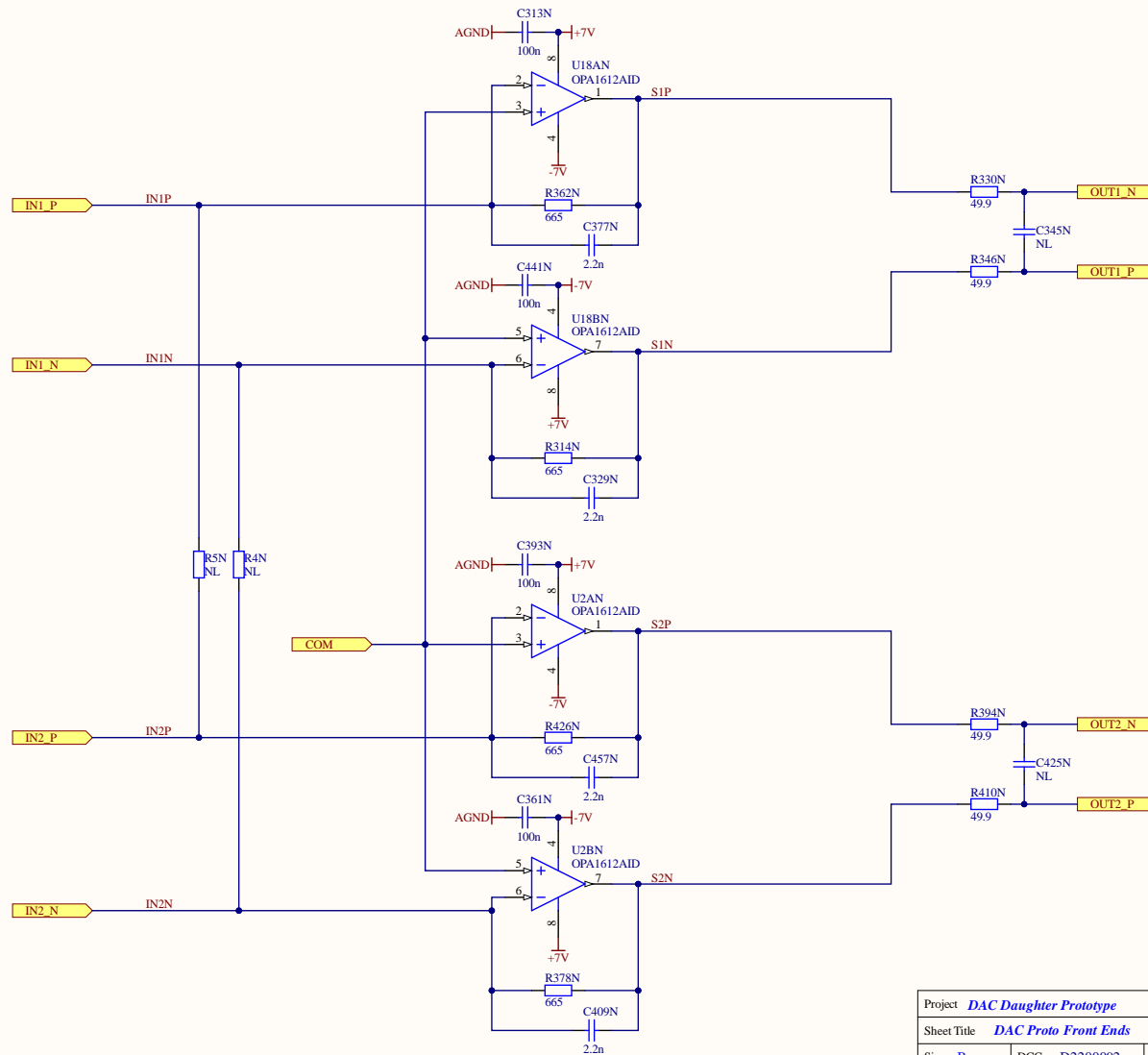
Parts Checked For Value and Consistency

Project <i>DAC Daughter Prototype</i>			<i>LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation</i>	
Sheet Title <i>DAC Proto Front Ends</i>				
Size: B	DCC D22000092	Rev: 2		
Date: <i>11/1/2022</i>	Time: <i>1:23:26 PM</i>	Sheet: <i>11 of 19</i>		
File: <i>LD32_FrontEnd.SchDoc</i>			<i>DrawnBy: M. Pirello</i>	




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Sheet Title <i>DAC Proto Front Ends</i>				
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File: LD32_FrontEnd.SchDoc			DrawnBy: <i>M. Pirello</i>	

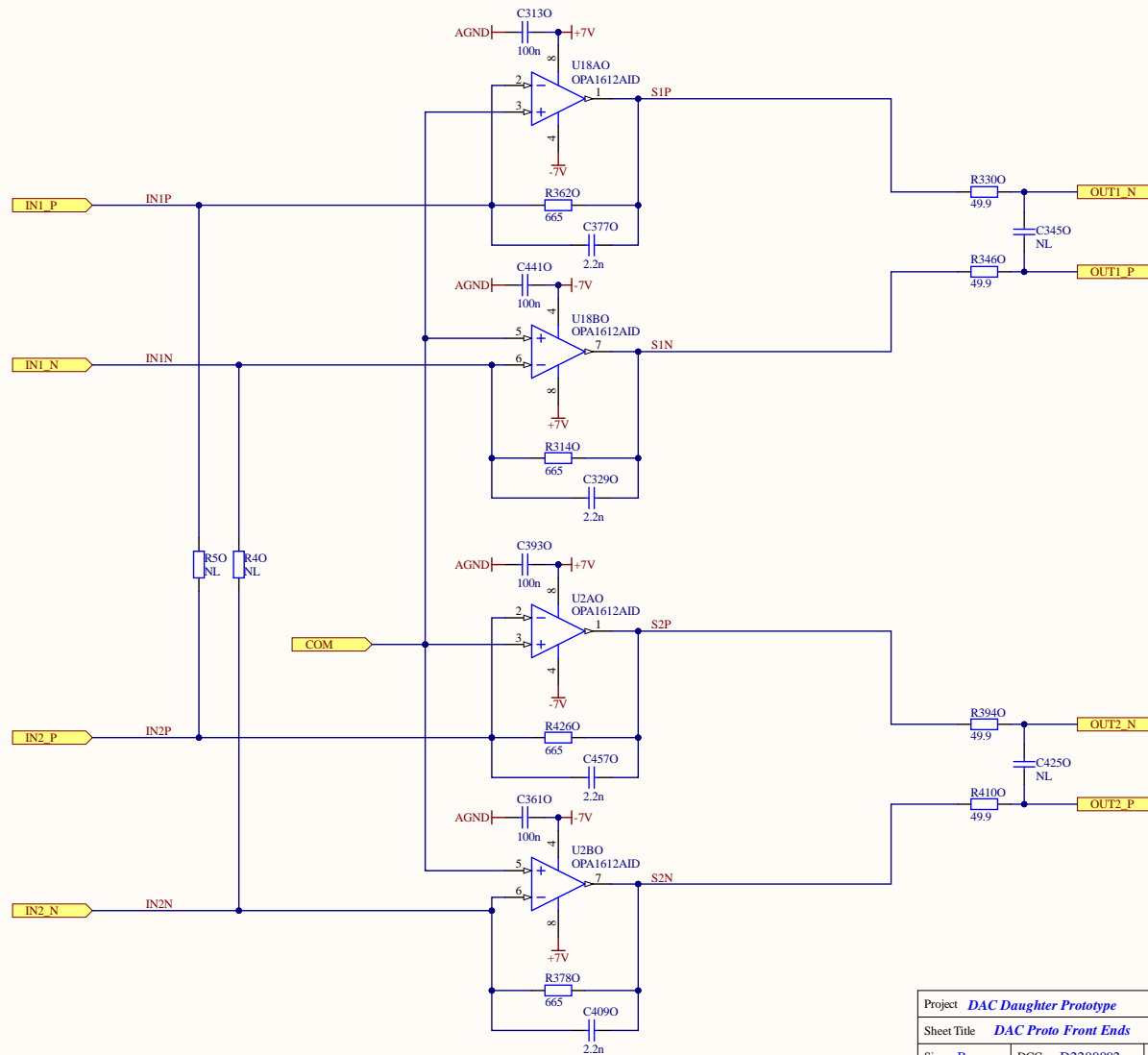





Parts Checked For Value and Consistency

Project <i>DAC Daughter Prototype</i>			<i>LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation</i>	
Sheet Title <i>DAC Proto Front Ends</i>				
Size: B	DCC D22000092	Rev: 2		
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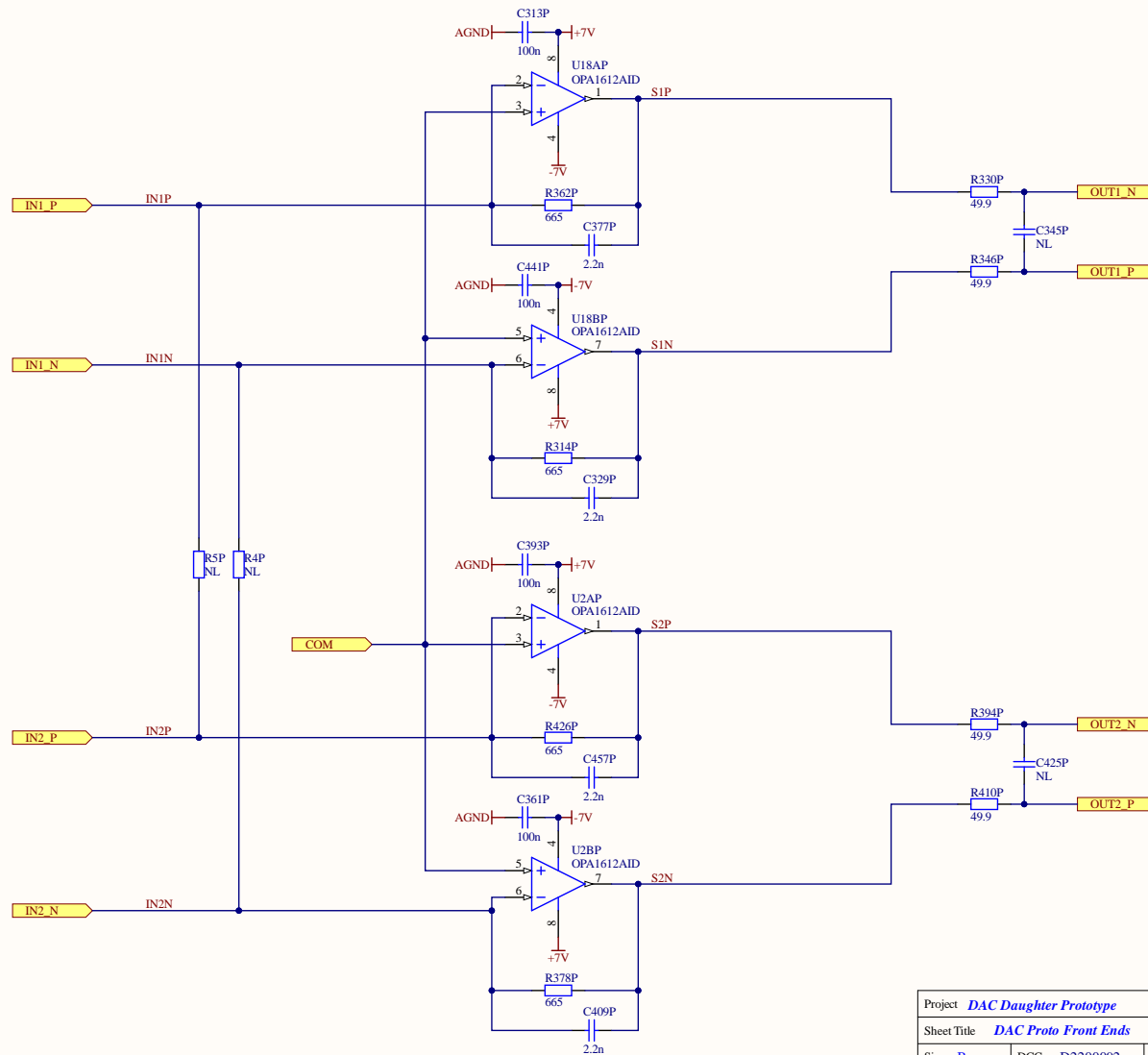




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Project <i>DAC Daughter Prototype</i>			<i>LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation</i>	
Sheet Title <i>DAC Proto Front Ends</i>				
Size: B	DCC D22000092	Rev: 2		
Date: <i>11/1/2022</i>	Time: <i>1:23:28 PM</i>	Sheet: <i>11 of 19</i>		
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Project <i>DAC Daughter Prototype</i>			<i>LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation</i>
Sheet Title <i>DAC Proto Front Ends</i>			
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