Diff Outputs to IFO

517-P50E-080P1-RR1EA

P1

OutputN1	80	79	OutputP1
OutputN3	78	77	OutputP3
OutputN5	76	75	OutputP5
OutputN7	74	73	OutputP7
OutputN6	72	71	OutputP6
OutputN8	70	69	OutputP8
OutputN2	68	67	OutputP2
OutputN4	66	65	OutputP4
	64	63	
OutputN9	62	61	OutputP9
OutputN11	60	59	OutputP11
OutputN13	58	57	OutputP13
OutputN15	56	55	OutputP15
OutputN14	54	53	OutputP14
OutputN16	52	51	OutputP16
OutputN10	50	49	OutputP10
OutputN12	48	47	OutputP12
	46	45	
OutputN17	44	43	OutputP17
OutputN19	42	41	OutputP19
OutputN21	40	39	OutputP21
OutputN23	38	37	OutputP23
OutputN22	36	35	OutputP22
OutputN24	34	33	OutputP24
OutputN18	32	31	OutputP18
OutputN20	30	29	OutputP20
	28	27	
OutputN25	26	25	OutputP25
OutputN27	24	23	OutputP27
OutputN29	22	21	OutputP29
OutputN31	20	19	OutputP31
OutputN30	18	17	OutputP30
OutputN32	16	15	OutputP32
OutputN26	14	13	OutputP26
OutputN28	12	11	OutputP28
	10	9	
CLK_O_N	8	7	CLK_O_P
	6	5	
CLK_E_N	4	3	CLK_E_P
TRG_N	2	1	TRG_P

81 82

P50E-080P1-RR1EA

AGND

GND

OutputP1 A1_P
OutputN1 A1_N
OutputP2 A2_P
OutputN2 A2_N
OutputP3 A3_P
OutputN3 A3_N
OutputP4 A4_P
OutputN4 A4_N
OutputP5 A5_P
OutputN5 A5_N
OutputP6 A6_P
OutputN6 A6_N
OutputP7 A7_P
OutputN7 A7_N
OutputP8 A8_P
OutputN8 A8_N
OutputP9 A8_N

ANALOG1

OutputN9 A1_P
OutputP10 A1_N
OutputN10 A2_P
OutputP11 A2_N
OutputN11 A3_P
OutputP12 A3_N
OutputN12 A4_P
OutputP13 A4_N
OutputN13 A5_P
OutputP14 A5_N
OutputN14 A6_P
OutputP15 A6_N
OutputN15 A7_P
OutputP16 A7_N
OutputN16 A8_P
OutputP17 A8_N

ANALOG2

OutputN17 A1_P
OutputP18 A1_N
OutputN18 A2_P
OutputP19 A2_N
OutputN19 A3_P
OutputP20 A3_N
OutputN20 A4_P
OutputP21 A4_N
OutputN21 A5_P
OutputP22 A5_N
OutputN22 A6_P
OutputP23 A6_N
OutputN23 A7_P
OutputP24 A7_N
OutputN24 A8_P
OutputP25 A8_N

ANALOG3

OutputN25 A1_P
OutputP26 A1_N
OutputN26 A2_P
OutputP27 A2_N
OutputN27 A3_P
OutputP28 A3_N
OutputN28 A4_P
OutputP29 A4_N
OutputN29 A5_P
OutputP30 A5_N
OutputN30 A6_P
OutputP31 A6_N
OutputN31 A7_P
OutputP32 A7_N
OutputN32 A8_P
A8_N

ANALOG4

CLKO_P CLK_O_P
CLKO_N CLK_O_N
CLKE_P CLK_E_P
CLKE_N CLK_E_N
TRIG_P TRIGout_P
TRIG_N TRIGout_N

EXT

DACS

Analog

LD32_Analog.SchDoc

ANALOG1 Analog1 DAC1 DAC1
ANALOG2 Analog2 DAC2 DAC2
ANALOG3 Analog3 DAC3 DAC3
ANALOG4 Analog4 DAC4 DAC4

POWER

Power Supplies

LD32_Power.SchDoc

POWER POWER
SENSE SENSE
PG PG
APWR1 APWR1
APWR2 APWR2

FPGA

FPGA

LD32_FPGA.SchDoc

DAC1 DAC1
DAC2 DAC2
DAC3 DAC3
DAC4 DAC4
PG
PCIE PCIE
SW[8..1] SW[8..1]
POWER POWER
APWR1 APWR1
APWR2 APWR2
CLOCK
SENSE SENSE
EXT EXT

Input Clock Buffers

VCC GND

R293 1.6K R292 NL

CLK_O_P C58 100n

CLK_O_N C57 100n

R294 49.9 49.9 R295

R290 2.32K

R296 22K C277 10nF

R78 NL GND C60 100n

U41 NC VDD VCC A Y B Z VBB GND SN65LVDS100D

CLKO_P CLKO_N GND

R77 NL

R76 NL R289 NL GND C61 100n

U40 NC VDD VCC A Y B Z VBB GND SN65LVDS100D

R291 2.67K R72 100 R288 1.6K

CLK_E_P CLK_E_N

CLKE_P CLKE_N GND

R75 NL

R73 NL C275 100n

U42 VDD NC Y A Z B GND VBB SN65LVDS100D

R297 NL R71 NL R298 NL

TRG_N TRG_P

TRIG_N TRIG_P

R83 100

R74 NL

VCO Phase

LD32_PHASE.SchDoc

CLOCK CLOCK

Designator

LD32_PCIE_HL.schdoc

SENSE SENSE
PCIE PCIE

Config Switches

SW[8..1]

S1

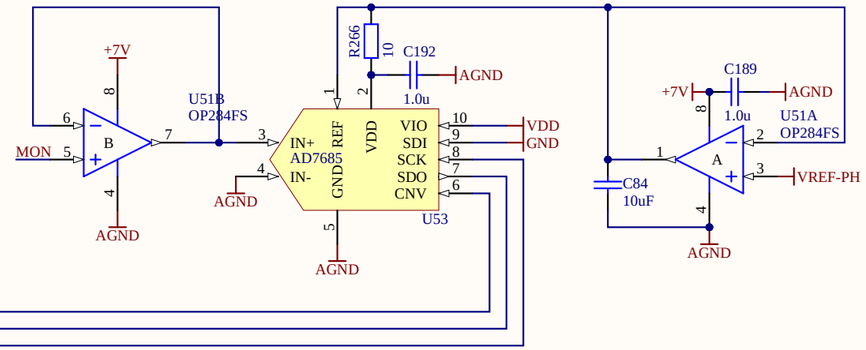
SW1 16 1
SW2 15 2
SW3 14 3
SW4 13 4
SW5 12 5
SW6 11 6
SW7 10 7
SW8 9 8 GND

SW DIP-8

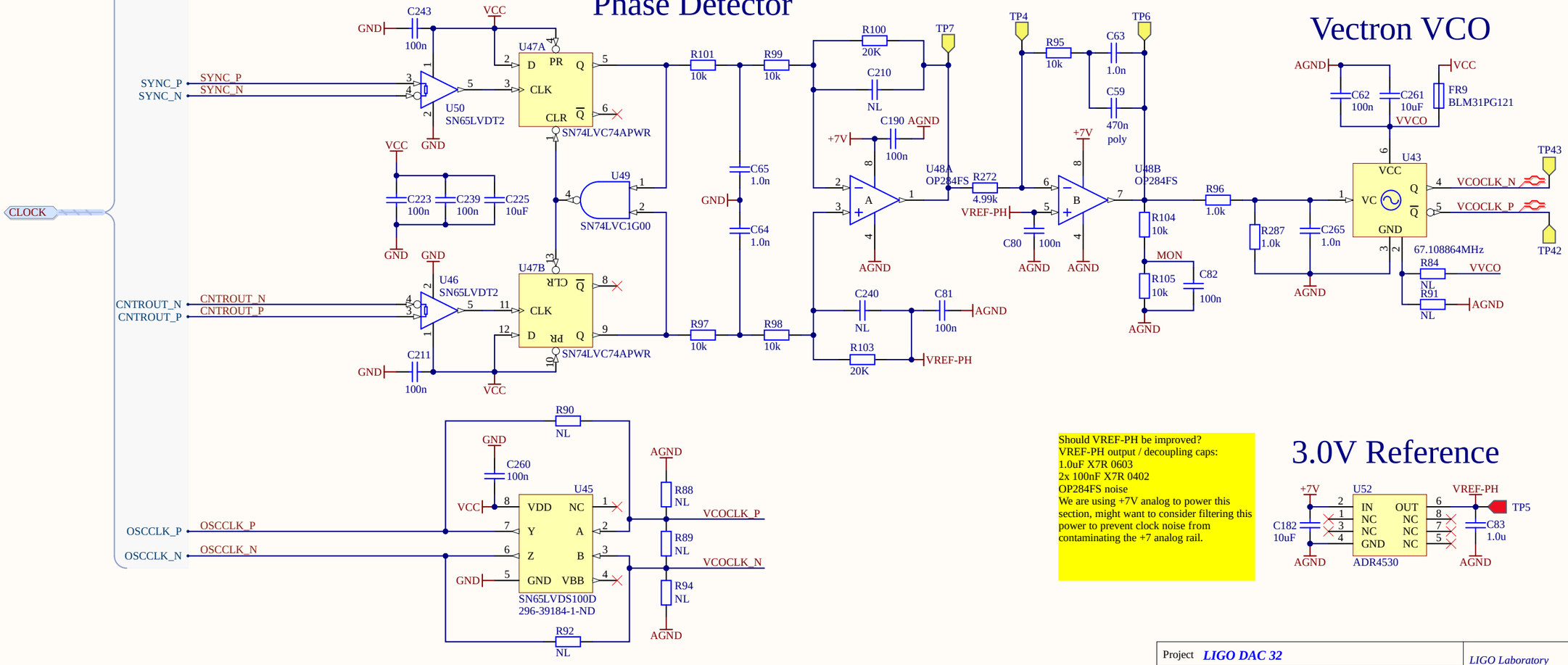
CKN6128CT-ND

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC Proto Top Sheet*		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024 Time: 1:46:36 PM		Sheet: 1 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_TOP.SchDoc			

Control Voltage Monitor



Phase Detector



Vectron VCO

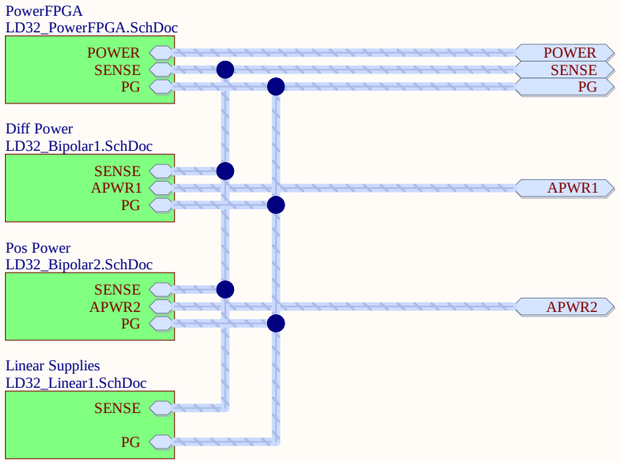
Should VREF-PH be improved?
VREF-PH output / decoupling caps:
1.0uF X7R 0603
2x 100nF X7R 0402
OP284FS noise
We are using +7V analog to power this section, might want to consider filtering this power to prevent clock noise from contaminating the +7 analog rail.

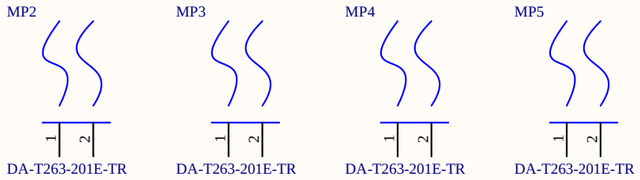
3.0V Reference

Optional LVPECL-LVDS Translator

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*VCO & Phase Detector*		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024 Time: 1:46:37 PM		Sheet: 2 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_PHASE.SchDoc			

Power Top Sheet





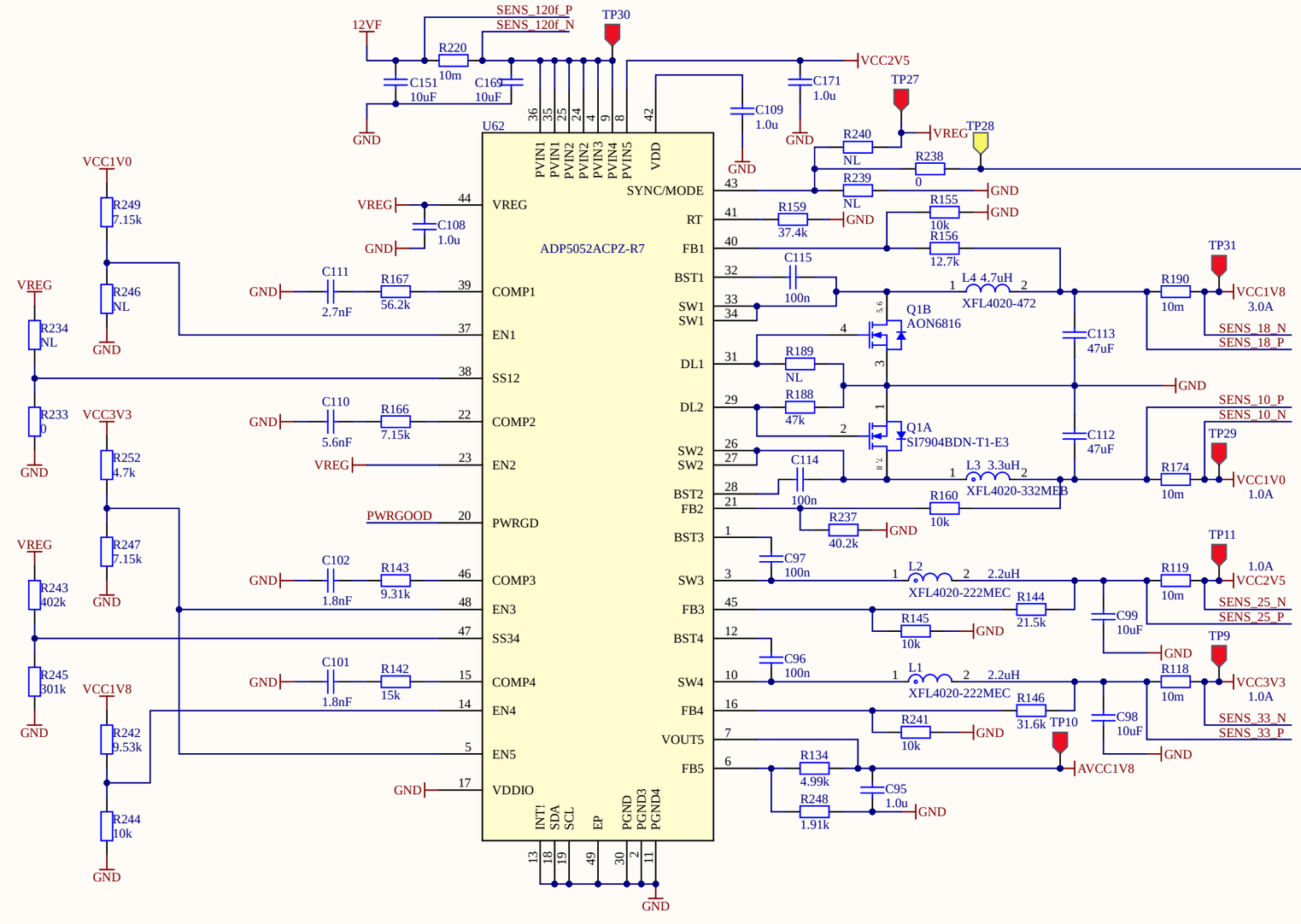
Project	***LIGO DAC 32***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***Power Top***		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024 Time: 1:46:37 PM		Sheet: 3 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Power.SchDoc			

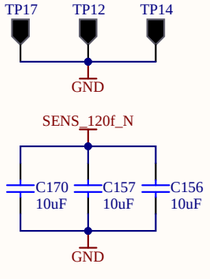
Switched FPGA Power

ADP505x Configs
FB1 - 1.8V 12.7k, 10k, 4.7uH
FB2 - 1.0V 10k. 40k, 3.3uH
FB3 - 2.5V 21.5k, 10k, 2.2uH
FB4 - 3.3V 31.6k, 10k, 2.2uH
FB5 - 1.8V 5k, 1.91k

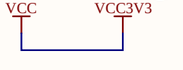
Legend
VCC = 3.3V (digital votlage)
VDD = 1.8V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Power Up Config
1st - VCC1V0
2nd - VCC1V8
3rd - VCC3V3
4th & 5th VCC2V5 & AVCC1V8

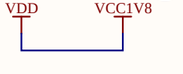


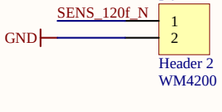


VCC Bridge



VDD Bridge





POWER
PWRSYNC → PWRSYNC → POWER

SENSE
SENS_33_P → SENS_33_P
SENS_33_N → SENS_33_N
SENS_25_P → SENS_25_P
SENS_25_N → SENS_25_N
SENS_18_P → SENS_18_P
SENS_18_N → SENS_18_N
SENS_10_P → SENS_10_P
SENS_10_N → SENS_10_N
SENS_120x_P → SENS_120x_P
SENS_120x_N → SENS_120x_N
SENS_120b_P → SENS_120b_P
SENS_120b_N → SENS_120b_N
SENS_VCCA3.3V → SENS_VCCA3.3V
SENS_AVCC3.3V → SENS_AVCC3.3V
SENS_DVDD1.2V → SENS_DVDD1.2V
SENS_AVCC → SENS_AVCC
SENS_AVTT → SENS_AVTT
SENS_+7 → SENS_+7
SENS_-7 → SENS_-7
→ SENSE

POWER GOOD
PG_VCCAL3.3V → PG_VCCAL3.3V
PG_AVCCL3.3V → PG_AVCCL3.3V
PG_DVDDL1.2V → PG_DVDDL1.2V
PG_SW+2V → PG_SW+2V
PG_SW+4V → PG_SW+4V
PWRGOOD → PG_FPGA
PG_SW+8V → PG_SW+8
PG_SW-8V → PG_SW-8
PG-7 → PG_L-7v
PG+7 → PG_L+7v
→ PG

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*FPGA Supply*		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024 Time: 1:46:37 PM		Sheet: 4 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_PowerFPGA.SchDoc			

Front End Power +/- 8V

Low Noise +7V

Low Noise -7V

LT3045-1 Configs:
+7V:
Vset = Iset * Rset = 100uA * Rset
Rs = 70k
Vset = 70k *100uA = 7.0V
PGFB:
Vset = 7.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(7V/0.3V-1) = 4.47k < 4.7k

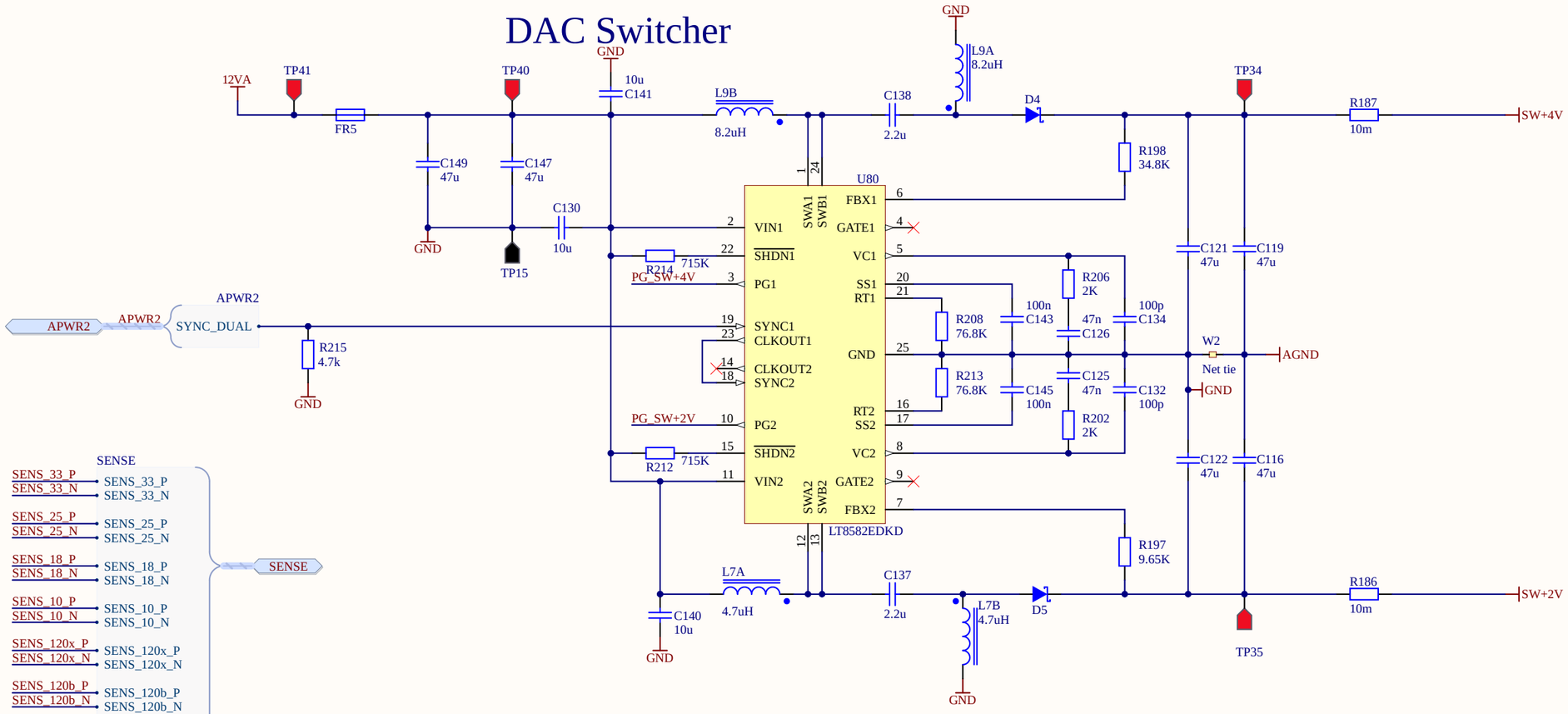
-7V:
Vset = Iset * Rset = 100uA * Rset
Rs = 70k
Vset = 70k *100uA = 7.0V
PGFB:
Vset = 7.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(7V/0.3V-1) = 4.47k < 4.7k

LT3045-1 Configs:
+7V:
Vset = Iset * Rset = 100uA * Rset
Rs = 70k
Vset = 70k *100uA = 7.0V
PGFB:
Vset = 7.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(7V/0.3V-1) = 4.47k < 4.7k

-7V:
Vset = Iset * Rset = 100uA * Rset
Rs = 70k
Vset = 70k *100uA = 7.0V
PGFB:
Vset = 7.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(7V/0.3V-1) = 4.47k < 4.7k

Project	*LIGO DAC 32*		*LIGO Laboratory*
Sheet Title	*Bipolar Analog Supply*		*California Institute of Technology*
Size: B	DCC D2200368	Rev: 1	*Massachusetts Institute of Technology*
Date: 2/8/2024	Time: 1:46:37 PM	Sheet: 5 of 17	*National Science Foundation*
File: LD32_Bipolar1.SchDoc			*DrawnBy: M. Pirello, D. Sigg*

DAC Switcher

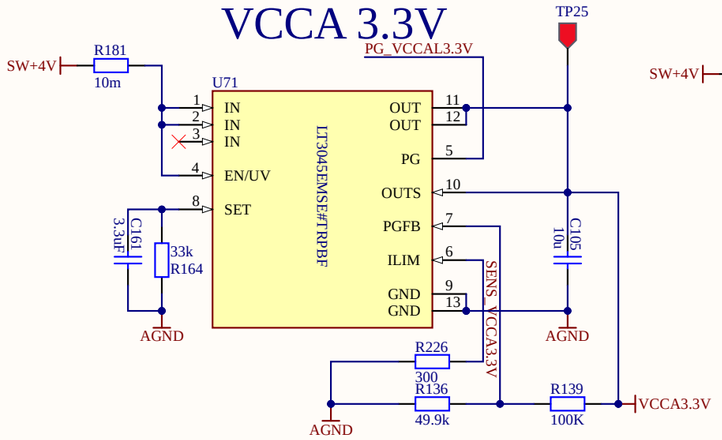


Front End Power +/- 7V
QC per channel 5.5mA * 64 = 352mA so single supplies are sufficient
DVDD 1.2V 128 * 4 = 512mA > 500mA so two supplies
VCCA 3.3V one supply
AVDD 1.8V one suppply
AVCC_R 3.3V 90*4 = 360mA one supply
AVCC_L 3.3V 90*4 = 360mA one supply
VDD_R, VDD_L 3.3V 128 per DAC * 4 = 512mA > 500mA is two supplies

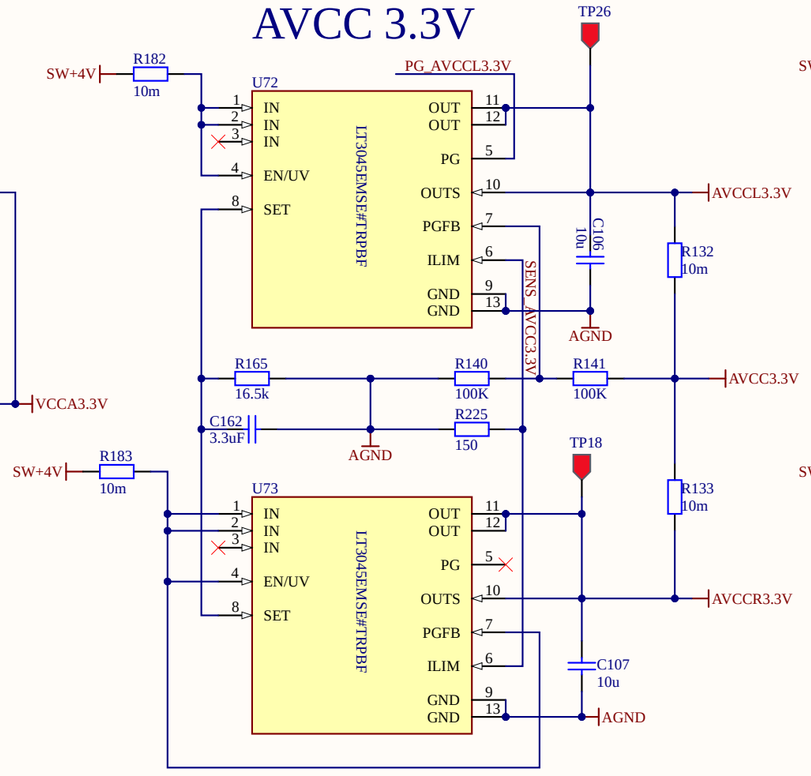
Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Dual Analog Supply*		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024	Time: 1:46:37 PM	Sheet: 6 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Bipolar2.SchDoc			

DAC Linear Power Supplies

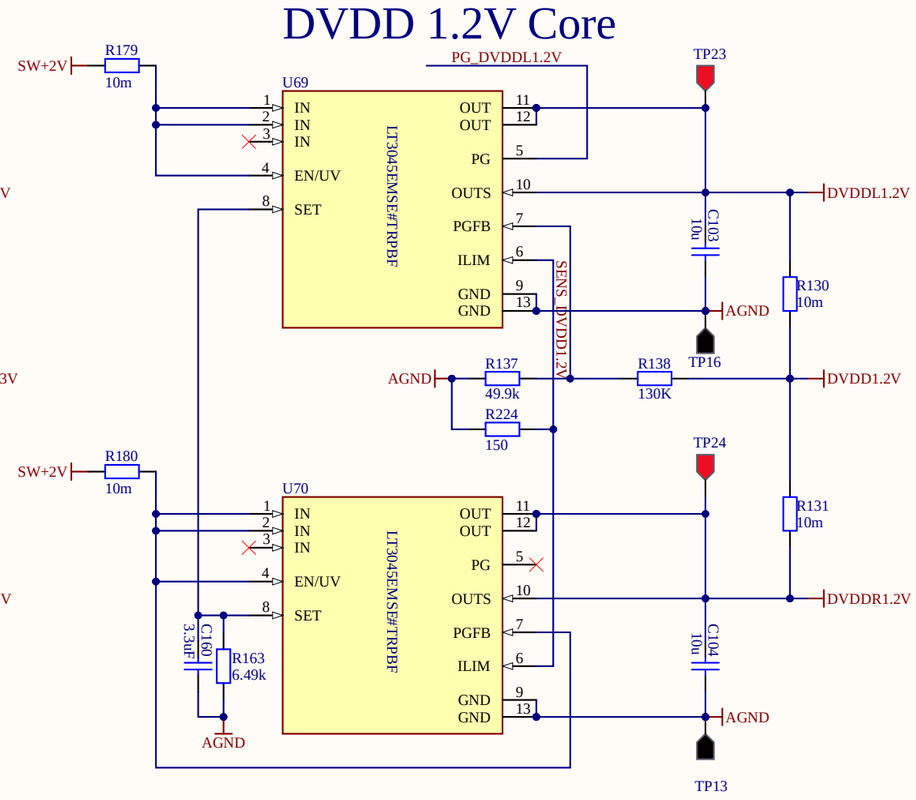
VCCA 3.3V



AVCC 3.3V



DVDD 1.2V Core



SENSE

- SENS_33_P → SENS_33_P
- SENS_33_N → SENS_33_N
- SENS_25_P → SENS_25_P
- SENS_25_N → SENS_25_N
- SENS_18_P → SENS_18_P
- SENS_18_N → SENS_18_N
- SENS_10_P → SENS_10_P
- SENS_10_N → SENS_10_N
- SENS_120x_P → SENS_120x_P
- SENS_120x_N → SENS_120x_N
- SENS_120b_P → SENS_120b_P
- SENS_120b_N → SENS_120b_N
- SENS_VCCA3.3V → SENS_VCCA3.3V
- SENS_AVCC3.3V → SENS_AVCC3.3V
- SENS_DVDD1.2V → SENS_DVDD1.2V
- SENS_AVCC → SENS_AVCC
- SENS_AVTT → SENS_AVTT
- SENS_+7 → SENS_+7
- SENS_-7 → SENS_-7

→ SENSE

LT3045-1 Configs:
VCCA3V3
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k *100uA = 3.3V
PGFB:
Vset = 3.3V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

AVCC3V3:
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k *100uA = 3.3V
PGFB:
Vset = 3.3V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

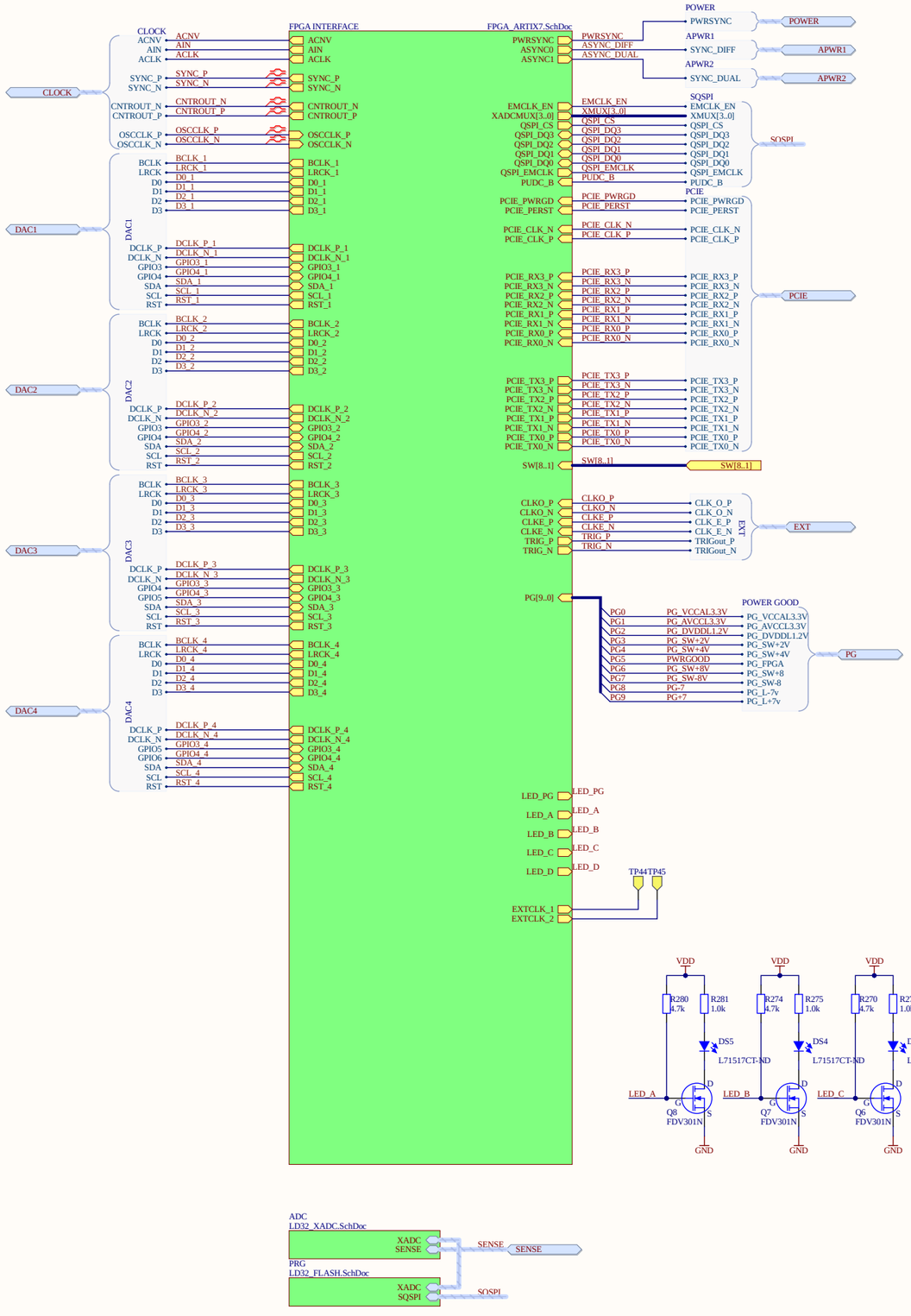
LT3045-1 Configs:
DVDD1V2:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k

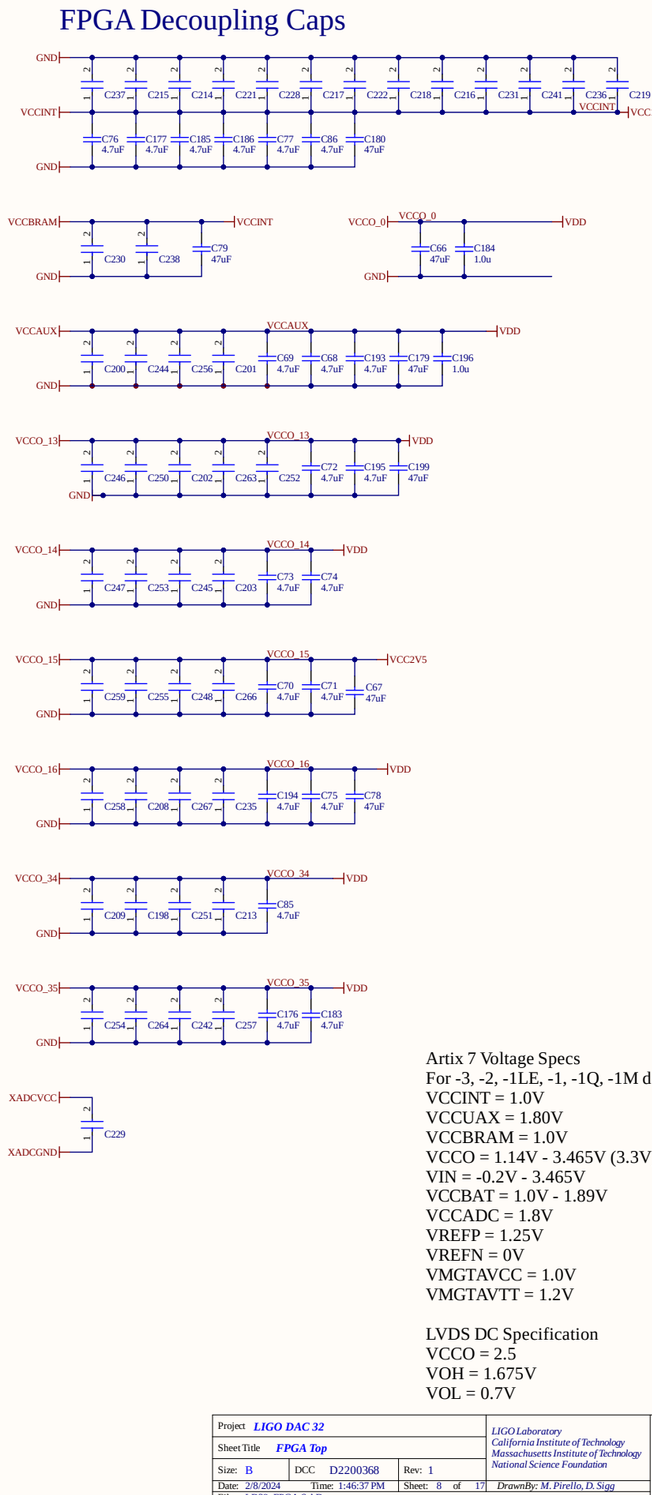
POWER GOOD

- PG_VCCAL3.3V → PG_VCCAL3.3V
- PG_AVCCL3.3V → PG_AVCCL3.3V
- PG_DVDDL1.2V → PG_DVDDL1.2V
- PG_SW+2V → PG_SW+2V
- PG_SW+4V → PG_SW+4V
- PWRGOOD → PG_FPGA
- PG_SW+8V → PG_SW+8
- PG_SW-8V → PG_SW-8
- PG-7 → PG_L-7v
- PG+7 → PG_L+7v

→ PG

Project	*LIGO DAC 32*		*LIGO Laboratory*
Sheet Title	*Linear Supplies*		*California Institute of Technology*
Size: B	DCC D2200368	Rev: 1	*Massachusetts Institute of Technology*
Date: 2/8/2024	Time: 1:46:37 PM	Sheet: 7 of 17	*National Science Foundation*
File: LD32_Linear1.SchDoc		*DrawnBy: M. Pirello, D. Sigg*	





Artix 7 Voltage Specs
For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V

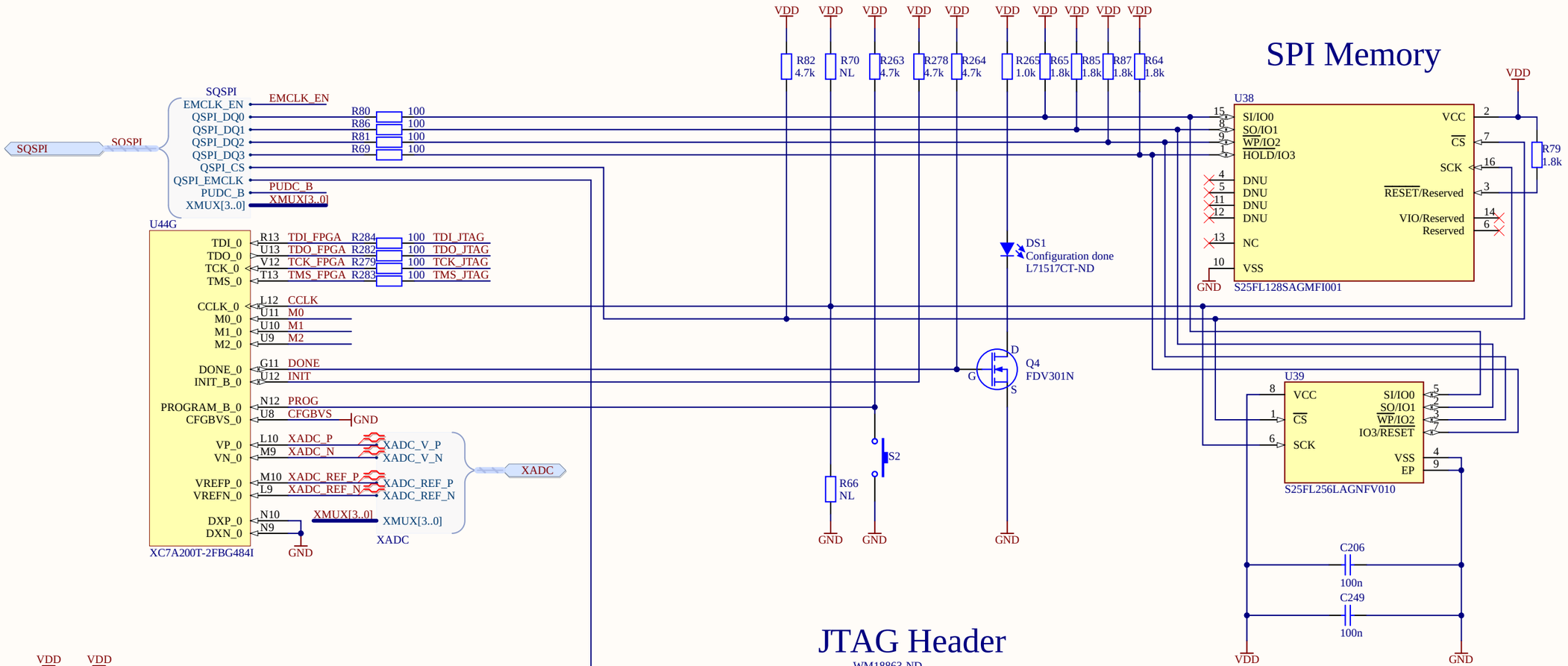
LVDS DC Specification
VCCO = 2.5
VOH = 1.675V
VOL = 0.7V

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*FPGA Top*		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024	Time: 1:46:37 PM	Sheet: 8 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FPGA.SchDoc			

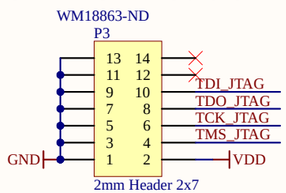
JTAG and SPI Flash

VDD is 1.8V for this design

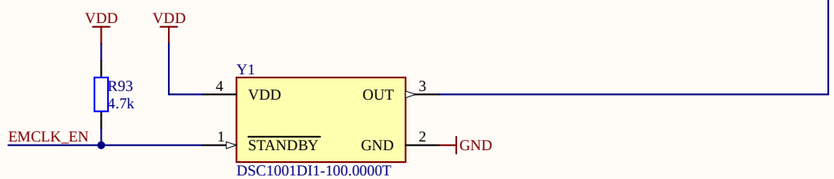
SPI Memory

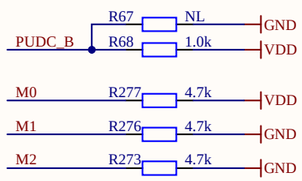


JTAG Header



100 MHz Program Clock





Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*JTAG & SPI Flash*		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024	Time: 1:46:37 PM	Sheet: 9 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FLASH.SchDoc			

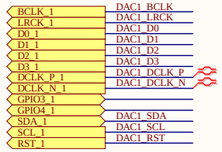
INA210 configuration
VCC = VCC2 = 3.3V
Vout = (I x 10mohm) * 200
I = Vout / (200 * 10mohm)

12.5mOhm sense R
2A range
Gain 200 V/V

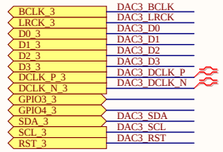
10mOhm sense R
1A max
Sensing gain 1Ohm

Project	*LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*	
Sheet Title	*XADC*				
Size: B	DCC D2200368		Rev: 1		
Date: 2/8/2024	Time: 1:46:38 PM		Sheet: 10 of 17	*DrawnBy: M. Pirello, D. Sigg*	
File: LD32_XADC.SchDoc					

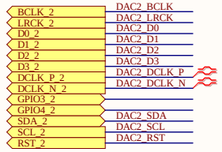
DAC 1



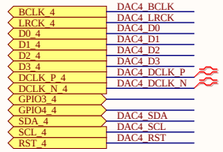
DAC3



DAC2



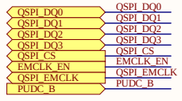
DAC4



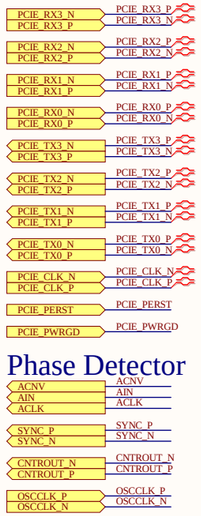
FPGA xADC

FPGA Config

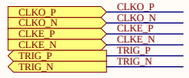
FPGA Flash

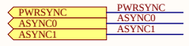


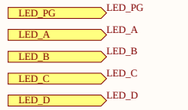
PCIe Connector



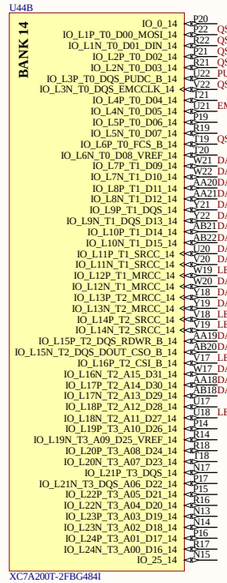
Phase Detector

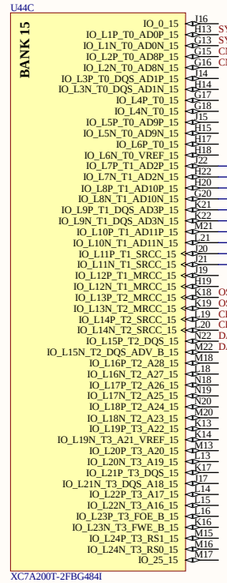


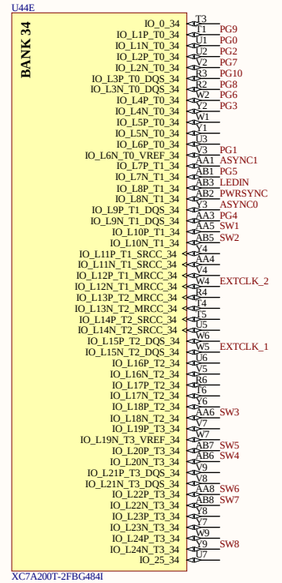


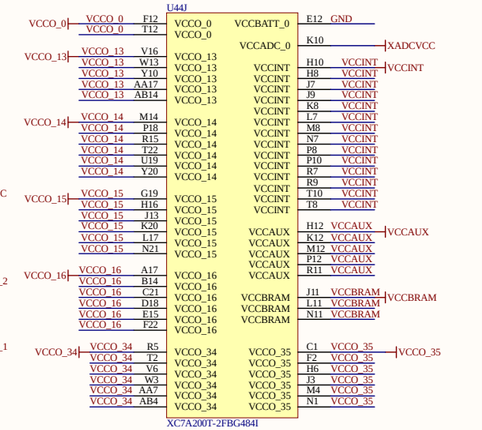


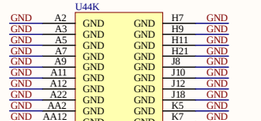
Optional External Clock

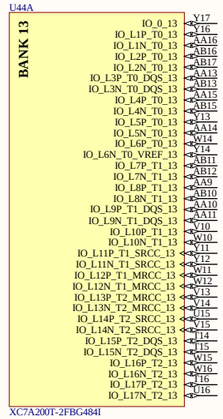


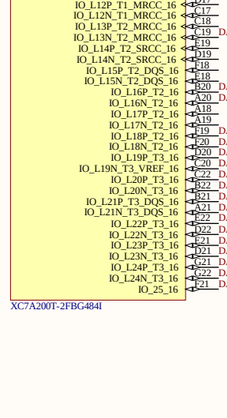


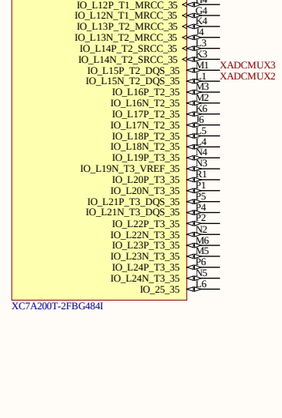


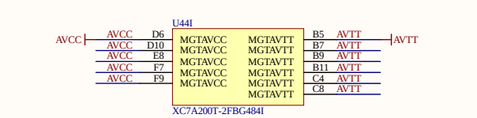


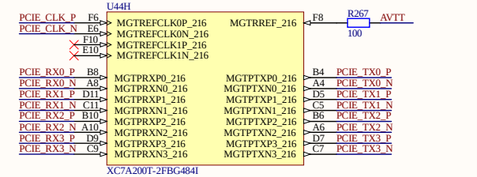






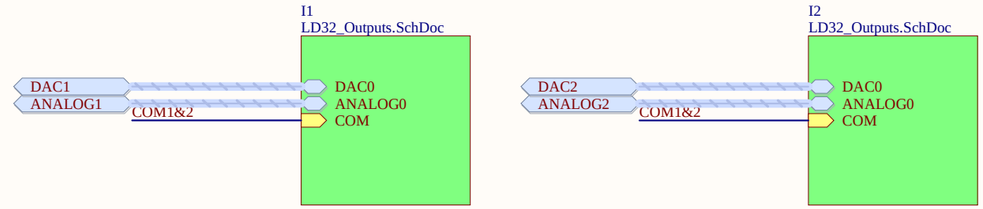


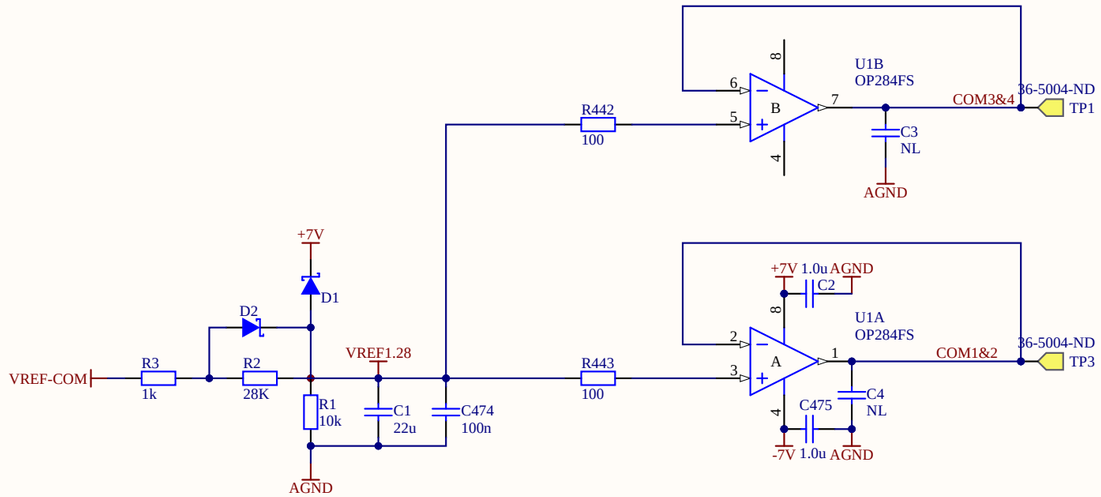


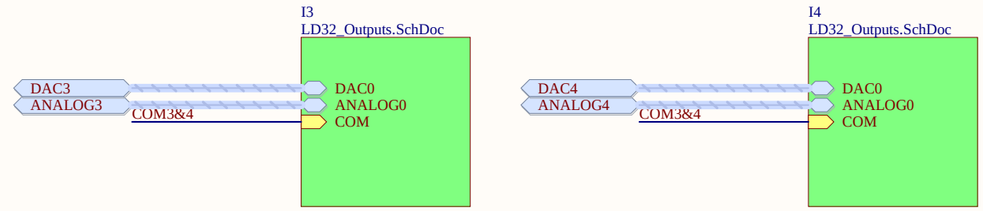


Project	LIGO DAC 32		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	FPGA		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024	Time: 1:46:38 PM	Sheet: 11 of 17	DrawnBy: M. Pirello, D. Sigg
File: FPGA_ART1X7.SchDoc			

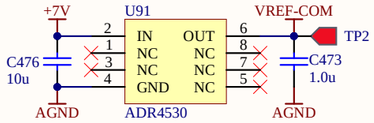
Multiple DAC's COM Distro







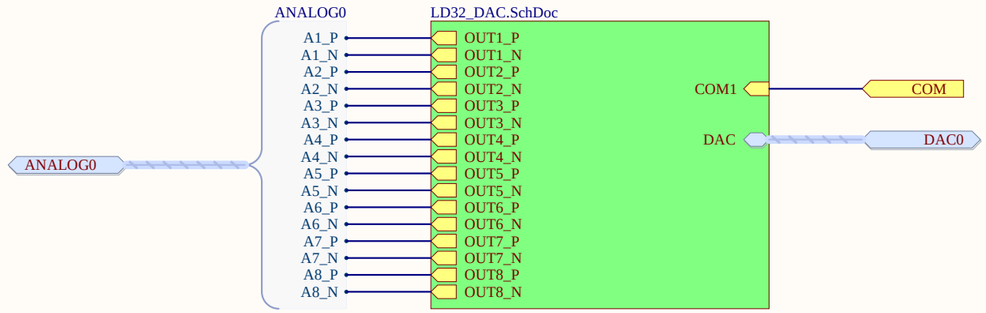
3.0V COM Reference



Parts Checked for =Value and Consistency

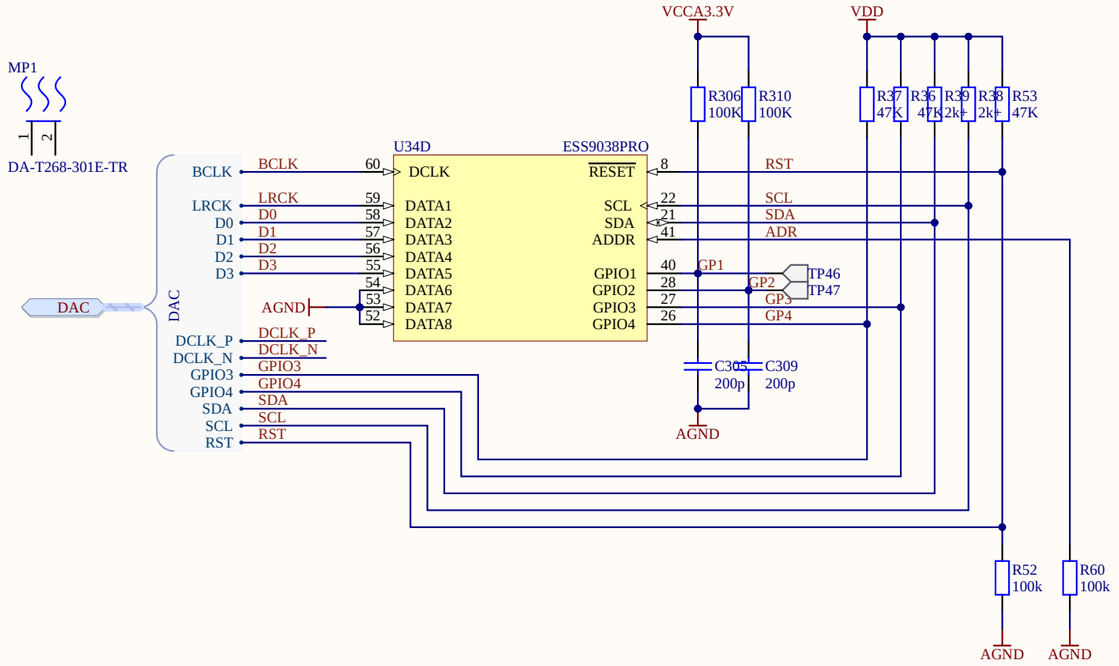
Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *DAC Top*			
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024 Time: 1:46:38 PM		Sheet: 12 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Analog.SchDoc			

DAC Overview

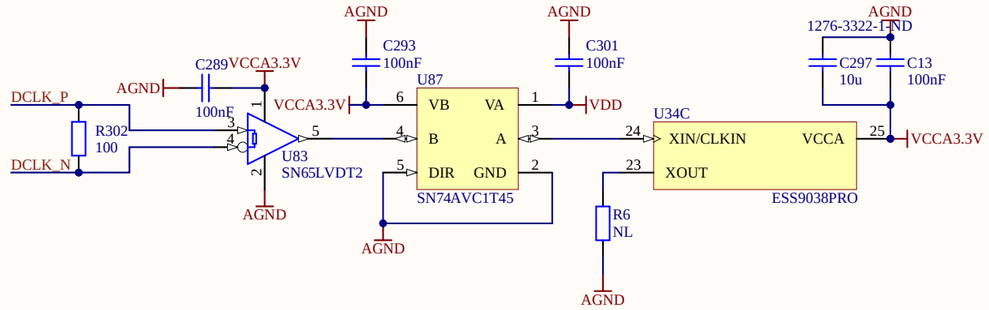


Project	***LIGO DAC 32***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Overview***		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024 Time: 1:46:38 PM		Sheet: 13 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Outputs.SchDoc			

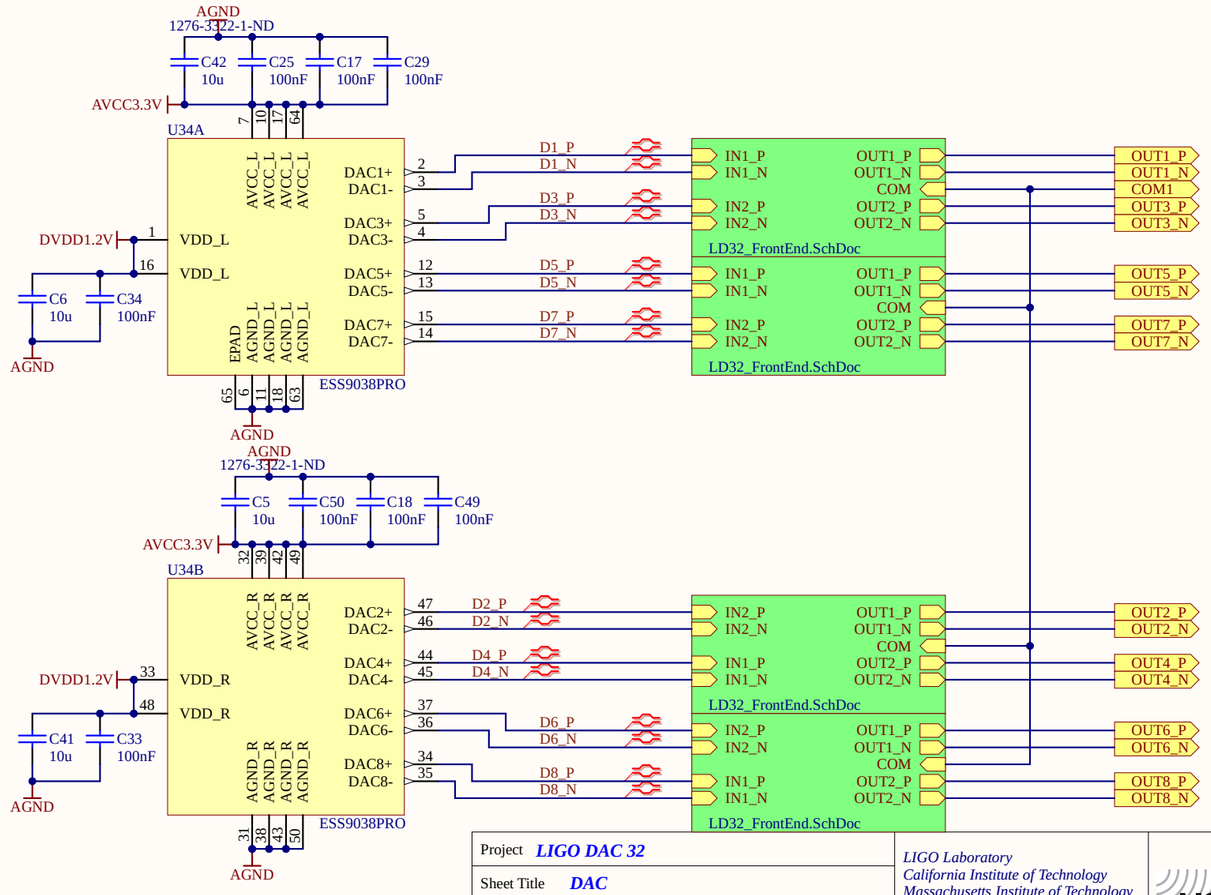
DAC Inputs



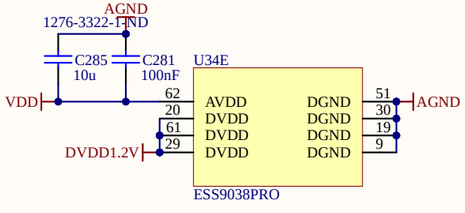
Main Clock



DAC Outputs



Core Power



Clock lines and reset could be shared in principle.

You also routed more lines than we really need.

1 fast clock (LVDS, SN65LVDS104 for FO)
1 BCLK
1 LRCLK
4 D lines
2 I2C lines
is needed per DAC.

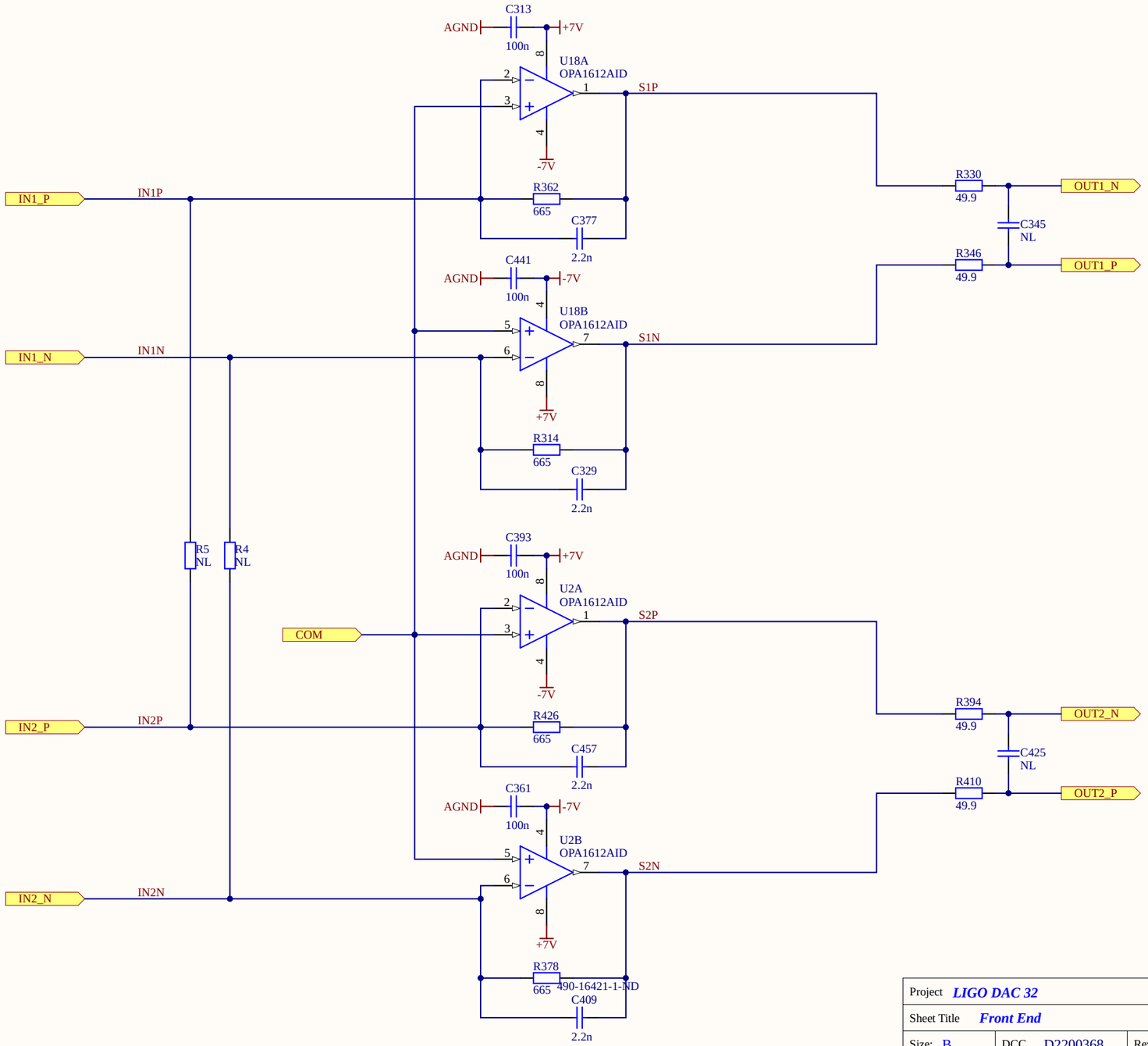
There will be a difference between Artix-7 and Artix Ultrascale with later only supporting 1.8V.

Daniel

Parts Checked for =Value and Consistency

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC*		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024	Time: 1:46:38 PM	Sheet: 14 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_DAC.SchDoc			

Front End Amplifiers



Parts Checked for =Value and Consistency

Project	***LIGO DAC 32***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***Front End***		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024 Time: 1:46:38 PM		Sheet: 15 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

PCIe Power

ChassisTimingInterfacePCIE
LD32_PCIE.SchDoc

PCIE
PCIE_TX0_N
PCIE_TX0_P
PCIE_TX1_N
PCIE_TX1_P
PCIE_TX2_N
PCIE_TX2_P
PCIE_TX3_N
PCIE_TX3_P
C274 220n
C276 220n
C272 220n
C273 220n
C270 220n
C271 220n
C268 220n
C269 220n
PER0_N
PER0_P
PER1_N
PER1_P
PER2_N
PER2_P
PER3_N
PER3_P
PCIExpress_X4_RX
RX

PCIE_RX0_N
PCIE_RX0_P
PCIE_RX1_N
PCIE_RX1_P
PCIE_RX2_N
PCIE_RX2_P
PCIE_RX3_N
PCIE_RX3_P
PET0_N
PET0_P
PET1_N
PET1_P
PET2_N
PET2_P
PET3_N
PET3_P
PCIExpress_X4_TX
TX

PCIE
POWER

PCIE_CLK_P
PCIE_CLK_N
C279 10nF
C278 10nF
REFCLK_P
REFCLK_N
WAKE#
SMDAT
SMCLK
PRSNT1#
PRSNT2#
PERST#
JTAG[1..5]
PCIExpress_X4_AUX SIGNALS
REFCLK+
REFCLK-
WAKE#
SMDAT
SMCLK
PRSNT1#
PRSNT2#
PERST#
JTAG[1..5]
AUX

PCIE_PERST
PCIE_PWRGD

GND
C262 100n
C280 100n
U82
VDD
VA
VB
A
B
GND
DIR
SN74AVC1T45
R299 NL
R300 15
R301 NL

PCIExpress_X4_POWER
3.3Vaux
+3.3V
+12V
GND
BUS12V
3097930
D7
R199 10m
SENS_120b_P
SENS_120b_N
12V
TP33
EXTGND
TP36
R218 10m
SENS_120x_N
SENS_120x_P
EXT12V

FL2 BNX016-01
FL1 BNX016-01
1
2
3
6
5
4
12VA
GND
12VF
GND

SENSE
SENS_33_P
SENS_33_N
SENS_25_P
SENS_25_N
SENS_18_P
SENS_18_N
SENS_10_P
SENS_10_N
SENS_120x_P
SENS_120x_N
SENS_120b_P
SENS_120b_N
SENS_VCCA3.3V
SENS_AVCC3.3V
SENS_DVDD1.2V
SENS_AVCC
SENS_AVTT
SENS_+7
SENS_-7
SENSE

PCIE_PWRGD

VDD
L5 33nH
U67
IN
IN
IN
EN/UV
SET
OUT
OUT
PG
OUTS
PGFB
ILIM
GND
GND
LT3045EMSE#TRPBF
R158 13.3K
R161 49.9k
SENS_AVTT
C212
C204
C93 10uF
C205
C224
C232
TP21
AVTT
GND
AVTT
C153 47uF
C159 1.0u
R235 12.1K
C167 3.3uF
R172 300
GND

VDD
L6 100nH
U68
LT3045EMSE#TRPBF
R157 10.0K
R162 49.9k
SENS_AVCC
C220
C226
C207
C233
C234
C94 10uF
TP22
AVCC
GND
AVCC
C154 47uF
C158 1.0u
R236 10k
C168 3.3uF
R173 300
GND

LT3045-1 Configs:
AVCC:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k

AVTT:
Vset = Iset * Rset = 100uA * Rset
Rs = 10k
Vset = 10k *100uA = 1.0V
PGFB:
Vset = 1.0V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.0/0.3-1)*50k = 116k > 100k

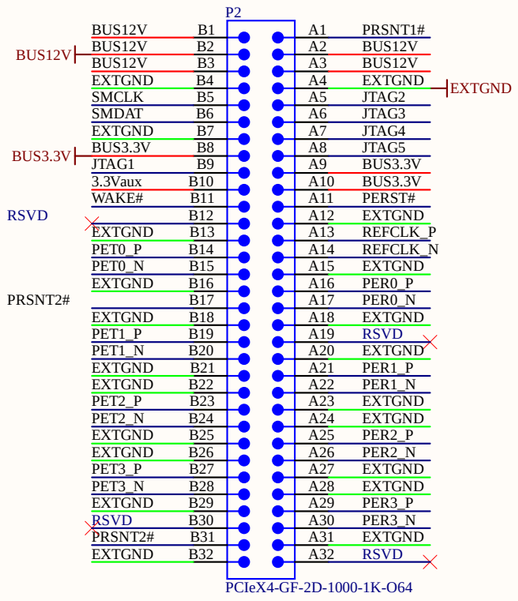
Parts Checked for =Value and Consistency
0201 parts need to be hand sorted

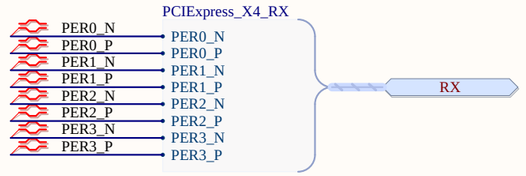
- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

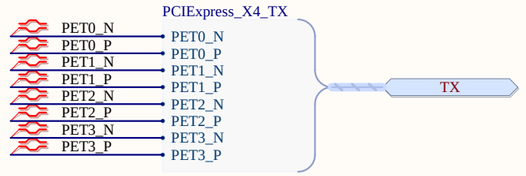
WM10869-ND
J1
EXT12V
EXTGND
45558-0003

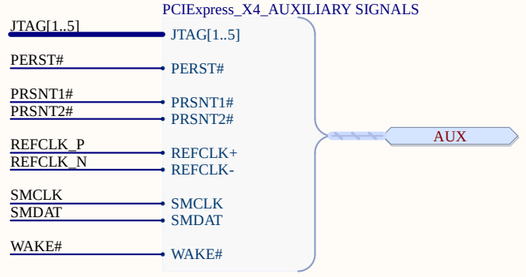
Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*PCIe Interface*		
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024	Time: 1:46:38 PM	Sheet: 16 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_PCIE_HL.SchDoc			

PCIe 4x Slot









Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *PCIe*			
Size: B	DCC D2200368	Rev: 1	
Date: 2/8/2024 Time: 1:46:38 PM		Sheet: 17 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_PCIE.SchDoc			