

Advanced LIGO Engineering Change Request (ECR)

ECR: Upgrade existing DAQ front-end chassis with new PCIe timing boards **DCC No: E2000625-v2**
Date: 01/15/2021

Requester: Daniel Sigg **Impacted Subsystem(s):** **CDS**

Description of Proposed Change(s):

We propose to upgrade all existing front-end systems to the new PCIe based timing interface. It will replace the existing DuoTone timing interface, the IRIG-B based commercial timing board, and a binary IO board. The backplane needs to be updated as well.

Reason for Change(s): As part of the A+ project we developed a new timing interface that directly plugs into an PCI Express slot. This solution is fully compatible with the existing LIGO timing distribution system. It can support multiple sampling rates within the same chassis and is required to support the new 524kHz sampling ADCs for the filter cavity design.

Estimated Cost: To upgrade the existing front-ends requires 27 new systems (timing interface, I/O backplane) per site. We should add 6 systems per site as spares and future needs. Thus 33 systems per site or 66 systems total.

The A+ project will be procuring 10 systems per site or 20 total for their project. This covers the added front-ends for each IFO plus test stands.

We will save money if this purchase is made at the same time as the A+ purchase. Here are estimated costs as the order size increases

Costs	PCIe Board	Backplane	Total
20 units	\$747 each	\$425 each	\$1,172
60 units	\$575 each	\$335 each	\$910
80 units	\$548 each	\$315 each	\$863

So the cost per site would be $33 \times \$863 = \$28,429$. We should also budget \$1,500 per site for cables and fixturing. So cost per site will be ~\$30,000 or \$60,000 total.

A check of the current CDS outlays at each site shows that each site should be able to absorb this expansion in the FY2021 LOPS.CDS budget, as large expenditures for the new front-end computers, etc. are already accounted for.

Schedule Impact Estimate: The existing I/O chassis delivered to the sites (but not yet installed) will need to be reworked for the hardware change. This can be done at the same time other work is done, such as eliminating the blinking LEDs on the PCIe expansion boards in each chassis and redoing the DC power distribution. At this point, only ~6 new I/O chassis are installed in the field at the LHO end-stations, so potential schedule impact to availability for commissioning should only be a few days at most.

Nature of Change (check all that apply):

- Hardware Safety
- Correct Hardware
- Correct Documentation

- Improve Hardware/Software
- Improve/Clarify Documentation
- Change Interface
- Change Requirement

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Importance:

- Desirable for ease of use, maintenance, safety
- Desirable for improved performance, reliability
- Essential for performance, reliability
- Essential for function
- Essential for hardware safety

Urgency:

- No urgency
- Desirable by date/event: Feb/March 2021 (A+ order date)
- Essential by date/event:
- Immediately (ASAP):

Impacted Hardware (select all that apply):

- Repair/Modify. List part & SNs: _____
- Scrap & Replace. List part & SNs: IRIG-B based timing boards; binary IO board; DuoTone timing interface (the later will become spares)
- Installed units? List IFO, part & SNs: _____
- Future units to be built

Impacted Documentation (list all dwgs, design reports, test reports, etc.):

[D1900002](#) IO expansion chassis
[E2000328](#) PCIe Timing Interface and related

Disposition of the proposed change(s):

The disposition of this proposed engineering change request is to be completed by Systems Engineering and indicated in the “Notes and Changes” metadata field in the DCC entry for this ECR. The typical dispositions are as follows:

- **Additional Information Required:** in which case the additional information requested is defined. The ECR requester then re-submits the ECR with the new information using the same DCC number for the ECR but with the next version number.
- **Rejected:** in which case the reason(s) for the rejection are to be given
- **Approved**
- **Approved with Caveat(s):** in which case the caveat(s) are listed
- **TRB:** the ECR is referred to an ad-hoc Technical Review Board for further evaluation and recommendation. It is the System Engineer’s (or designee’s) responsibility to organize the TRB. The System Engineer (or designee) then makes a technical decision based on the TRB’s recommendation. Links to the TRB’s documentation (charge, memos, final report, etc.) are to be added to the “Related Documents” field for this ECR.
- **CCB:** a change request for approval of additional funds or schedule impact is to be submitted to the Configuration Control Board. Links to the CCB’s documentation (CR, etc.) are to be added to the “Related Documents” field for this ECR.

Concurrence by Project Management:

Acknowledgement/acceptance/approval of the disposition is to be indicated by the electronic “signature” feature in the DCC entry for this ECR, by one of the following personnel:

- Systems Scientist
- Systems Engineer
- Deputy Systems Engineer