LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

LIGO Laboratory / LIGO Scientific Collaboration

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Test Procedure for PCIe Timing Interface

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1 Introduction

The following Test Procedure describes the test of proper operation of the PCIe Timing Interface.

S/N _____ FPGA: XC7A _____ T - _____

Tester _____ Date _____

2 Test Equipment

- Voltmeter
- Oscilloscope
- RF frequency synthesizer
- Fiber from a Timing Master/Fanout,
- Windows PC with open motherboard with at least 1 PCIe slot free. Alternatively, use a PC with an PCIe extender like the Adnaco.
- Extra PC ATX power supply
- Adapter: Dual PSU power supply 24-pin adapter cable for ATX motherboard, and
- IDC-10 header test adapter, and
- D-Sub test adapters, see D2100517.
- Test daughter board, D080192.
- 2 test adapter board for backplane, D2100184.
- Breakout Boards – DB37, DB25 if needed

3 Preparations

- PC needs to run Windows 10, 64-bit.
- Install Vivado 2020.1 or later.
- Download the FPGA test code, E2100232, and the production FPGA code, E2000337.
- Install the device driver for LIGO Timing.
- Install the LIGOTimingApp and LIGOTimingVerify programs.

4 Caution

When connecting test adapters, backplanes and daughter cards, it is important that the correct FPGA program is loaded. Otherwise, it is possible to short two outputs together which can potentially damage the board.

- Test adapters, D2100517 and D080192, require the FPGA timing test code, E2100232, to be loaded.
- The backplane, D20000297, daughter board, D2000331, and the GPS expansion module, D2000301, require the FPGA timing code, E2000337.

5 Timing Interface Tests

The PCIe Timing Interface is powered by either PCIe slot or External PCIe power. For this testing use the External PCIe power to measure current draw on the bench. **Use grounding strap while testing. Properly ground board before applying any voltage.**

1) **Verify the proper current draw without FPGA program.** Using a bench DC supply apply +12 Volts to the PCI power connector. Measure the current draw of the board prior to flashing the FPGA.

   +12 Volt current _____ 0.1 A Nom. (20mA)

2) **Check voltages on the following test points prior to flashing FPGA program. Come back after flashing the FPGA program and verify that the voltages did not change.**

TP30 (+12V)_____ TP40 (EXT12V)_____

TP32 (VDD 2.5V)_____ TP26 (VREG)_____

TP18 (VCC1V8)_____ TP17 (AVCC1V8)_____

TP21 (VCC)_____ TP34 (VCCINT1.0)_____

TP12 (P12V)_____ TP10 (N12V) _____

TP1 (P5V)_____ TP3 (N5V)_____

TP4 (VREF2V5)_____ TP11 (BGND)_____

TP36 (A12V)_____ TP35 (AGND)_____

_

TP19 (P10V)_____

TP14 (AVCC)_____ TP15 (AVTT)_____

3) **Flash the FPGA with the test code.** Using an FPGA programmer, flash the test program, E2100232, to the on-board SPI memory and press the program button (S2) on the back of the PCB behind the JTAG programming header. Ensure that the done light (DS1) is on when the process is complete. Return to step 2 and verify the voltages did not change, note any changes.

4) **Verify the synchronization frequencies.** Using a scope, check

TP20 (PSYNC)_____ Nominal: 524.288 kHz

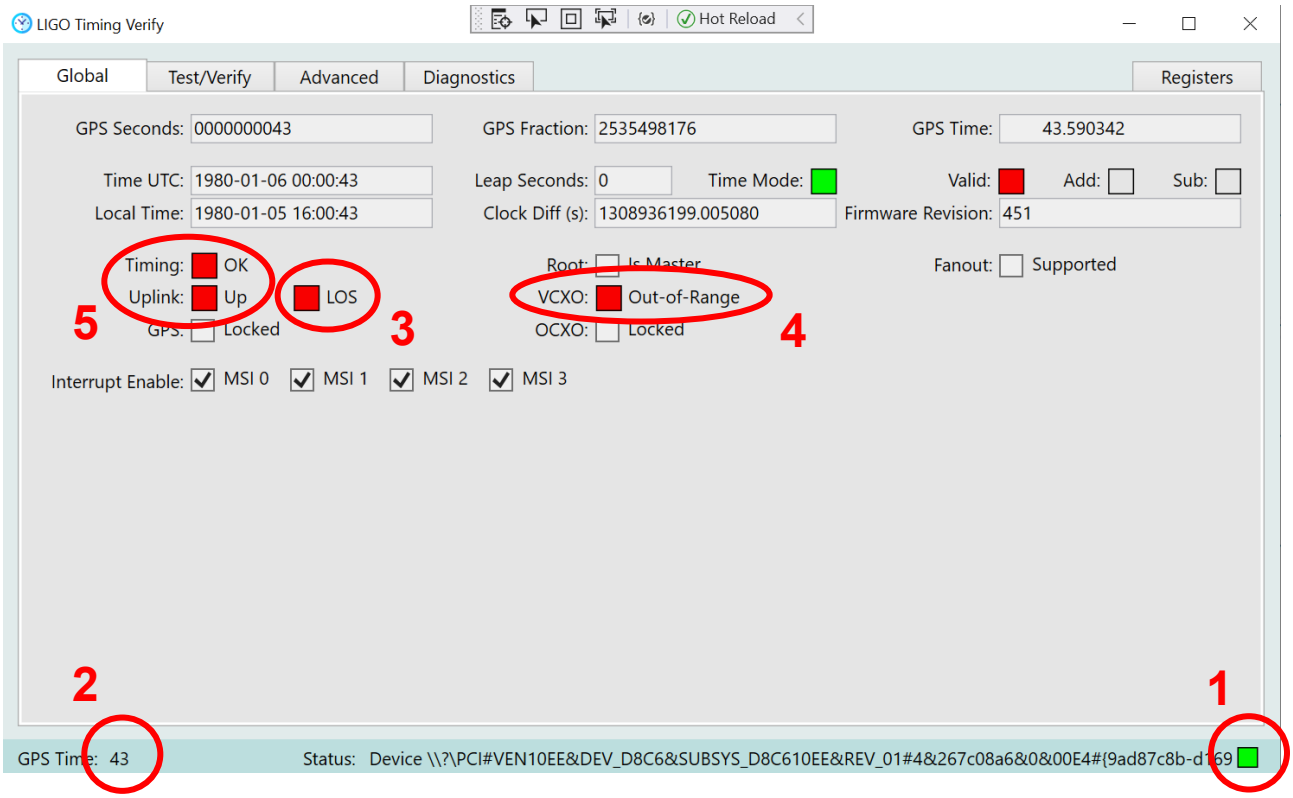
TP10/R41 bracket side (INV SYNC)_____ Nominal: 32.768 kHz

5) **Verify the proper current draw with FPGA program.** Using a bench DC supply apply +12Volts to the PCIE power connector. Measure the current draw of the board prior to flashing the FPGA.

+12 Volt current _____ Nom: 0.57 ± 0.1A

6) **Mount the test daughter board and D-Sub/IDC-10 test adapters, insert PCIe board into PC, and reboot.** Run the LIGO Timing Verify program

7) **Check PCIe functionality**



1: Device driver connected_____ Nominal: green

2: GPS Time display_____ Nominal: counting at 1 sec

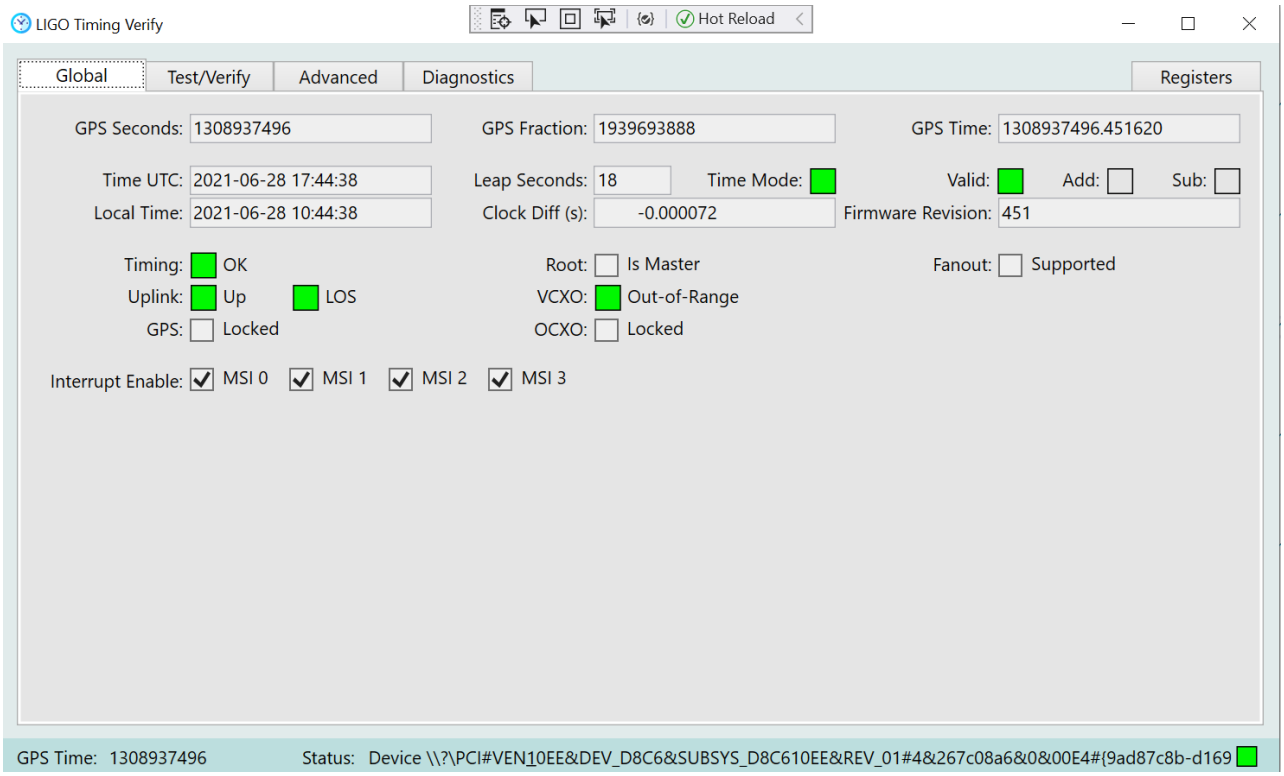
3: LOS (Loss of signal)_____ Nominal: red without fiber

4: VCXO out-of-range_____ Nominal: red

5: Timing OK/Uplink UP_____ Nominal: green

On board green LED_____ Nominal: off

8) Timing fiber connection



3: LOS (Loss of signal) _____ Nominal: green

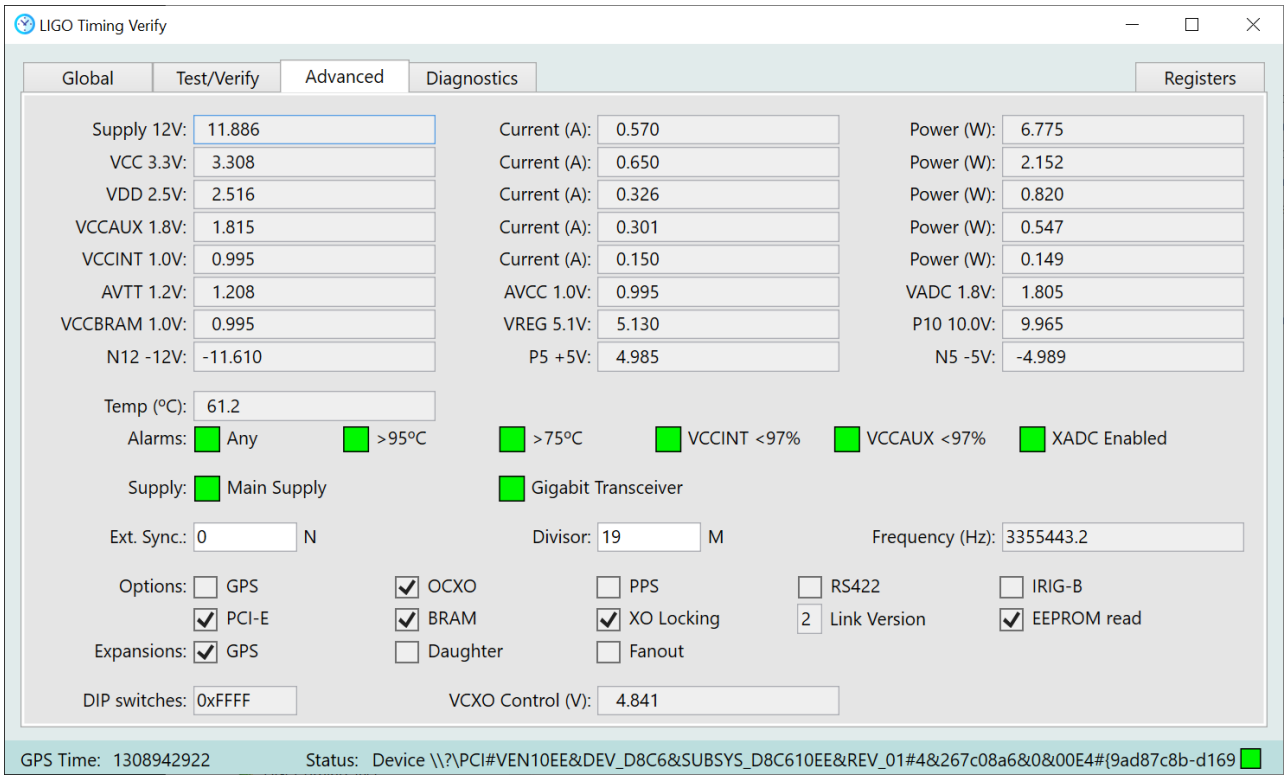
5: Timing OK/Uplink UP_____ Nominal: green

On board green LED_____ Nominal: on

2: GPS Time display_____ Nominal: large number

4: VCXO out-of-range_____ Nominal: green

9) Voltage and current readbacks



Supply 12V: _____ Nom: +12V Current (A)_____ Nom: ~0.58A

VCC 3.3V: _____ Nom: +3.3V Current (A)_____ Nom: ~0.65A

VDD 2.5V: _____ Nom: +2.5V Current (A)_____ Nom: ~0.34A

VCCAUX: _____ Nom: +1.8V Current (A)_____ Nom: ~0.30A

VCCINT: _____ Nom: +1.0V Current (A)_____ Nom: ~0.15A

AVTT: _____ Nom: +1.2V AVCC: _____ Nom: +1.0V

VADC: _____ Nom: +1.8V

VCCBRAM: _____ Nom: +1.0V VREG: _____ Nom: +5.1V

P10: _____ Nom: +10V N12: _____ Nom: −10V

P5: _____ Nom: +5V N5: _____ Nom: −5V

10) Check temperature and alarms

Temp: _____ Nom: 50ºC to 80ºC

Alarms Any: _____ Nom: varies >95ºC: _____ Nom: green

>75ºC: _____ Nom: varies VCCINT: _____ Nom: green

VCCAUX: _____ Nom: green XADC: _____ Nom: green

Supply: _____ Nom: green Giga TRX: _____ Nom: green

If the temperature reads below 75ºC, all alarms must show green. If not, “Any” and “75” will show red.

11) Check DIP switches

Nominal switch position of the DIP switch of the board are up. Readback should show 0xFFFF. Now toggle on-off-on each switch in succession starting towards the front of the board (SW1). The readbacks should go from 0xFFFE, 0xFFFD, 0xFFFB, 0xFFF7, 0xFFEF, 0xFFDF, 0xFFBF, to 0xFF7F.

SW1-8: _____: Nom: OK

Now press the two buttons S1 and S2 on the test daughter board and check again the readbacks. They should be 0xFEFF and 0xFDFF.

SW9/10: _____: Nom: OK

12) Check VCXO readback voltage.

This voltage goes from 0−10V and should be somewhat centered to be able to correct for the crystal aging over the years.

VCXO Voltage (V): _____: Nominal range: 3−7V

13) Check external frequency synchronization.

The default settings for Ext. Sync. N and the Divisor M are 0 and 19, respectively. The frequency should then read 3355443.2 Hz. Connect the scope to J9/J10 of the header test adapter and check that there is a differential RS422 square wave signal present at a frequency of 3.3554432 MHz.

J9/J10: _____ Nom: 3.3554432 MHz 3.3V TTL differential

Leave J9 on channel A, and connect channel B to J5 through J8 in turn. The nominal frequencies will be 8 times lower and at different phases.

J9/J5: _____ Nom: 419.4304 kHz at 0º phase, 3.3V TTL

J9/J6: _____ Nom: 419.4304 kHz at 135º phase, 3.3V TTL

J9/J7: _____ Nom: 419.4304 kHz at 90º phase, 3.3V TTL

J9/J8: _____ Nom: 419.4304 kHz at 45º phase, 3.3V TTL

Leave the scope on J9/J5 and check through the following N/M values.

N=0/M=0: _____ Nom: no frequency signal

N=1/M=0: _____ Nom: 2.048 kHz/256 Hz

N=15/M=0: _____ Nom: 33.554432/4.194304 MHz

N=0/M=1234: _____ Nom: 54.339/6.792 kHz

14) Check internal frequency synchronization.

Use a scope probe and check on testpoints TP20 (PWRSYNC) and R41 (INVSYNC).

TP20 (PWRSYNC): _____ Nom: 524.288 kHz 3.3V TTL

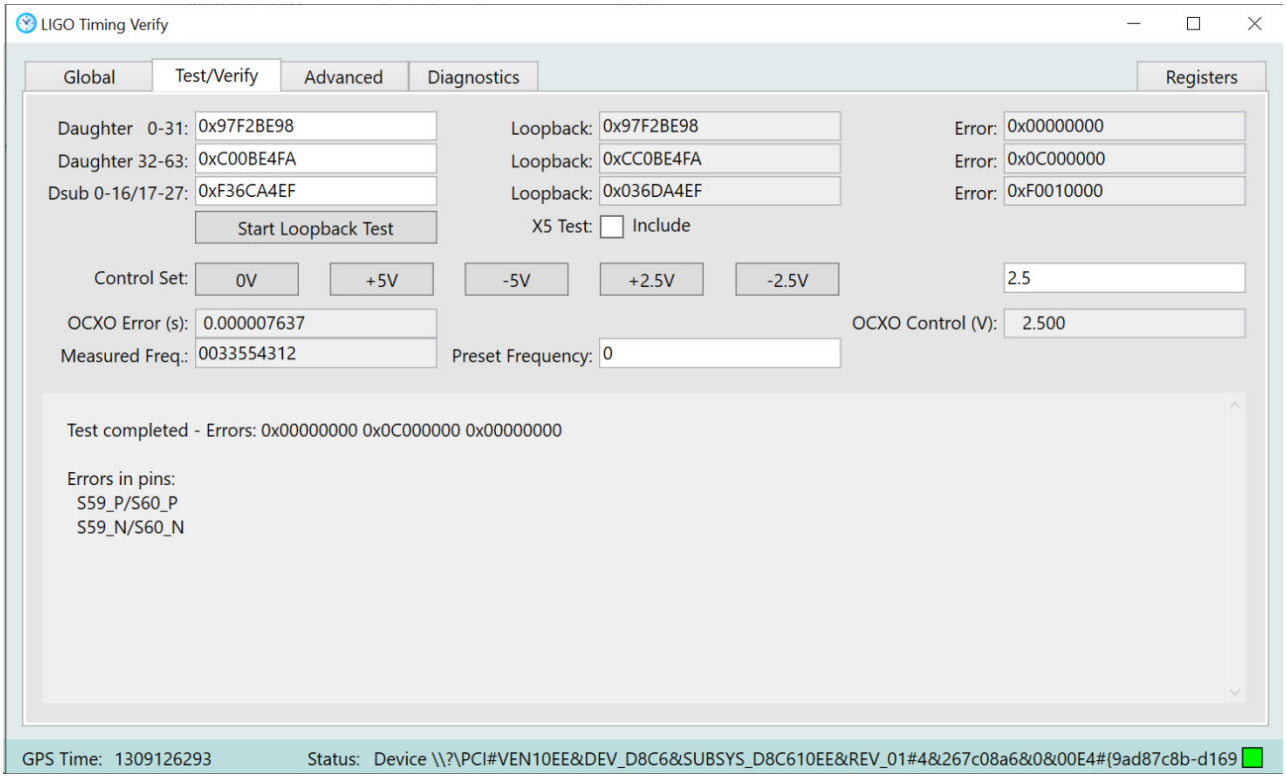
R41 (INVSYNC): _____ Nom: 32.768 kHz 12V

15) Check DuoTone

Connect the scope to J2 of the DB37 test adapter. It should show 2 sine waves at 960 Hz and 961 Hz and a amplitude ratio of 2. This generates a 1 Hz beat note.

DuoTone: _____ Nom: Present

16) Check OCXO locking.



Connect an OCXO, for example T0900279, to SMA input J5 on the rear side of the board. Check the measured frequency.

Measured frequency: _____ Nom: crystal frequency

Now check the control output by hitting the Control Set buttons in turn, while measuring the voltage at J5 of the DB25 test adapter.

Control set 0V: _____ Nom: +0.00V

Control set +5V: _____ Nom: +5.00V

Control set −5V: _____ Nom: −5.00V

Control set +2.5V: _____ Nom: +2.50V

Control set −2.5V: _____ Nom: −2.50V

17) Loopback testing.

Start the test by pressing the “Start Loopback Test” button. The test should return with "Test completed - No errors." If not, write down the failed signals:

Failed: _____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

18) Flash the FPGA with the production code. After removing all test adapters: Using an FPGA programmer, flash the production program, code, E2000337, to the on-board SPI memory and press the program button (S2) on the back of the PCB behind the JTAG programming header. Ensure that the done light (DS1) is on when the process is complete.

Put the board back into the test computer

19) Verify the proper current draw with FPGA program. Using a bench DC supply apply +12Volts to the PCIE power connector. Measure the current draw of the board prior to flashing the FPGA.

+12 Volt current _____ Nom: 0.7 ± 0.1A

6 Backplane Test

Continue with test procedure T2100299, if this timing interface is used with a backplane.

7 Pass/Fail

Pass: _____

Fail: _____

_____

_____

_____

_____

_____

_____

_____

_____