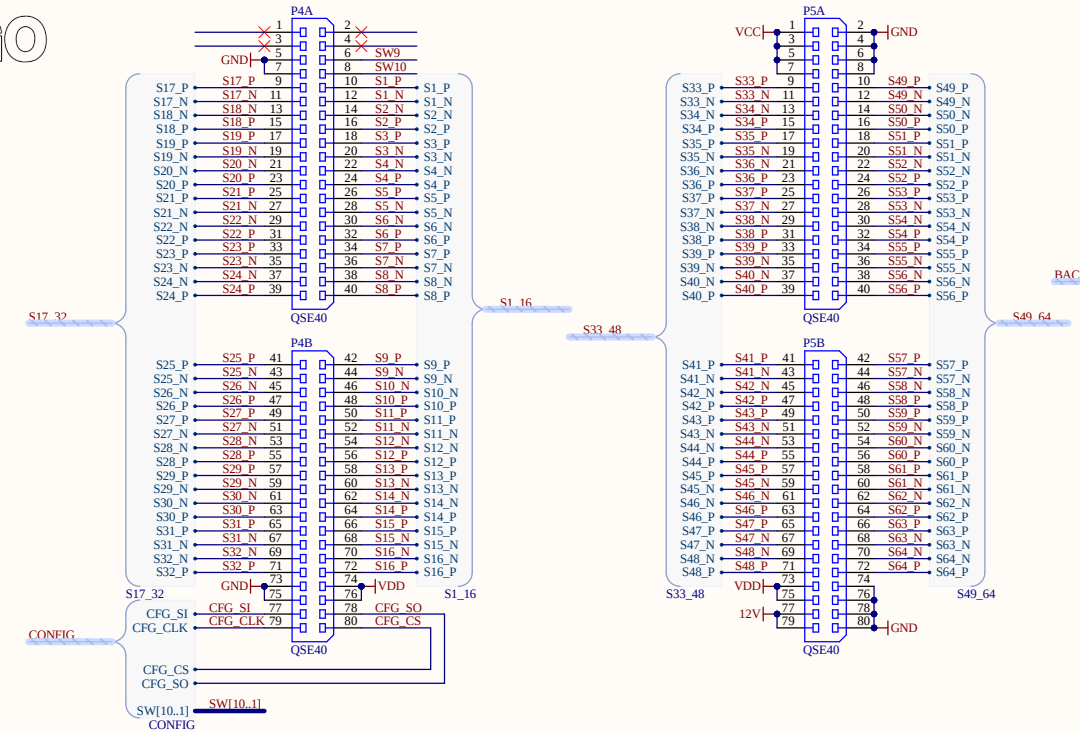
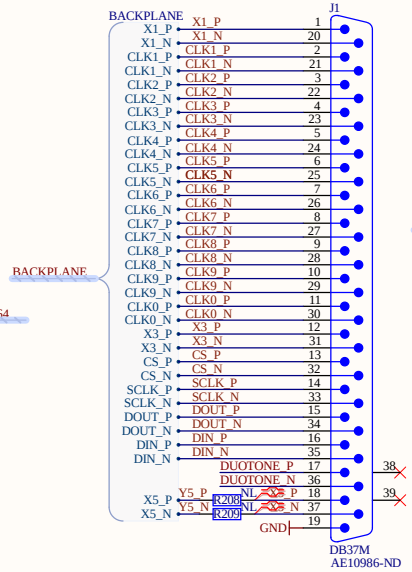
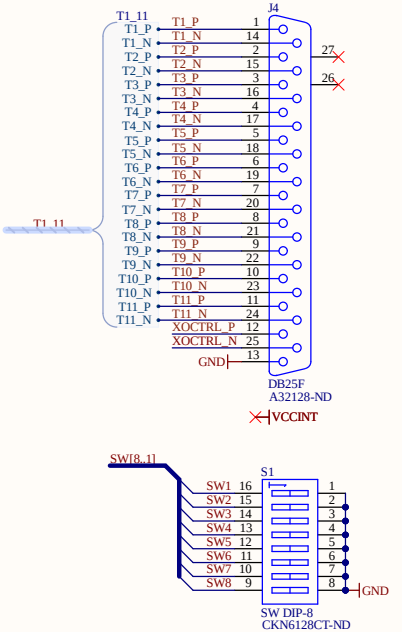
Samtec Expansion Port

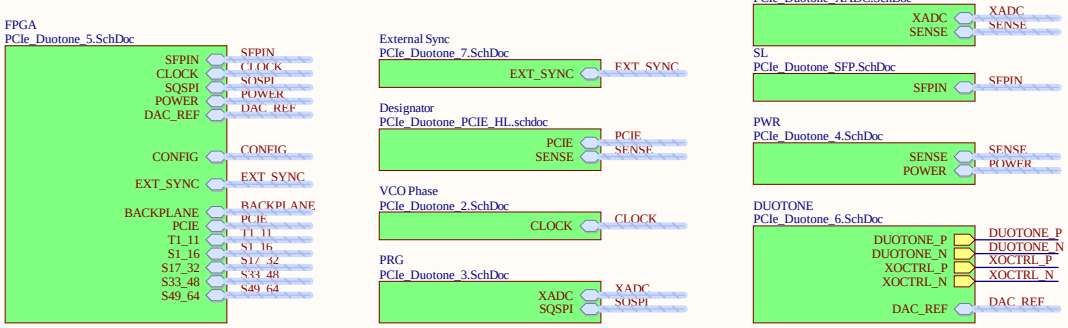


Duotone & Binary IO



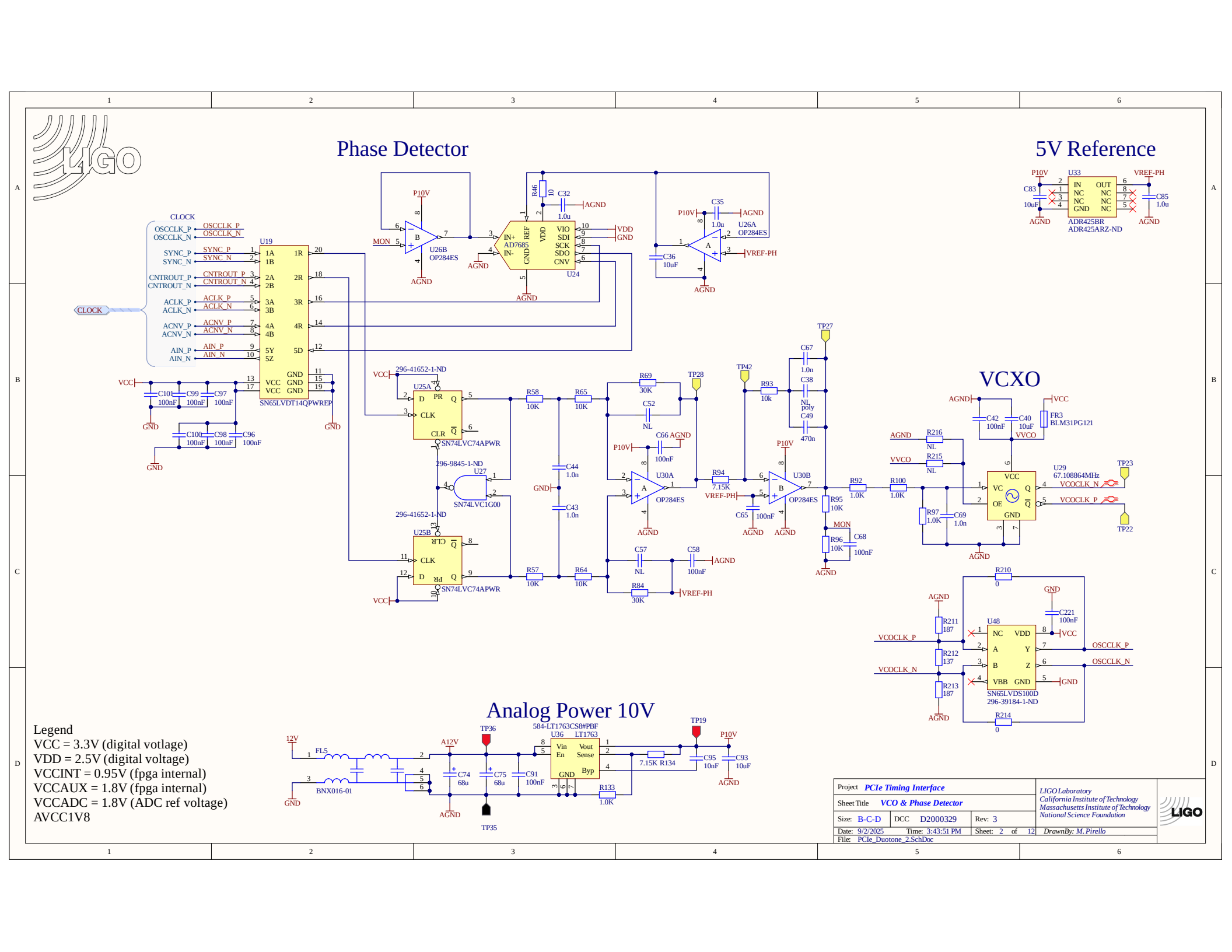
Rear DB25



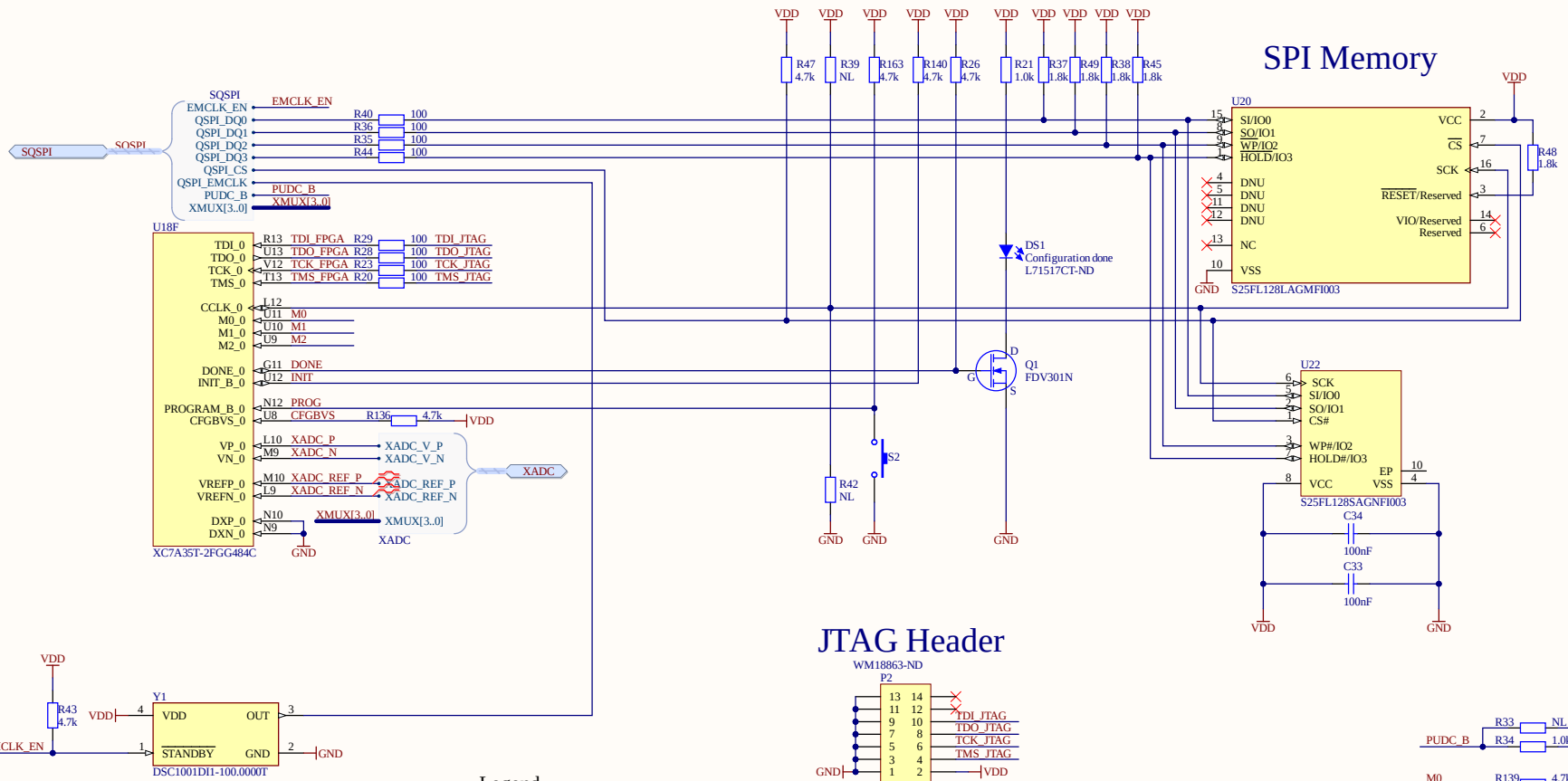


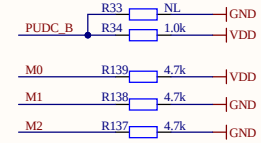
Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Timing Interface*		
Size: B-C-D	DCC D2000329	Rev: 3	
Date: 9/2/2025	Time: 3:43:50 PM	Sheet: 1 of 12	*DrawnBy: M. Pirello*
File: PCIe_Duotone_1.SchDoc			


Phase Detector
5V Reference
VCXO
Analog Power 10V
Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8
Project PCIe Timing Interface
Sheet Title VCO & Phase Detector
Size: B-C-D
DCC D2000329
Rev: 3
Date: 9/2/2025
Time: 3:43:51 PM
Sheet: 2 of 12
File: PCIe_Duotone_2.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello

JTAG and SPI Flash

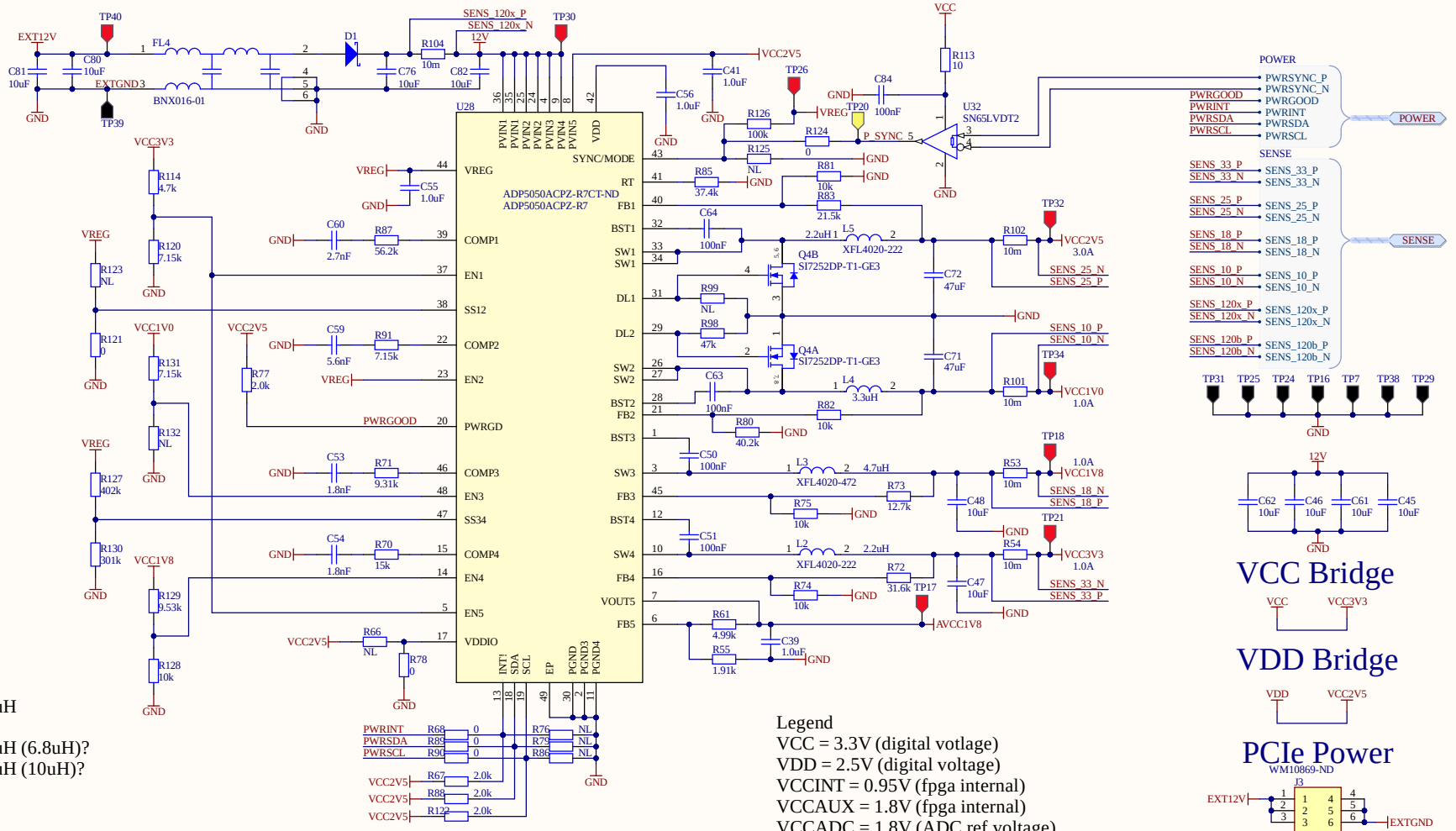




Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*JTAG & SPI Flash*		
Size: B-C-D	DCC D2000329	Rev: 3	
Date: 9/2/2025	Time: 3:43:51 PM	Sheet: 3 of 12	*DrawnBy: M. Pirello*
File: PCIe_Duotone_3.SchDoc			

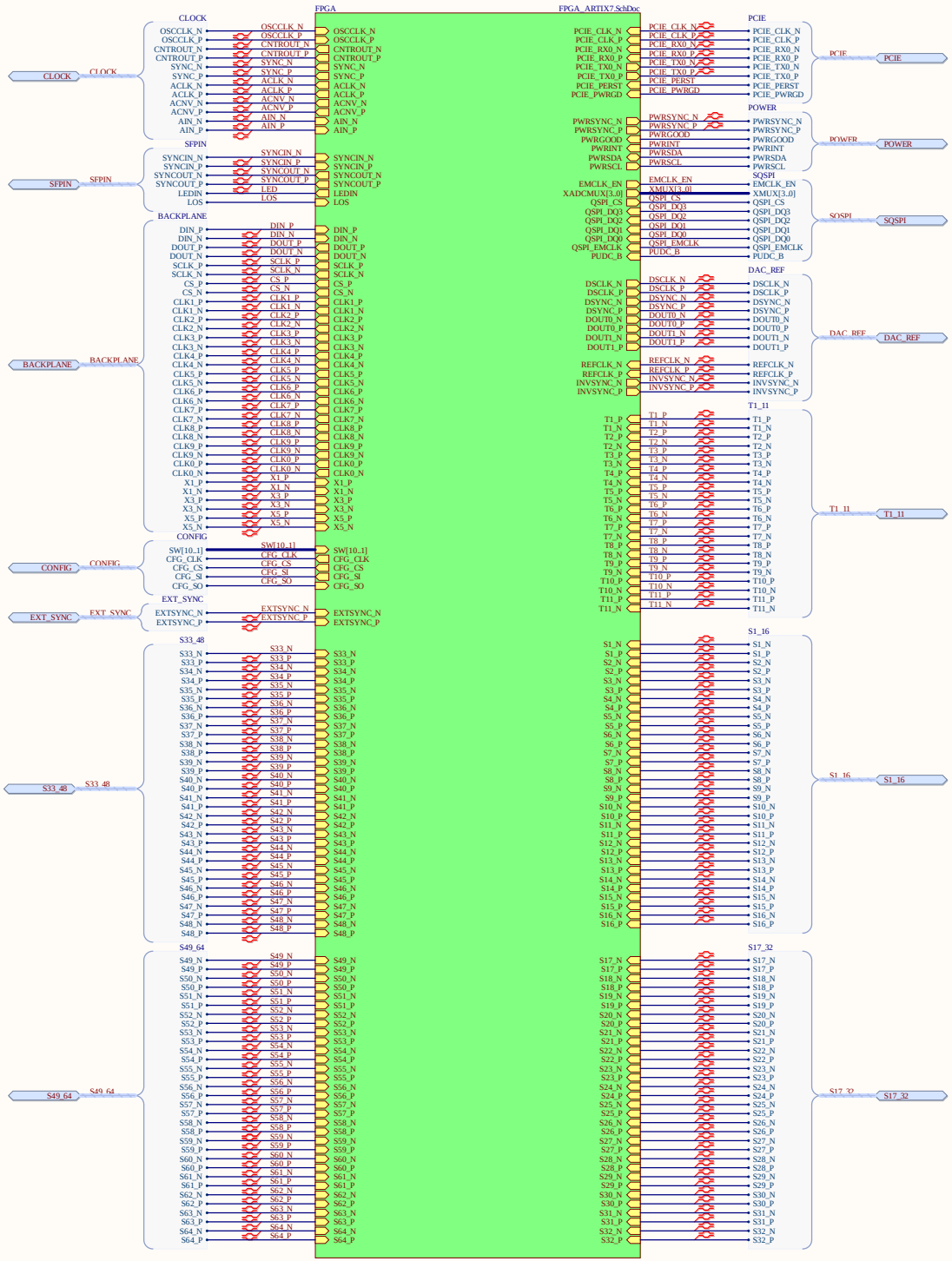
Switched FPGA Power

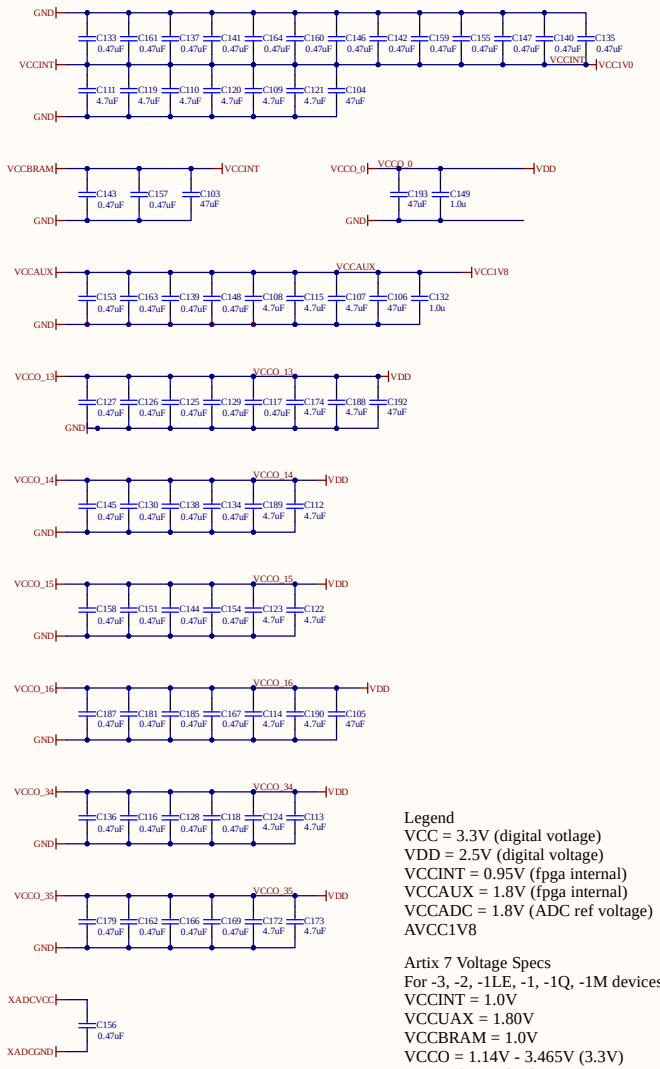


600kHz fsw?
RT Sync Calculation (R80)
FB1 - 2.5V 21.5k, 10.2k, 2.2uH
FB2 - 1.0V 10k. 40k, 3.3uH
FB3 - 1.8V 12.7k, 10.2k, 4.7uH (6.8uH)?
FB4 - 3.3V 31.6k, 10.2k, 2.2uH (10uH)?
FB5 - 1.8V 5k, 1.91k

Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Power Supply*		
Size: B-C-D	DCC D2000329	Rev: 3	
Date: 9/2/2025	Time: 3:43:51 PM	Sheet: 4 of 12	*DrawnBy: M. Pirello*
File: PCIe_Duotone_4.SchDoc			



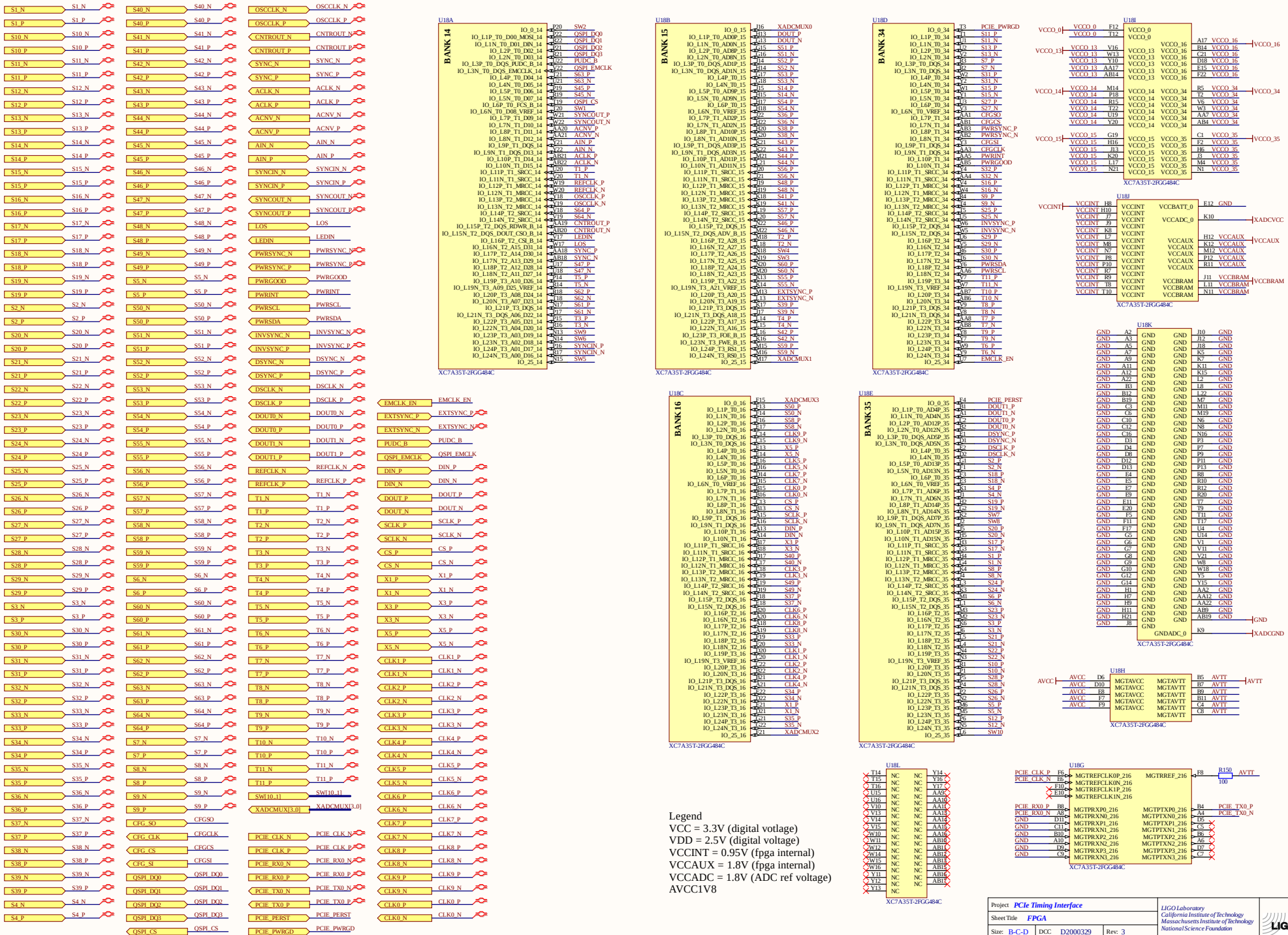


Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Artix 7 Voltage Specs
For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V

LVDS DC Specification
VCCO = 2.5
VOH = 1.675V
VOL = 0.7V

Project	PCIe Timing Interface	LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	LIGO
Sheet Title	FPGA Interface		
Size: B-C-D	DCC: D2000329	Rev: 3	
Date: 9/2/2025	Time: 3:43:51 PM	Sheet 5 of 12	DrawnBy: M. Pirello
File: PCIe_Duotone_5.SchDoc			


S1_N
S1_P
S10_N
S10_P
S11_N
S11_P
S12_N
S12_P
S13_N
S13_P
S14_N
S14_P
S15_N
S15_P
S16_N
S16_P
S17_N
S17_P
S18_N
S18_P
S19_N
S19_P
S2_N
S2_P
S20_N
S20_P
S21_N
S21_P
S22_N
S22_P
S23_N
S23_P
S24_N
S24_P
S25_N
S25_P
S26_N
S26_P
S27_N
S27_P
S28_N
S28_P
S29_N
S29_P
S3_N
S3_P
S30_N
S30_P
S31_N
S31_P
S32_N
S32_P
S33_N
S33_P
S34_N
S34_P
S35_N
S35_P
S36_N
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S37_N
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S38_N
S38_P
S39_N
S39_P
S4_N
S4_P
S40_N
S40_P
S41_N
S41_P
S42_N
S42_P
S43_N
S43_P
S44_N
S44_P
S45_N
S45_P
S46_N
S46_P
S47_N
S47_P
S48_N
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S49_P
S5_N
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S63_N
S63_P
S64_N
S64_P
S7_N
S7_P
S8_N
S8_P
S9_N
S9_P
CFG_SO
CFG_CLK
CFG_CS
CFG_SI
QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
QSPI_CS
OSCCLK_N
OSCCLK_P
CNTROUT_N
CNTROUT_P
SYNC_N
SYNC_P
ACLK_N
ACLK_P
ACNV_N
ACNV_P
AIN_N
AIN_P
SYNCIN_N
SYNCIN_P
SYNCOUT_N
SYNCOUT_P
LOS
LEDIN
PWRSYNC_N
PWRSYNC_P
PWRGOOD
PWRINT
PWRSCL
PWRSDA
INVSYNC_N
INVSYNC_P
DSYNC_N
DSYNC_P
DSCLK_N
DSCLK_P
DOUT0_N
DOUT0_P
DOUT1_N
DOUT1_P
REFCLK_N
REFCLK_P
T1_N
T1_P
T2_N
T2_P
T3_N
T3_P
T4_N
T4_P
T5_N
T5_P
T6_N
T6_P
T7_N
T7_P
T8_N
T8_P
T9_N
T9_P
T10_N
T10_P
T11_N
T11_P
SW[10..1]
XADCMUX[3..0]
PCIE_CLK_N
PCIE_CLK_P
PCIE_RX0_N
PCIE_RX0_P
PCIE_TX0_N
PCIE_TX0_P
PCIE_PERST
PCIE_PWRGD
U18A
BANK 14
IO_0_14
IO_L1P_T0_D00_MOSI_14
IO_L1N_T0_D01_DIN_14
IO_L2P_T0_D02_14
IO_L2N_T0_D03_14
IO_L3P_T0_DQS_PUDC_B_14
IO_L3N_T0_DQS_EMCCLK_14
IO_L4P_T0_D04_14
IO_L4N_T0_D05_14
IO_L5P_T0_D06_14
IO_L5N_T0_D07_14
IO_L6P_T0_FCS_B_14
IO_L6N_T0_D08_VREF_14
IO_L7P_T1_D09_14
IO_L7N_T1_D10_14
IO_L8P_T1_D11_14
IO_L8N_T1_D12_14
IO_L9P_T1_DQS_14
IO_L9N_T1_DQS_D13_14
IO_L10P_T1_D14_14
IO_L10N_T1_D15_14
IO_L11P_T1_SRCC_14
IO_L11N_T1_SRCC_14
IO_L12P_T1_MRCC_14
IO_L12N_T1_MRCC_14
IO_L13P_T2_MRCC_14
IO_L13N_T2_MRCC_14
IO_L14P_T2_SRCC_14
IO_L14N_T2_SRCC_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L16P_T2_CSI_B_14
IO_L16N_T2_A15_D31_14
IO_L17P_T2_A14_D30_14
IO_L17N_T2_A13_D29_14
IO_L18P_T2_A12_D28_14
IO_L18N_T2_A11_D27_14
IO_L19P_T3_A10_D26_14
IO_L19N_T3_A09_D25_VREF_14
IO_L20P_T3_A08_D24_14
IO_L20N_T3_A07_D23_14
IO_L21P_T3_DQS_14
IO_L21N_T3_DQS_A06_D22_14
IO_L22P_T3_A05_D21_14
IO_L22N_T3_A04_D20_14
IO_L23P_T3_A03_D19_14
IO_L23N_T3_A02_D18_14
IO_L24P_T3_A01_D17_14
IO_L24N_T3_A00_D16_14
IO_25_14
XC7A35T-2FGG484C
U18B
BANK 15
IO_0_15
IO_L1P_T0_AD0P_15
IO_L1N_T0_AD0N_15
IO_L2P_T0_AD8P_15
IO_L2N_T0_AD8N_15
IO_L3P_T0_DQS_AD1P_15
IO_L3N_T0_DQS_AD1N_15
IO_L4P_T0_15
IO_L4N_T0_15
IO_L5P_T0_AD9P_15
IO_L5N_T0_AD9N_15
IO_L6P_T0_15
IO_L6N_T0_VREF_15
IO_L7P_T1_AD2P_15
IO_L7N_T1_AD2N_15
IO_L8P_T1_AD10P_15
IO_L8N_T1_AD10N_15
IO_L9P_T1_DQS_AD3P_15
IO_L9N_T1_DQS_AD3N_15
IO_L10P_T1_AD11P_15
IO_L10N_T1_AD11N_15
IO_L11P_T1_SRCC_15
IO_L11N_T1_SRCC_15
IO_L12P_T1_MRCC_15
IO_L12N_T1_MRCC_15
IO_L13P_T2_MRCC_15
IO_L13N_T2_MRCC_15
IO_L14P_T2_SRCC_15
IO_L14N_T2_SRCC_15
IO_L15P_T2_DQS_AD7P_15
IO_L15N_T2_DQS_AD7N_15
IO_L16P_T2_A28_15
IO_L16N_T2_A27_15
IO_L17P_T2_A26_15
IO_L17N_T2_A25_15
IO_L18P_T2_A24_15
IO_L18N_T2_A23_15
IO_L19P_T3_A22_15
IO_L19N_T3_A21_VREF_15
IO_L20P_T3_A20_15
IO_L20N_T3_A19_15
IO_L21P_T3_DQS_15
IO_L21N_T3_DQS_A18_15
IO_L22P_T3_A17_15
IO_L22N_T3_A16_15
IO_L23P_T3_FOE_B_15
IO_L23N_T3_FWE_B_15
IO_L24P_T3_RS1_15
IO_L24N_T3_RS0_15
IO_25_15
XC7A35T-2FGG484C
U18D
BANK 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
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U18I
VCCO_0
VCCO_13
VCCO_14
VCCO_15
VCCO_16
VCCO_34
VCCO_35
XC7A35T-2FGG484C
U18J
VCCINT
VCCBATT_0
VCCADC_0
VCCAUX
VCCBRAM
XADCVCC
XADCGND
XC7A35T-2FGG484C
U18K
GND
GNDADC_0
XC7A35T-2FGG484C
U18C
BANK 16
IO_0_16
IO_L1P_T0_16
IO_L1N_T0_16
IO_L2P_T0_16
IO_L2N_T0_16
IO_L3P_T0_DQS_16
IO_L3N_T0_DQS_16
IO_L4P_T0_16
IO_L4N_T0_16
IO_L5P_T0_16
IO_L5N_T0_16
IO_L6P_T0_16
IO_L6N_T0_VREF_16
IO_L7P_T1_16
IO_L7N_T1_16
IO_L8P_T1_16
IO_L8N_T1_16
IO_L9P_T1_DQS_16
IO_L9N_T1_DQS_16
IO_L10P_T1_16
IO_L10N_T1_16
IO_L11P_T1_SRCC_16
IO_L11N_T1_SRCC_16
IO_L12P_T1_MRCC_16
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IO_L13P_T2_MRCC_16
IO_L13N_T2_MRCC_16
IO_L14P_T2_SRCC_16
IO_L14N_T2_SRCC_16
IO_L15P_T2_DQS_16
IO_L15N_T2_DQS_16
IO_L16P_T2_16
IO_L16N_T2_16
IO_L17P_T2_16
IO_L17N_T2_16
IO_L18P_T2_16
IO_L18N_T2_16
IO_L19P_T3_16
IO_L19N_T3_VREF_16
IO_L20P_T3_16
IO_L20N_T3_16
IO_L21P_T3_DQS_16
IO_L21N_T3_DQS_16
IO_L22P_T3_16
IO_L22N_T3_16
IO_L23P_T3_16
IO_L23N_T3_16
IO_L24P_T3_16
IO_L24N_T3_16
IO_25_16
XC7A35T-2FGG484C
U18E
BANK 35
IO_0_35
IO_L1P_T0_AD4P_35
IO_L1N_T0_AD4N_35
IO_L2P_T0_AD12P_35
IO_L2N_T0_AD12N_35
IO_L3P_T0_DQS_AD5P_35
IO_L3N_T0_DQS_AD5N_35
IO_L4P_T0_35
IO_L4N_T0_35
IO_L5P_T0_AD13P_35
IO_L5N_T0_AD13N_35
IO_L6P_T0_35
IO_L6N_T0_VREF_35
IO_L7P_T1_AD6P_35
IO_L7N_T1_AD6N_35
IO_L8P_T1_AD14P_35
IO_L8N_T1_AD14N_35
IO_L9P_T1_DQS_AD7P_35
IO_L9N_T1_DQS_AD7N_35
IO_L10P_T1_AD15P_35
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IO_L11P_T1_SRCC_35
IO_L11N_T1_SRCC_35
IO_L12P_T1_MRCC_35
IO_L12N_T1_MRCC_35
IO_L13P_T2_MRCC_35
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IO_L14P_T2_SRCC_35
IO_L14N_T2_SRCC_35
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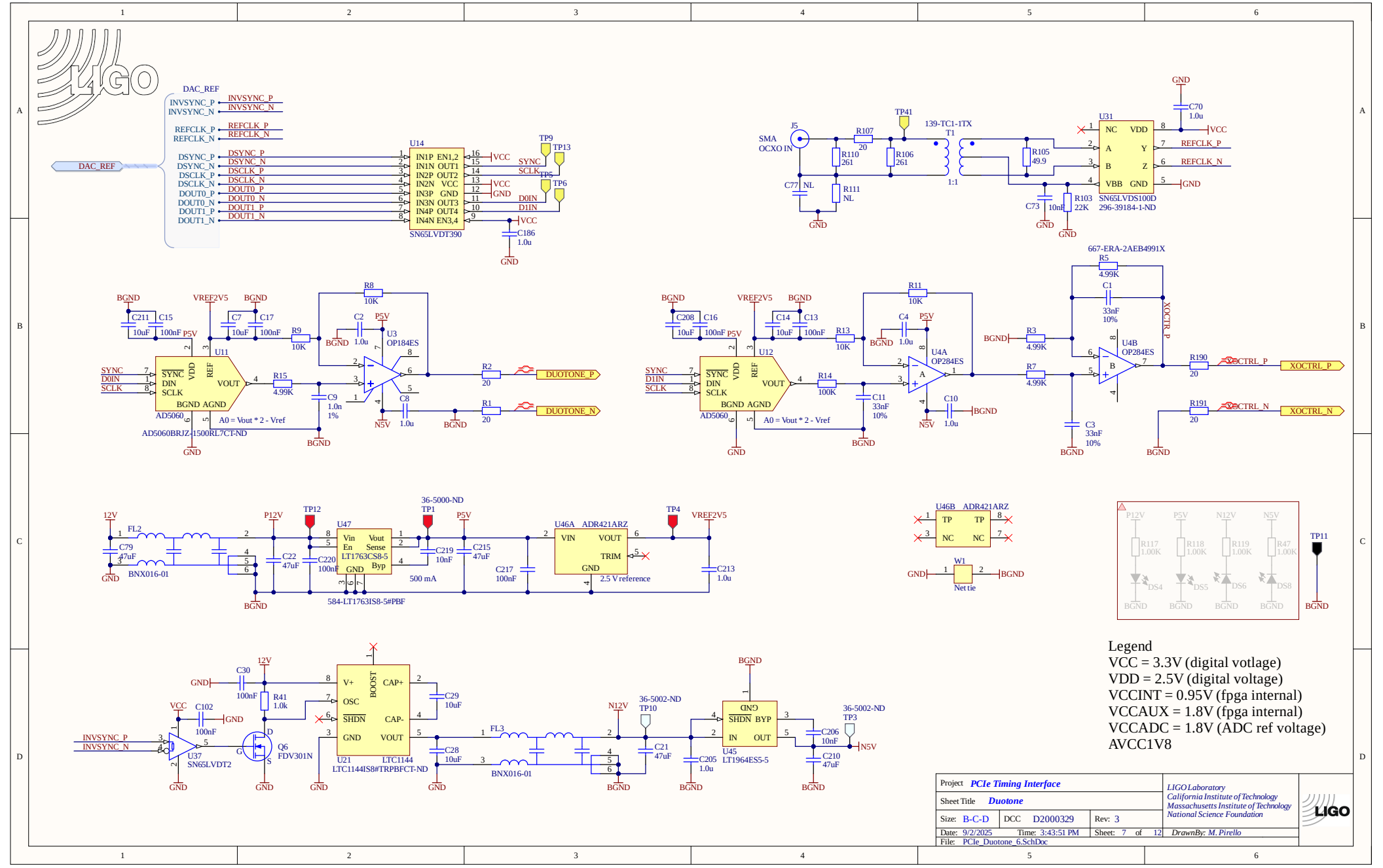
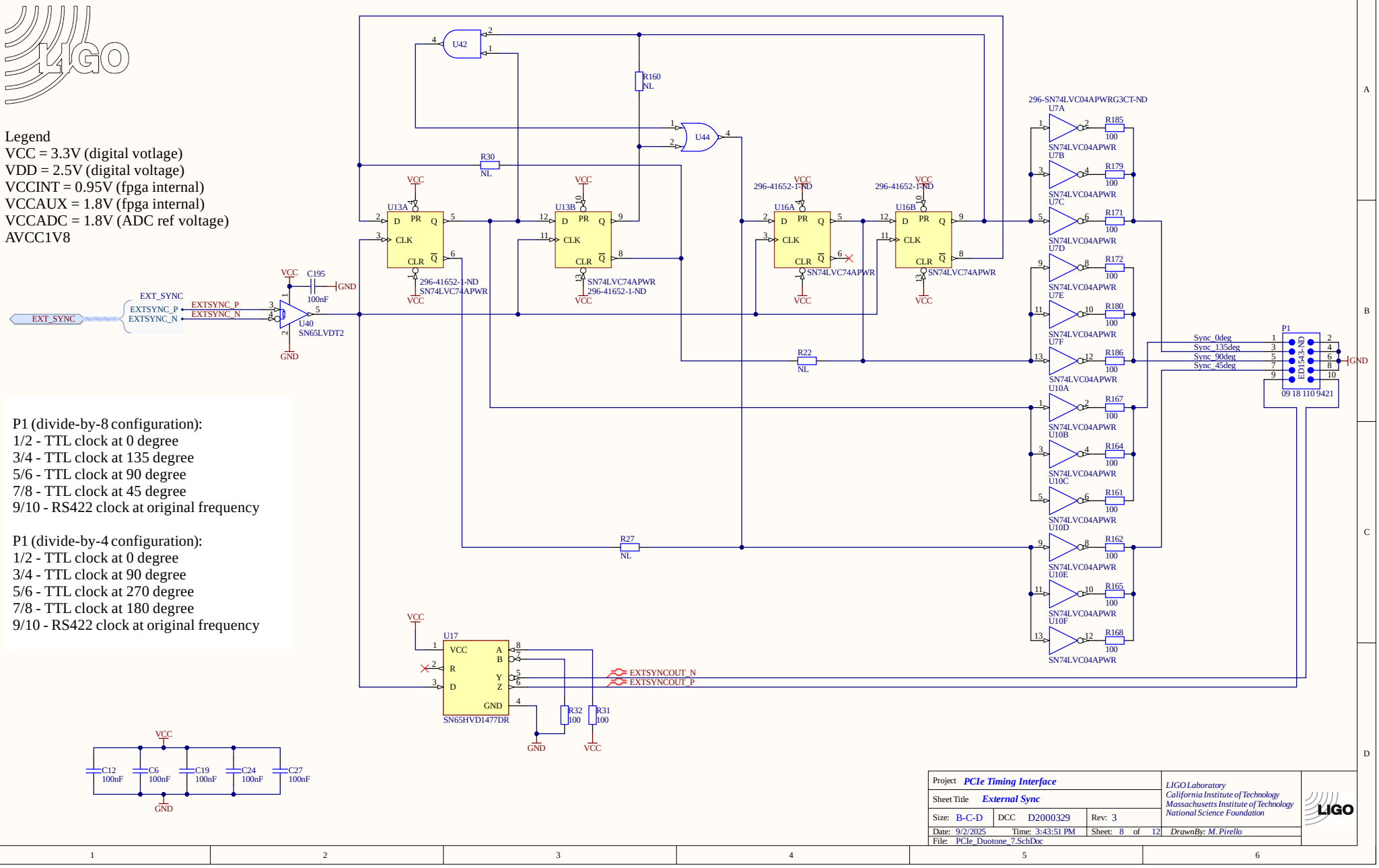
IO_L17N_T2_35
IO_L18P_T2_35
IO_L18N_T2_35
IO_L19P_T3_35
IO_L19N_T3_VREF_35
IO_L20P_T3_35
IO_L20N_T3_35
IO_L21P_T3_DQS_35
IO_L21N_T3_DQS_35
IO_L22P_T3_35
IO_L22N_T3_35
IO_L23P_T3_35
IO_L23N_T3_35
IO_L24P_T3_35
IO_L24N_T3_35
IO_25_35
XC7A35T-2FGG484C
U18H
AVCC
MGTAVCC
MGTAVTT
AVTT
XC7A35T-2FGG484C
U18L
NC
XC7A35T-2FGG484C
U18G
MGTREFCLK0P_216
MGTREFCLK0N_216
MGTREFCLK1P_216
MGTREFCLK1N_216
MGTREFR_216
MGTPRXP0_216
MGTPRXN0_216
MGTPRXP1_216
MGTPRXN1_216
MGTPRXP2_216
MGTPRXN2_216
MGTPRXP3_216
MGTPRXN3_216
MGTPTXP0_216
MGTPTXN0_216
MGTPTXP1_216
MGTPTXN1_216
MGTPTXP2_216
MGTPTXN2_216
MGTPTXP3_216
MGTPTXN3_216
R150
100
XC7A35T-2FGG484C
EMCLK_EN
EXTSYNC_P
EXTSYNC_N
PUDC_B
QSPI_EMCLK
DIN_P
DIN_N
DOUT_P
DOUT_N
SCLK_P
SCLK_N
CS_P
CS_N
X1_P
X1_N
X3_P
X3_N
X5_P
X5_N
CLK1_P
CLK1_N
CLK2_P
CLK2_N
CLK3_P
CLK3_N
CLK4_P
CLK4_N
CLK5_P
CLK5_N
CLK6_P
CLK6_N
CLK7_P
CLK7_N
CLK8_P
CLK8_N
CLK9_P
CLK9_N
CLK0_P
CLK0_N
Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8
Project PCIe Timing Interface
Sheet Title FPGA
Size: B-C-D
DCC D2000329
Rev: 3
Date: 9/2/2025
Time: 3:43:51 PM
Sheet 6 of 12
File: FPGA_ARTIX7.SchDoc
DrawnBy: M.Pirello
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
LIGO

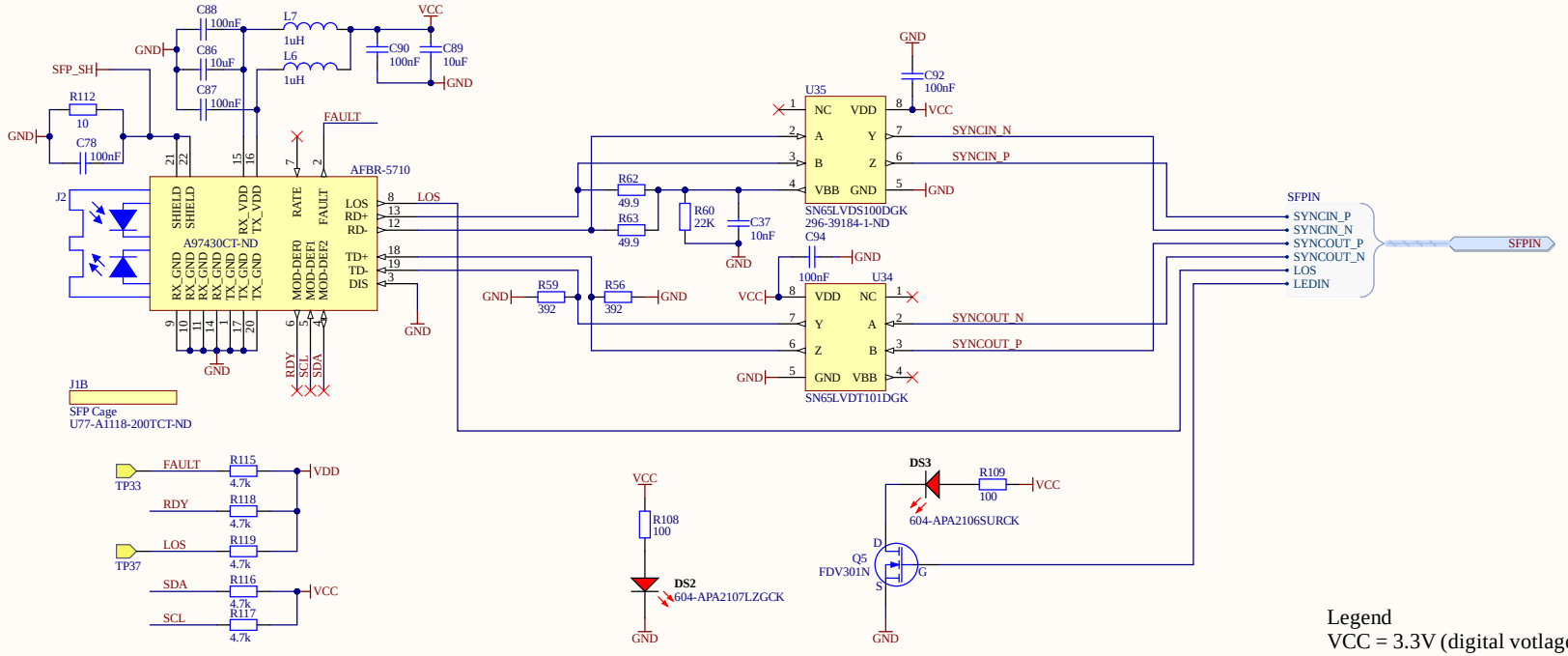


Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Project	PCIe Timing Interface		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	Duotone		
Size: B-C-D	DCC D2000329	Rev: 3	
Date: 9/2/2025	Time: 3:43:51 PM	Sheet: 7 of 12	DrawnBy: M. Pirello
File: PCIe_Duotone_6.SchDoc			

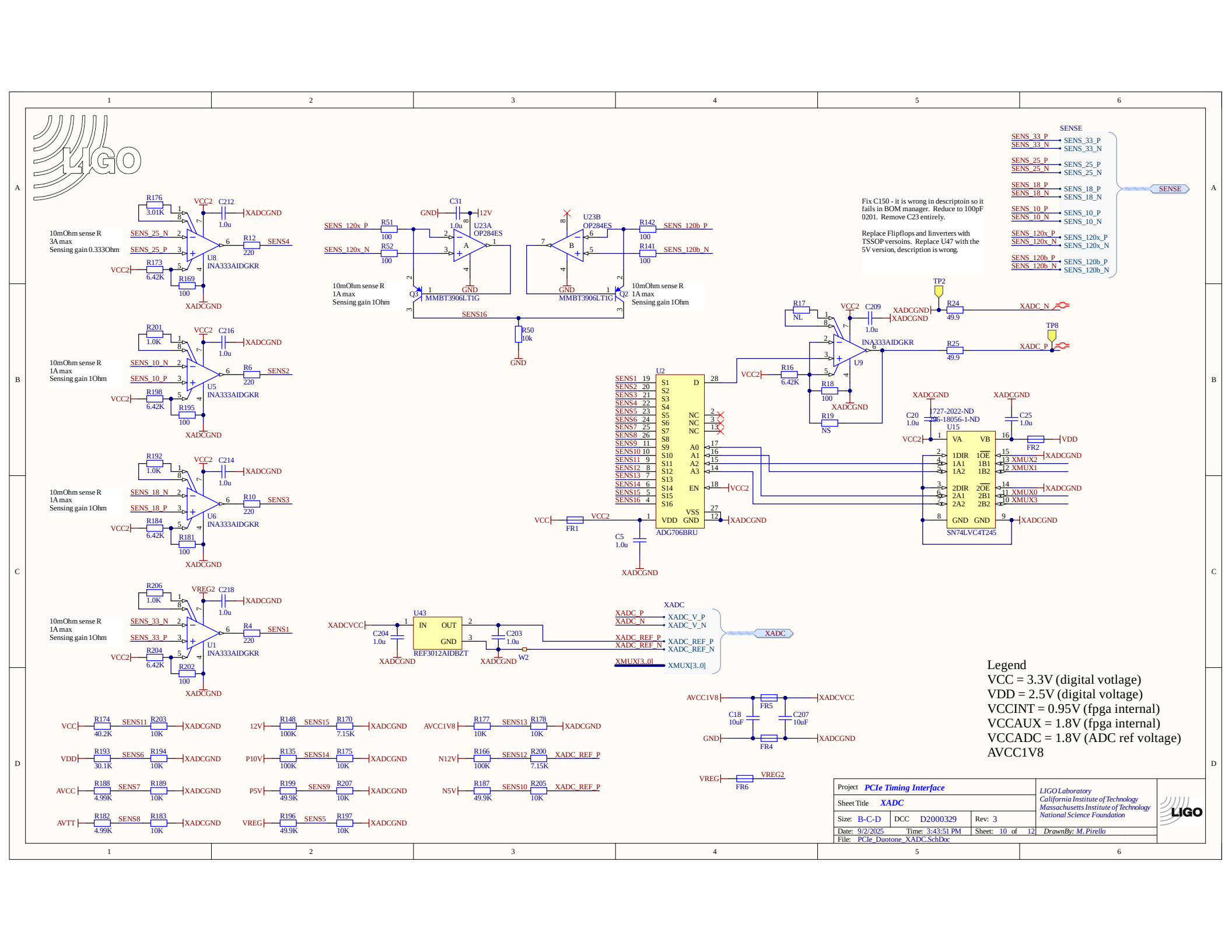

Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8
P1 (divide-by-8 configuration):
1/2 - TTL clock at 0 degree
3/4 - TTL clock at 135 degree
5/6 - TTL clock at 90 degree
7/8 - TTL clock at 45 degree
9/10 - RS422 clock at original frequency
P1 (divide-by-4 configuration):
1/2 - TTL clock at 0 degree
3/4 - TTL clock at 90 degree
5/6 - TTL clock at 270 degree
7/8 - TTL clock at 180 degree
9/10 - RS422 clock at original frequency
EXT_SYNC
EXTSYNC_P
EXTSYNC_N
U40
SN65LVDT2
C195
100nF
U42
U44
R160
NL
R30
NL
R22
NL
R27
NL
U13A
U13B
U16A
U16B
SN74LVC74APWR
296-41652-1-ND
296-SN74LVC04APWRG3CT-ND
SN74LVC04APWR
U7A
U7B
U7C
U7D
U7E
U7F
U10A
U10B
U10C
U10D
U10E
U10F
R185
R179
R171
R172
R180
R186
R167
R164
R161
R162
R165
R168
100
P1
ED1543-ND
09 18 110 9421
Sync_0deg
Sync_135deg
Sync_90deg
Sync_45deg
U17
SN65HVD1477DR
R32
R31
EXTSYNCOUT_N
EXTSYNCOUT_P
C12
C6
C19
C24
C27
VCC
GND
Project PCIe Timing Interface
Sheet Title External Sync
Size: B-C-D
DCC D2000329
Rev: 3
Date: 9/2/2025
Time: 3:43:51 PM
Sheet: 8 of 12
File: PCIe_Duotone_7.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello

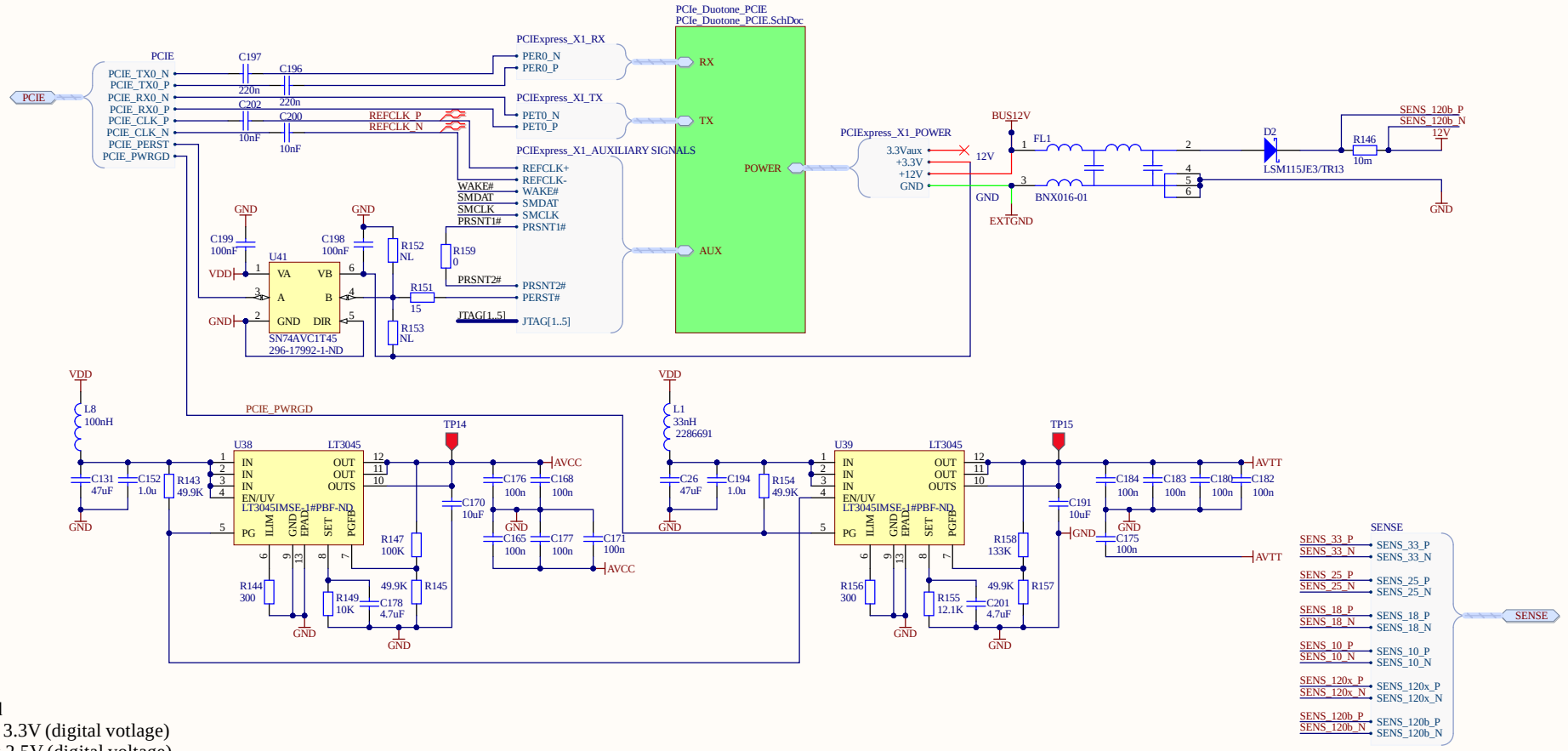
SFP Port



Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Project	PCIe Timing Interface		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	SFP		
Size: B-C-D	DCC D2000329	Rev: 3	
Date: 9/2/2025 Time: 3:43:51 PM		Sheet: 9 of 12	DrawnBy: M. Pirello
File: PCIe_Duotone_SFP.SchDoc			

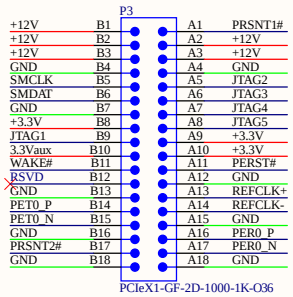

10mOhm sense R
3A max
Sensing gain 0.333Ohm
10mOhm sense R
1A max
Sensing gain 1Ohm
10mOhm sense R
1A max
Sensing gain 1Ohm
10mOhm sense R
1A max
Sensing gain 1Ohm
10mOhm sense R
1A max
Sensing gain 1Ohm
10mOhm sense R
1A max
Sensing gain 1Ohm
Fix C150 - it is wrong in descriptoin so it fails in BOM manager. Reduce to 100pF 0201. Remove C23 entirely.
Replace Flipflops and linverters with TSSOP versoins. Replace U47 with the 5V version, description is wrong.
SENSE
XADC
Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8
Project PCIe Timing Interface
Sheet Title XADC
Size: B-C-D
DCC D2000329
Rev: 3
Date: 9/2/2025
Time: 3:43:51 PM
Sheet: 10 of 12
File: PCIe_Duotone_XADC.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello

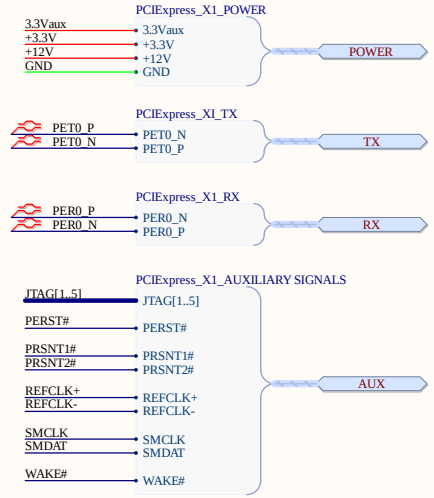


Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

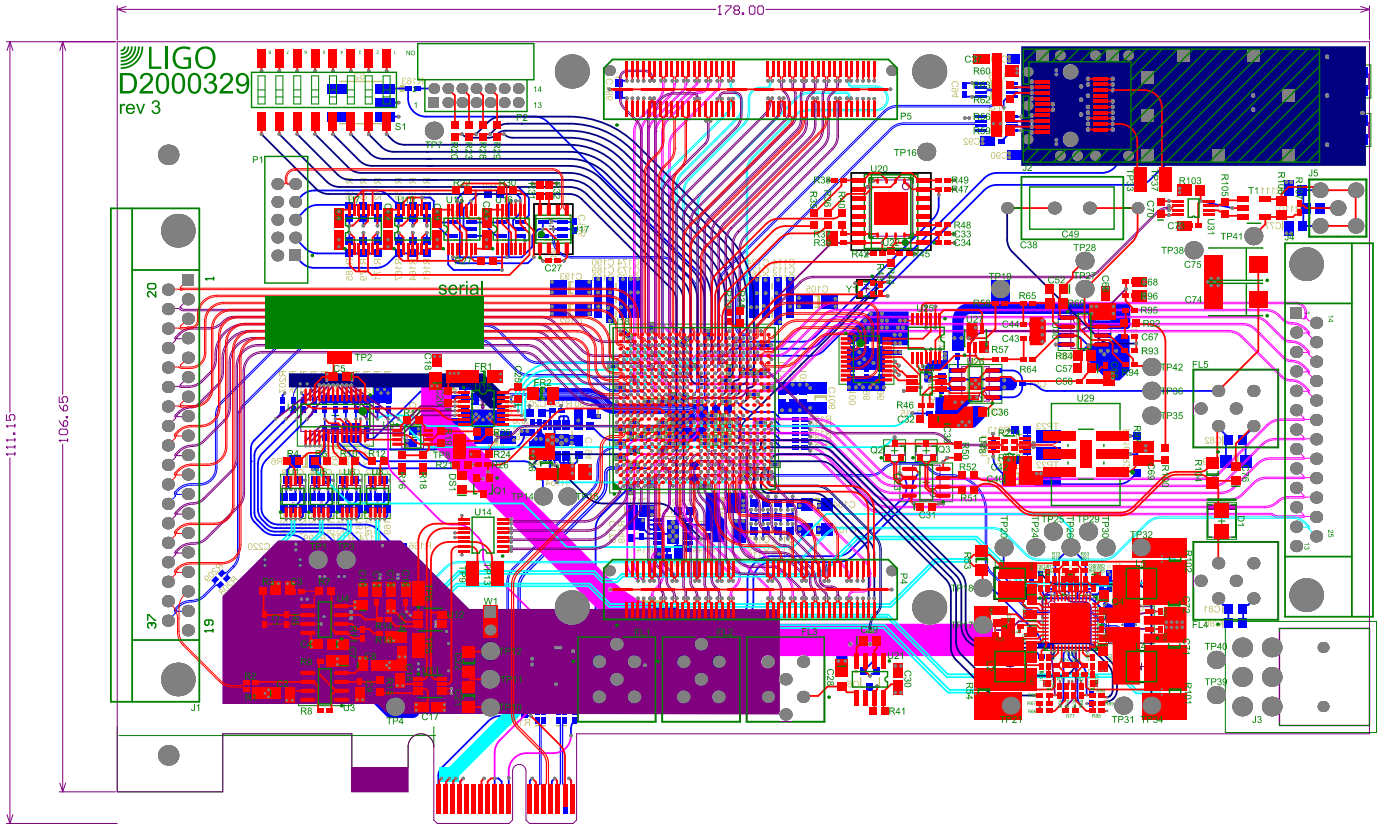
Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*PCIe Interface*		
Size: B-C-D	DCC D2000329	Rev: 3	
Date: 9/2/2025	Time: 3:43:51 PM	Sheet: 11 of 12	*DrawnBy: M. Pirello*
File: PCIe_Duotone_PCIE_HL.SchDoc			





Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*PCIe*		
Size: B-C-D	DCC D2000329	Rev: 3	
Date: 9/2/2025 Time: 3:43:51 PM		Sheet: 12 of 12	*DrawnBy: M. Pirello*
File: PCIe_Duotone_PCIE.SchDoc			



Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	SM-001	1.00mil	4
	Top Surface Finish	PbSn	0.79mil	
1	Top Layer	CF-004	1.38mil	
	Dielectric 1	PP-006	3.00mil	3.87
	Dielectric 2	PP-006	3.00mil	3.87
2	Int1 (GND)	CF-004	0.69mil	
	Dielectric 3	Core-016	5.00mil	4.1
3	Int2 (Sign)	CF-004	0.69mil	
	Dielectric 4	PP-006	3.50mil	4.1
	Dielectric 5	PP-006	3.50mil	4.1
4	Int3 (Sign)	CF-004	0.69mil	
	Dielectric 6	Core-016	4.00mil	4.1
5	Int4 (PWR)	CF-004	0.69mil	
	Dielectric 7	PP-006	2.85mil	3.87
	Dielectric 8	PP-006	2.85mil	3.87
6	Int5 (GND)	CF-004	0.69mil	
	Dielectric 9	Core-016	4.00mil	4.1
7	Int6 (Sign)	CF-004	0.69mil	
	Dielectric 10	PP-006	3.50mil	4.1
	Dielectric 11	PP-006	3.50mil	4.1
8	Int7 (Sign)	CF-004	0.69mil	
	Dielectric 12	Core-016	5.00mil	4.1
9	Int8 (GND)	CF-004	0.69mil	
	Dielectric 13	PP-006	3.00mil	3.87
	Dielectric 14	PP-006	3.00mil	3.87
10	Bottom Layer	CF-004	1.38mil	
	Bottom Surface Finish	PbSn	0.79mil	
	Bottom Solder	SM-001	1.00mil	4
	Bottom Overlay			
Total board thickness:			61.54mil	