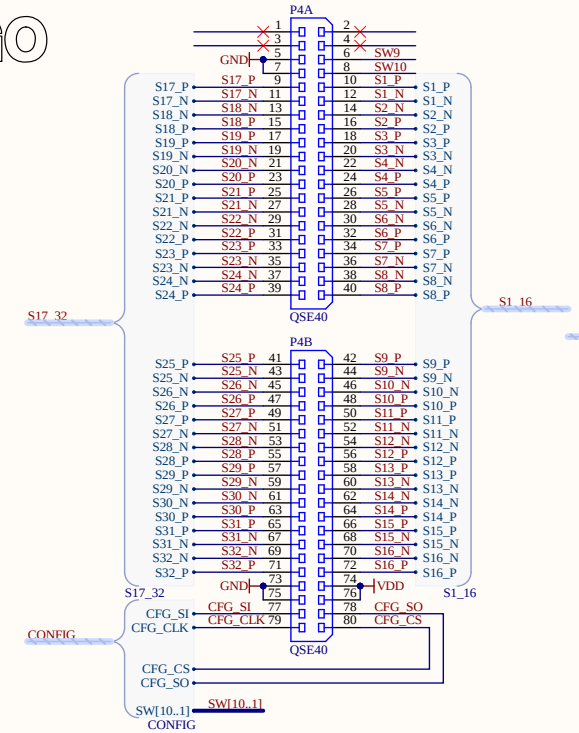
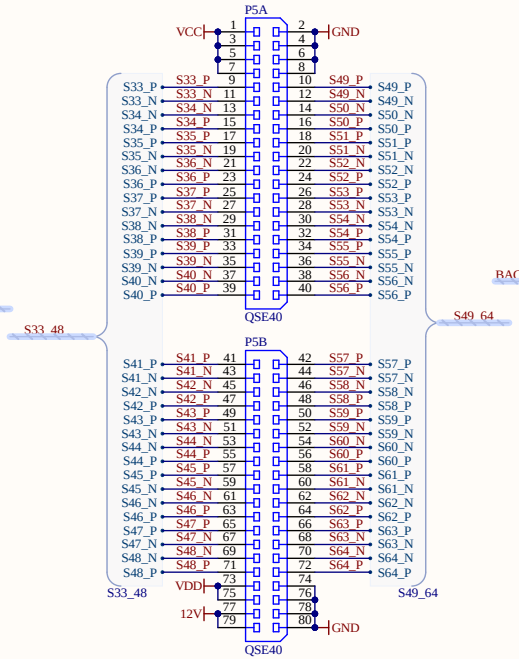
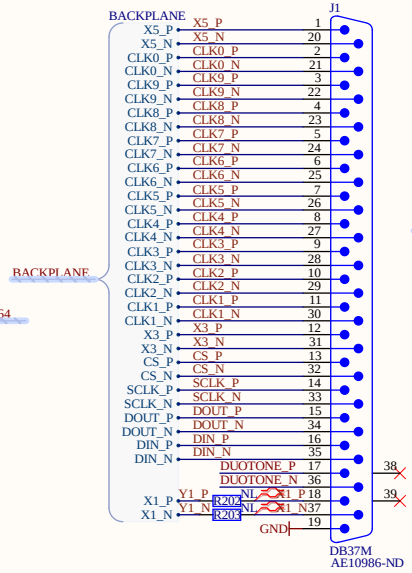
Samtec Expansion Port

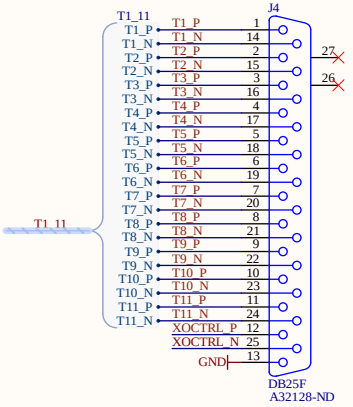


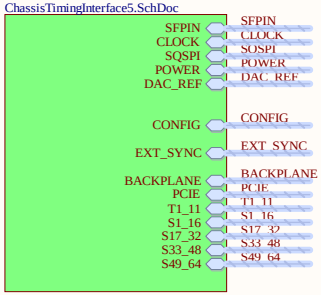


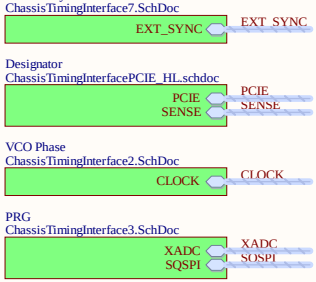
Duotone & Binary IO

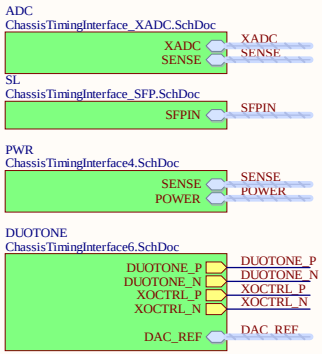


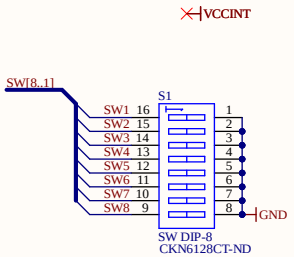
Rear DB25



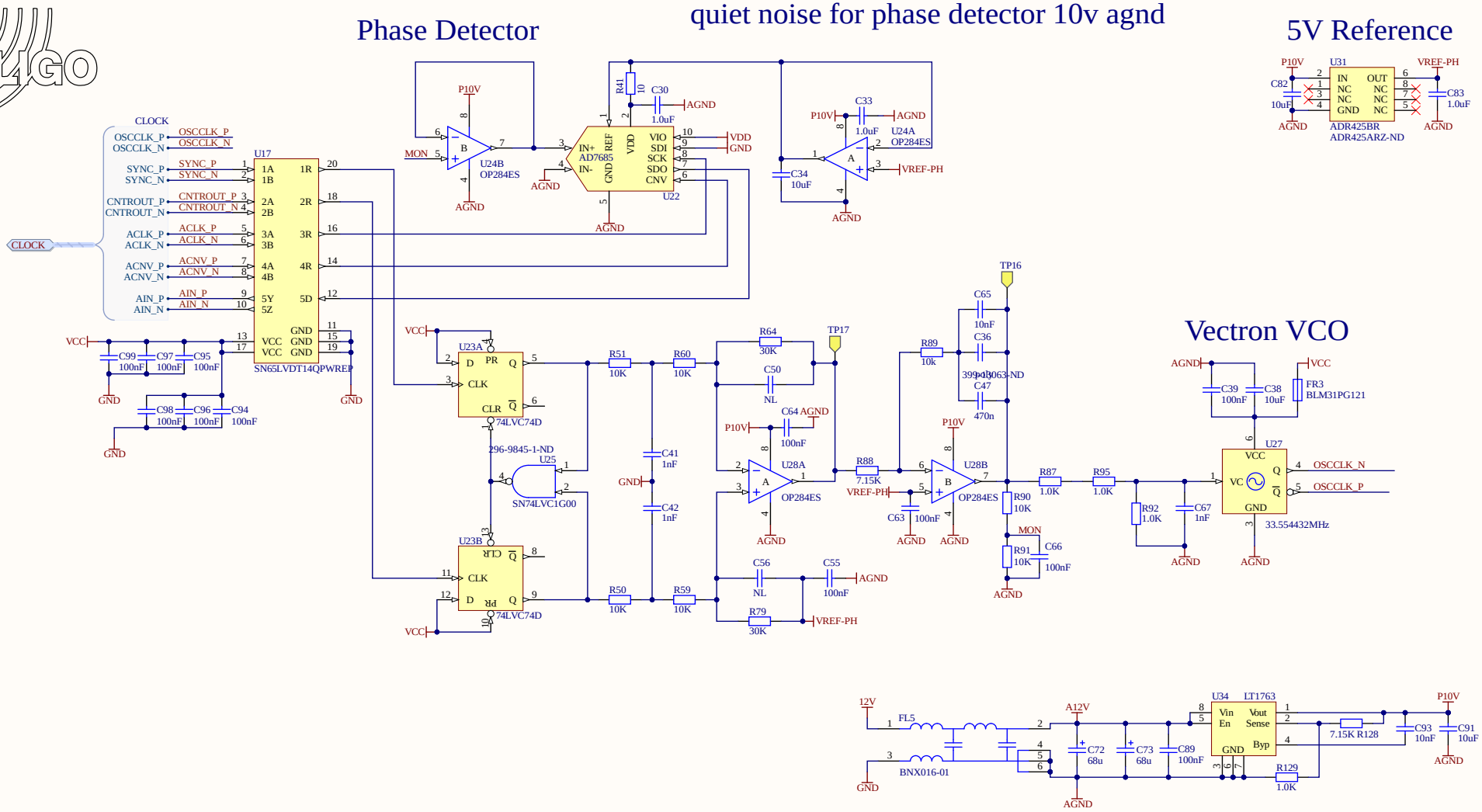




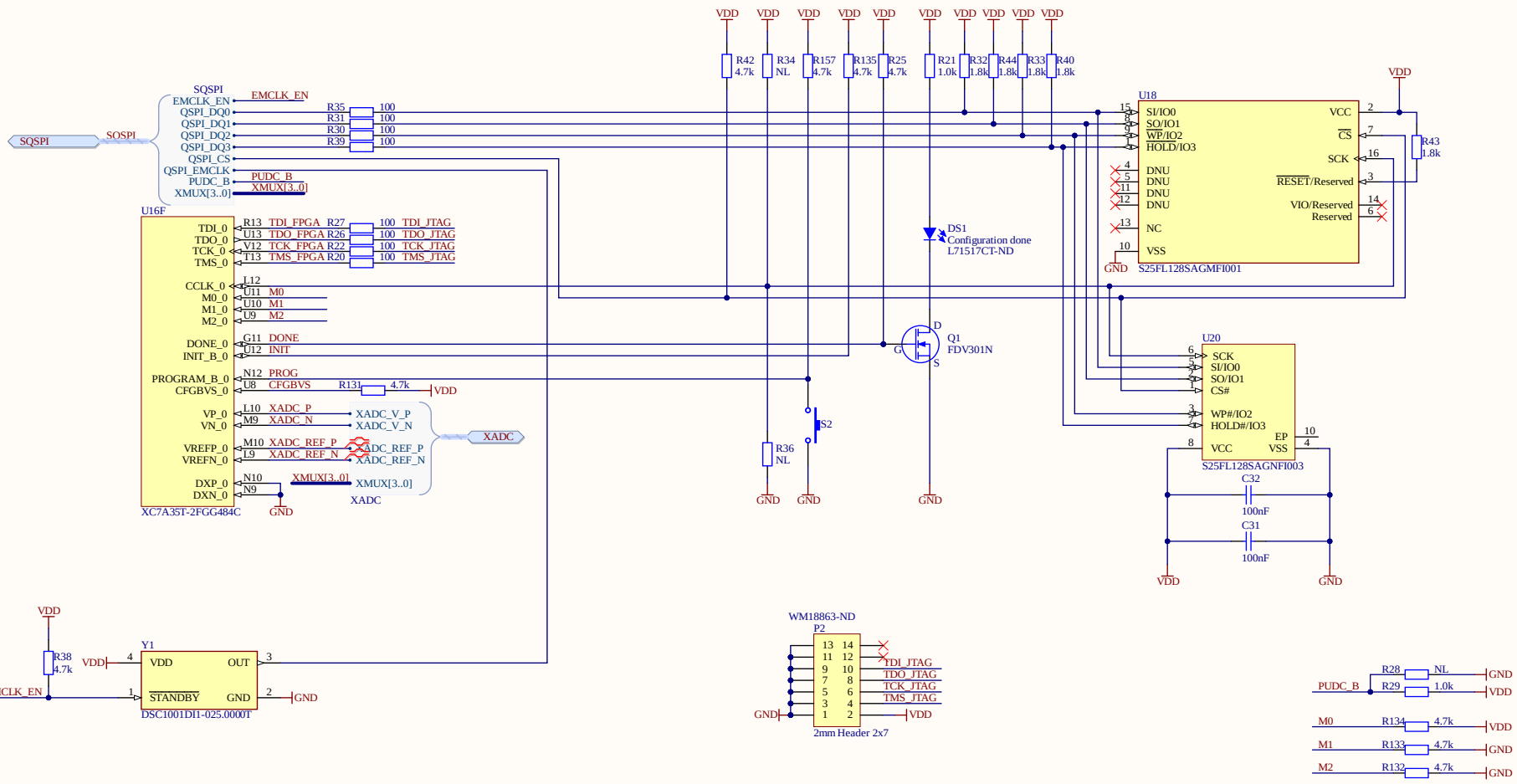




Project	PCIe Timing Interface		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	Timing Interface		
Size: B-C-D	DCC D2000329	Rev: 0	
Date: 8/28/2020	Time: 11:01:37 AM	Sheet: 1 of 12	DrawnBy: M. Pirello
File: ChassisTimingInterface1.SchDoc			

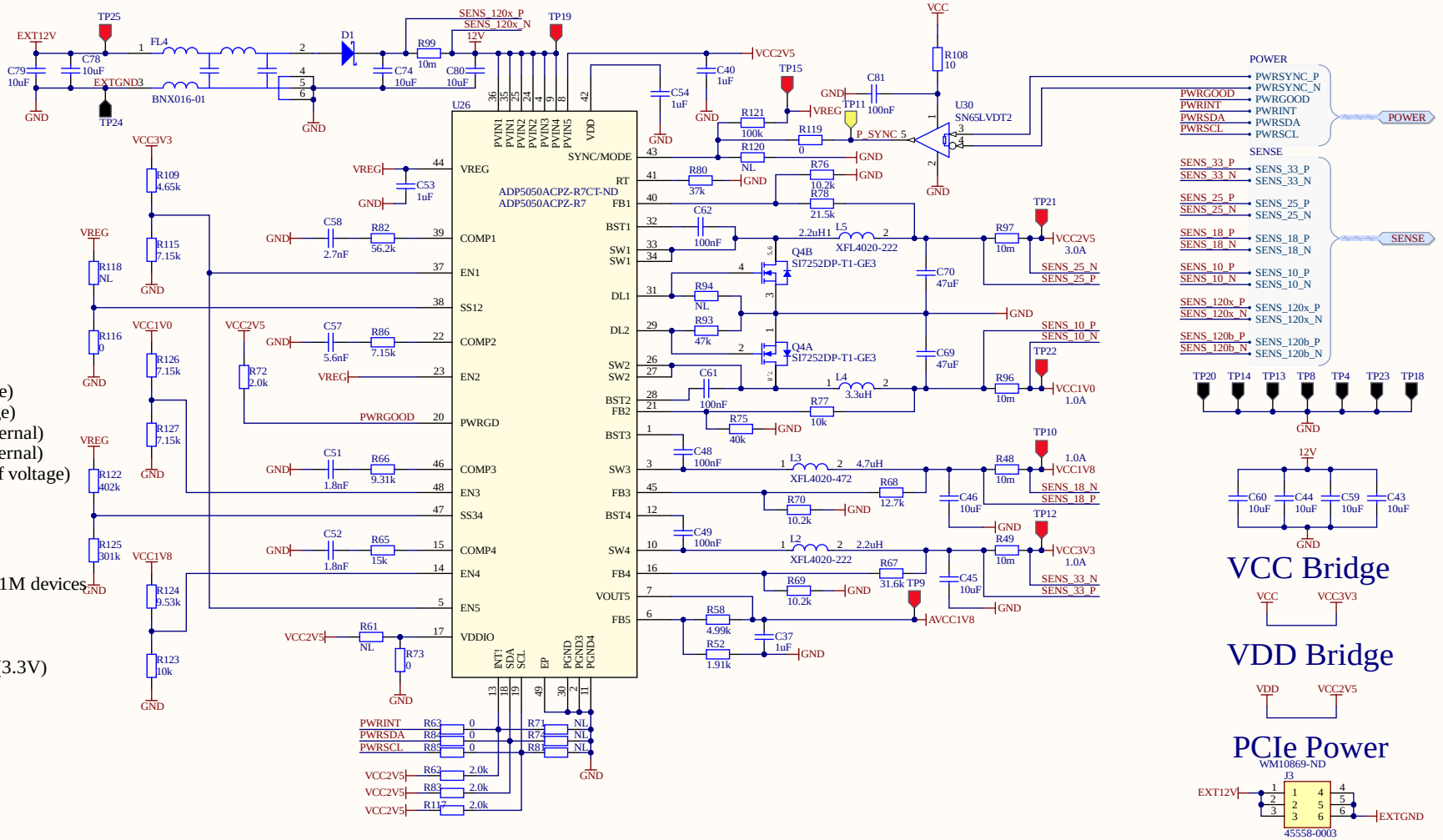

Phase Detector
quiet noise for phase detector 10v agnd
5V Reference
Vectron VCO
CLOCK
OSCCLK_P
OSCCLK_N
SYNC_P
SYNC_N
CNTROUT_P
CNTROUT_N
ACLK_P
ACLK_N
ACNV_P
ACNV_N
AIN_P
AIN_N
U17
SN65LVDT14QPWREP
U24B
OP284ES
U22
AD7685
U24A
U31
ADR425BR
ADR425ARZ-ND
U23A
U23B
74LVC74D
U25
SN74LVC1G00
296-9845-1-ND
U28A
U28B
TP16
TP17
U27
33.554432MHz
FR3
BLM31PG121
FL5
BNX016-01
U34
LT1763
7.15K R128
P10V
VCC
VDD
GND
AGND
VREF-PH
MON
A12V
12V
Project PCIe Timing Interface
Sheet Title VCO & Phase Detector
Size: B-C-D
DCC D2000329
Rev: 0
Date: 8/28/2020
Time: 11:01:38 AM
Sheet: 2 of 12
File: ChassisTimingInterface2.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello

JTAG and SPI Flash



Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*JTAG & SPI Flash*		
Size: B-C-D	DCC D2000329	Rev: 0	
Date: 8/28/2020	Time: 11:01:39 AM	Sheet: 3 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface3.SchDoc			

Switched FPGA Power

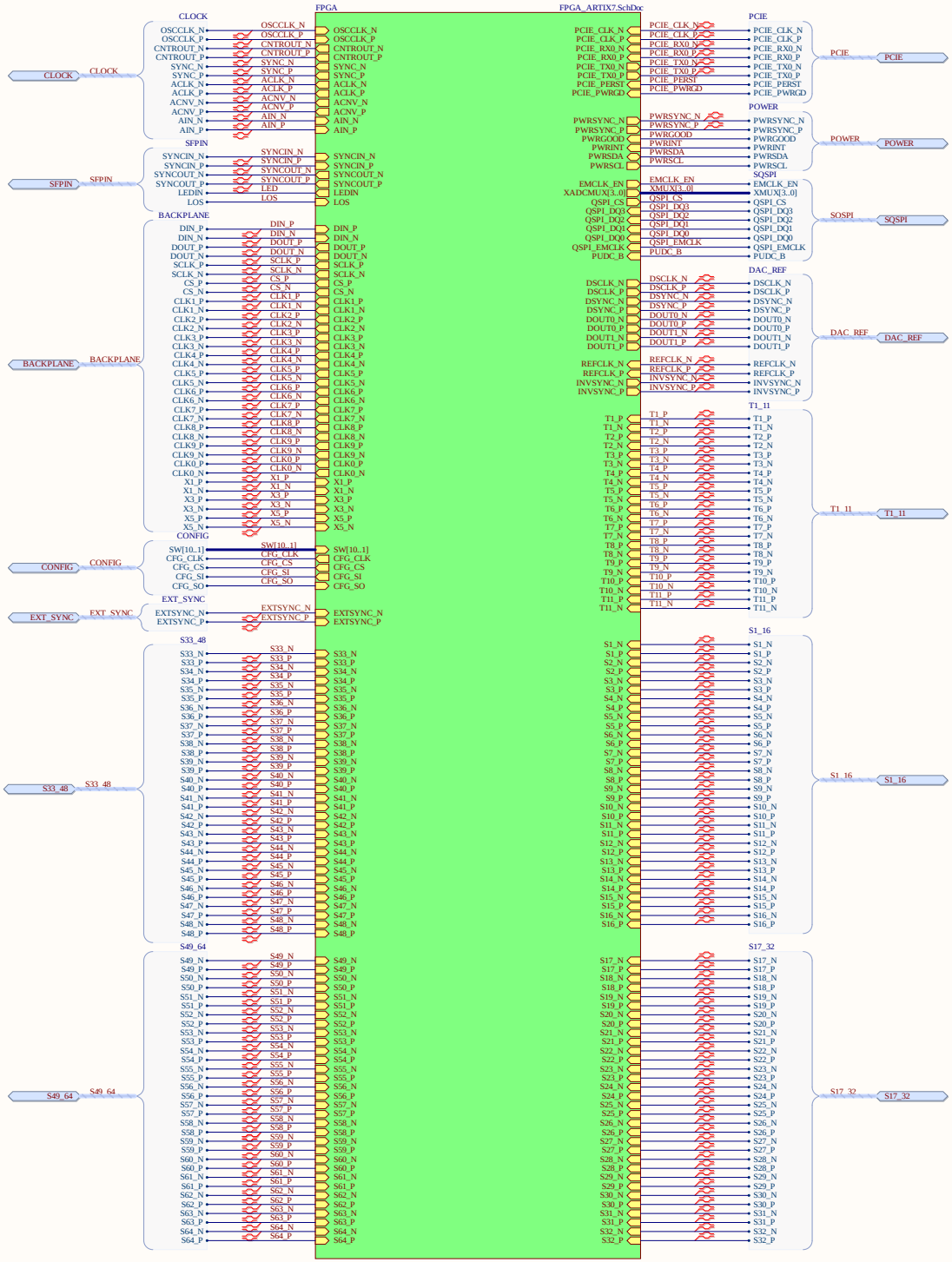


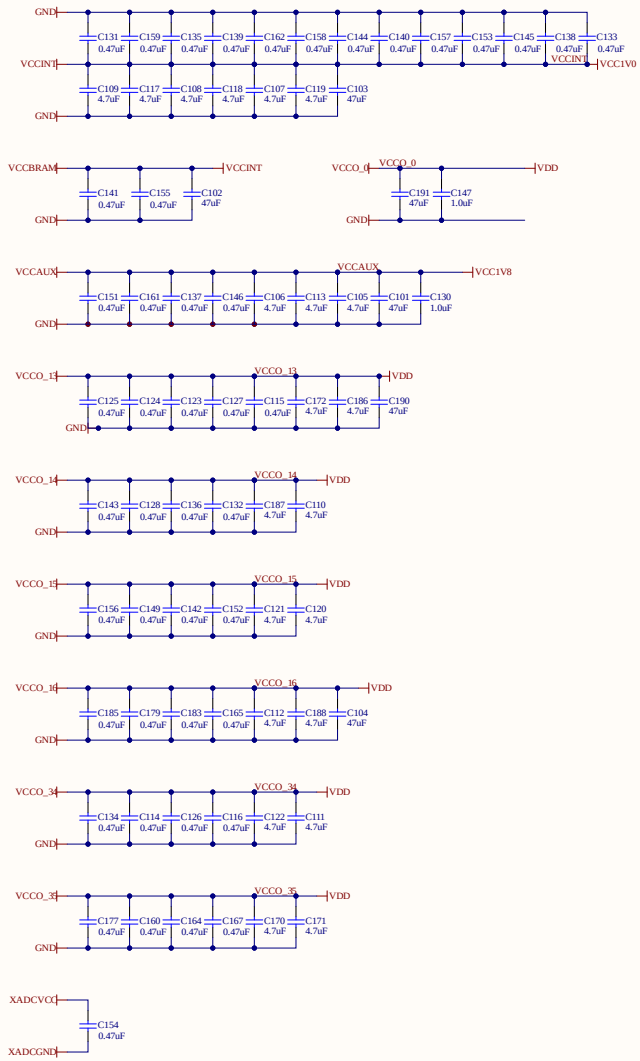
Voltage Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V

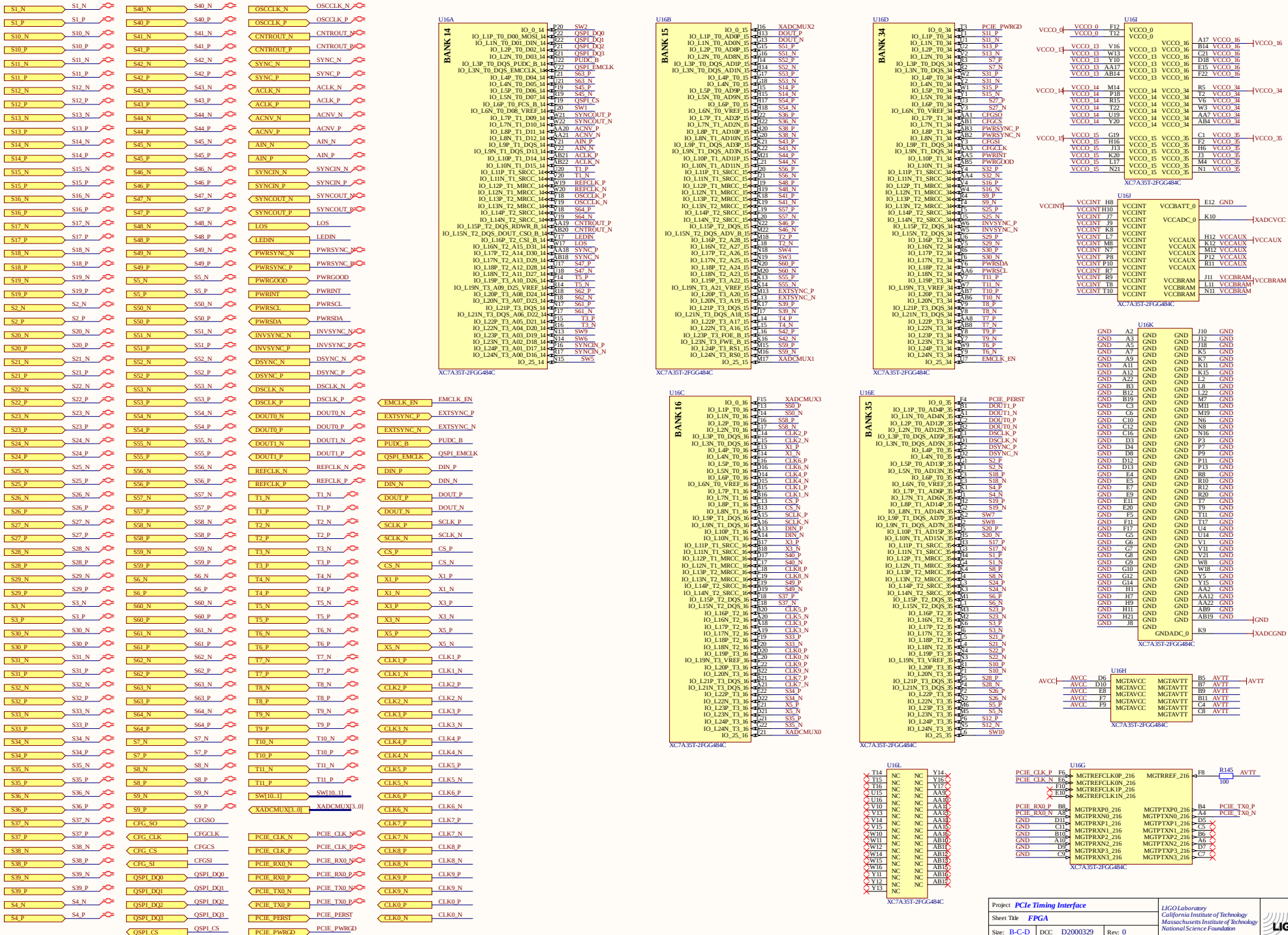
LVDS DC Specification
VCCO = 2.5
VOH = 1.675V
VOL = 0.7V

Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Power Supply*		
Size: B-C-D	DCC D2000329	Rev: 0	
Date: 8/28/2020	Time: 11:01:39 AM	Sheet: 4 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface4.SchDoc			





Project	PCIe Timing Interface		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	FPGA Interface		
Size: B-C-D	DCC D2000329	Rev: 0	
Date: 8/28/2020	Time: 11:01:40 AM	Sheet: 5 of 12	DrawnBy: M. Pirello
File: ChassisTimingInterface5.SchDoc			


S1_N
S1_P
S10_N
S10_P
S11_N
S11_P
S12_N
S12_P
S13_N
S13_P
S14_N
S14_P
S15_N
S15_P
S16_N
S16_P
S17_N
S17_P
S18_N
S18_P
S19_N
S19_P
S2_N
S2_P
S20_N
S20_P
S21_N
S21_P
S22_N
S22_P
S23_N
S23_P
S24_N
S24_P
S25_N
S25_P
S26_N
S26_P
S27_N
S27_P
S28_N
S28_P
S29_N
S29_P
S3_N
S3_P
S30_N
S30_P
S31_N
S31_P
S32_N
S32_P
S33_N
S33_P
S34_N
S34_P
S35_N
S35_P
S36_N
S36_P
S37_N
S37_P
S38_N
S38_P
S39_N
S39_P
S4_N
S4_P
S40_N
S40_P
S41_N
S41_P
S42_N
S42_P
S43_N
S43_P
S44_N
S44_P
S45_N
S45_P
S46_N
S46_P
S47_N
S47_P
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S61_N
S61_P
S62_N
S62_P
S63_N
S63_P
S64_N
S64_P
S7_N
S7_P
S8_N
S8_P
S9_N
S9_P
CFG_SO
CFG_CLK
CFG_CS
CFG_SI
QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
QSPI_CS
CFGSO
CFGCLK
CFGCS
CFGSI
QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
QSPI_CS
OSCCLK_N
OSCCLK_P
CNTROUT_N
CNTROUT_P
SYNC_N
SYNC_P
ACLK_N
ACLK_P
ACNV_N
ACNV_P
AIN_N
AIN_P
SYNCIN_N
SYNCIN_P
SYNCOUT_N
SYNCOUT_P
LOS
LEDIN
PWRSYNC_N
PWRSYNC_P
PWRGOOD
PWRINT
PWRSCL
PWRSDA
INVSYNC_N
INVSYNC_P
DSYNC_N
DSYNC_P
DSCLK_N
DSCLK_P
DOUT0_N
DOUT0_P
DOUT1_N
DOUT1_P
REFCLK_N
REFCLK_P
T1_N
T1_P
T2_N
T2_P
T3_N
T3_P
T4_N
T4_P
T5_N
T5_P
T6_N
T6_P
T7_N
T7_P
T8_N
T8_P
T9_N
T9_P
T10_N
T10_P
T11_N
T11_P
SW[10..1]
XADCMUX[3..0]
PCIE_CLK_N
PCIE_CLK_P
PCIE_RX0_N
PCIE_RX0_P
PCIE_TX0_N
PCIE_TX0_P
PCIE_PERST
PCIE_PWRGD
U16A
BANK 14
IO_0_14
IO_L1P_T0_D00_MOSI_14
IO_L1N_T0_D01_DIN_14
IO_L2P_T0_D02_14
IO_L2N_T0_D03_14
IO_L3P_T0_DQS_PUDC_B_14
IO_L3N_T0_DQS_EMCCLK_14
IO_L4P_T0_D04_14
IO_L4N_T0_D05_14
IO_L5P_T0_D06_14
IO_L5N_T0_D07_14
IO_L6P_T0_FCS_B_14
IO_L6N_T0_D08_VREF_14
IO_L7P_T1_D09_14
IO_L7N_T1_D10_14
IO_L8P_T1_D11_14
IO_L8N_T1_D12_14
IO_L9P_T1_DQS_14
IO_L9N_T1_DQS_D13_14
IO_L10P_T1_D14_14
IO_L10N_T1_D15_14
IO_L11P_T1_SRCC_14
IO_L11N_T1_SRCC_14
IO_L12P_T1_MRCC_14
IO_L12N_T1_MRCC_14
IO_L13P_T2_MRCC_14
IO_L13N_T2_MRCC_14
IO_L14P_T2_SRCC_14
IO_L14N_T2_SRCC_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L16P_T2_CSI_B_14
IO_L16N_T2_A15_D31_14
IO_L17P_T2_A14_D30_14
IO_L17N_T2_A13_D29_14
IO_L18P_T2_A12_D28_14
IO_L18N_T2_A11_D27_14
IO_L19P_T3_A10_D26_14
IO_L19N_T3_A09_D25_VREF_14
IO_L20P_T3_A08_D24_14
IO_L20N_T3_A07_D23_14
IO_L21P_T3_DQS_14
IO_L21N_T3_DQS_A06_D22_14
IO_L22P_T3_A05_D21_14
IO_L22N_T3_A04_D20_14
IO_L23P_T3_A03_D19_14
IO_L23N_T3_A02_D18_14
IO_L24P_T3_A01_D17_14
IO_L24N_T3_A00_D16_14
IO_25_14
SW2
QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
QSPI_EMCLK
S63_P
S63_N
S45_P
S45_N
QSPI_CS
SW1
SYNCOUT_P
SYNCOUT_N
ACNV_P
ACNV_N
AIN_P
AIN_N
ACLK_P
ACLK_N
T1_P
T1_N
REFCLK_P
REFCLK_N
S64_P
S64_N
CNTROUT_P
CNTROUT_N
T5_P
T5_N
S62_P
S62_N
S61_P
S61_N
SYNC_P
SYNC_N
OSCCLK_P
OSCCLK_N
LEDIN
LOS
SYNC_P
SYNC_N
S60_P
S60_N
S59_P
S59_N
S58_P
S58_N
S57_P
S57_N
S56_P
S56_N
S55_P
S55_N
S54_P
S54_N
S53_P
S53_N
DSCLK_P
DSCLK_N
DOUT0_P
DOUT0_N
DOUT1_P
DOUT1_N
INVSYNC_P
INVSYNC_N
S52_P
S52_N
DSYNC_P
DSYNC_N
S51_P
S51_N
S50_P
S50_N
PWRSDA
PWRSCL
PWRINT
PWRGOOD
S49_P
S49_N
S48_P
S48_N
S47_P
S47_N
S46_P
S46_N
S45_P
S45_N
S44_P
S44_N
S43_P
S43_N
S42_P
S42_N
S41_P
S41_N
S40_P
S40_N
XC7A35T-2FGG484C
U16B
BANK 15
IO_0_15
IO_L1P_T0_AD0P_15
IO_L1N_T0_AD0N_15
IO_L2P_T0_AD1P_15
IO_L2N_T0_AD8N_15
IO_L3P_T0_DQS_AD1P_15
IO_L3N_T0_DQS_AD1N_15
IO_L4P_T0_15
IO_L4N_T0_15
IO_L5P_T0_AD9P_15
IO_L5N_T0_AD9N_15
IO_L6P_T0_15
IO_L6N_T0_VREF_15
IO_L7P_T1_AD2P_15
IO_L7N_T1_AD2N_15
IO_L8P_T1_AD10P_15
IO_L8N_T1_AD10N_15
IO_L9P_T1_DQS_AD3P_15
IO_L9N_T1_DQS_AD3N_15
IO_L10P_T1_AD11P_15
IO_L10N_T1_AD11N_15
IO_L11P_T1_SRCC_15
IO_L11N_T1_SRCC_15
IO_L12P_T1_MRCC_15
IO_L12N_T1_MRCC_15
IO_L13P_T2_MRCC_15
IO_L13N_T2_MRCC_15
IO_L14P_T2_SRCC_15
IO_L14N_T2_SRCC_15
IO_L15P_T2_DQS_15
IO_L15N_T2_DQS_ADV_B_15
IO_L16P_T2_A28_15
IO_L16N_T2_A27_15
IO_L17P_T2_A26_15
IO_L17N_T2_A25_15
IO_L18P_T2_A24_15
IO_L18N_T2_A23_15
IO_L19P_T3_A22_15
IO_L19N_T3_A21_VREF_15
IO_L20P_T3_A20_15
IO_L20N_T3_A19_15
IO_L21P_T3_DQS_15
IO_L21N_T3_DQS_A18_15
IO_L22P_T3_A17_15
IO_L22N_T3_A16_15
IO_L23P_T3_FOE_B_15
IO_L23N_T3_FWE_B_15
IO_L24P_T3_RS1_15
IO_L24N_T3_RS0_15
IO_25_15
SW4
SW3
S60_P
S60_N
T5_P
T5_N
S62_N
S62_P
S61_N
S61_P
S64_P
S64_N
S63_P
S63_N
S58_P
S58_N
S57_P
S57_N
S56_P
S56_N
S55_P
S55_N
S54_P
S54_N
S53_P
S53_N
S52_P
S52_N
S51_P
S51_N
S50_P
S50_N
S49_P
S49_N
S48_P
S48_N
S47_P
S47_N
S46_P
S46_N
S45_P
S45_N
S44_P
S44_N
S43_P
S43_N
S42_P
S42_N
S41_P
S41_N
S40_P
S40_N
XC7A35T-2FGG484C
U16C
BANK 16
IO_0_16
IO_L1P_T0_16
IO_L1N_T0_16
IO_L2P_T0_16
IO_L2N_T0_16
IO_L3P_T0_DQS_16
IO_L3N_T0_DQS_16
IO_L4P_T0_16
IO_L4N_T0_16
IO_L5P_T0_16
IO_L5N_T0_16
IO_L6P_T0_16
IO_L6N_T0_VREF_16
IO_L7P_T1_16
IO_L7N_T1_16
IO_L8P_T1_16
IO_L8N_T1_16
IO_L9P_T1_DQS_16
IO_L9N_T1_DQS_16
IO_L10P_T1_16
IO_L10N_T1_16
IO_L11P_T1_SRCC_16
IO_L11N_T1_SRCC_16
IO_L12P_T1_MRCC_16
IO_L12N_T1_MRCC_16
IO_L13P_T2_MRCC_16
IO_L13N_T2_MRCC_16
IO_L14P_T2_SRCC_16
IO_L14N_T2_SRCC_16
IO_L15P_T2_DQS_16
IO_L15N_T2_DQS_16
IO_L16P_T2_16
IO_L16N_T2_16
IO_L17P_T2_16
IO_L17N_T2_16
IO_L18P_T2_16
IO_L18N_T2_16
IO_L19P_T3_16
IO_L19N_T3_VREF_16
IO_L20P_T3_16
IO_L20N_T3_16
IO_L21P_T3_DQS_16
IO_L21N_T3_DQS_16
IO_L22P_T3_16
IO_L22N_T3_16
IO_L23P_T3_16
IO_L23N_T3_16
IO_L24P_T3_16
IO_L24N_T3_16
IO_25_16
EMCLK_EN
EXTSYNC_P
EXTSYNC_N
PUDC_B
QSPI_EMCLK
DIN_P
DIN_N
DOUT_P
DOUT_N
SCLK_P
SCLK_N
CS_P
CS_N
X1_P
X1_N
X3_P
X3_N
X5_P
X5_N
CLK1_P
CLK1_N
CLK2_P
CLK2_N
CLK3_P
CLK3_N
CLK4_P
CLK4_N
CLK5_P
CLK5_N
CLK6_P
CLK6_N
CLK7_P
CLK7_N
CLK8_P
CLK8_N
CLK9_P
CLK9_N
CLK0_P
CLK0_N
XC7A35T-2FGG484C
U16D
BANK 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
PCIE_PWRGD
S1_P
S1_N
S3_P
S3_N
PWRSYNC_P
PWRSYNC_N
CFGSI
CFGCLK
PWRINT
PWRGOOD
S32_P
S32_N
S16_P
S16_N
S9_P
S9_N
S25_P
S25_N
INVSYNC_P
INVSYNC_N
S29_P
S29_N
S30_P
S30_N
T8_P
T8_N
T7_P
T7_N
T11_P
T11_N
T10_P
T10_N
T8_P
T8_N
T9_P
T9_N
PWRSDA
PWRSCL
T6_P
T6_N
EMCLK_EN
XADCMUX1
XC7A35T-2FGG484C
U16E
BANK 35
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IO_L1P_T0_AD4P_35
IO_L1N_T0_AD4N_35
IO_L2P_T0_AD12P_35
IO_L2N_T0_AD12N_35
IO_L3P_T0_DQS_AD5P_35
IO_L3N_T0_DQS_AD5N_35
IO_L4P_T0_35
IO_L4N_T0_35
IO_L5P_T0_AD13P_35
IO_L5N_T0_AD13N_35
IO_L6P_T0_35
IO_L6N_T0_VREF_35
IO_L7P_T1_AD6P_35
IO_L7N_T1_AD6N_35
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IO_L8N_T1_AD14N_35
IO_L9P_T1_DQS_AD7P_35
IO_L9N_T1_DQS_AD7N_35
IO_L10P_T1_AD15P_35
IO_L10N_T1_AD15N_35
IO_L11P_T1_SRCC_35
IO_L11N_T1_SRCC_35
IO_L12P_T1_MRCC_35
IO_L12N_T1_MRCC_35
IO_L13P_T2_MRCC_35
IO_L13N_T2_MRCC_35
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IO_L17N_T2_35
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IO_L18N_T2_35
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IO_L19N_T3_VREF_35
IO_L20P_T3_35
IO_L20N_T3_35
IO_L21P_T3_DQS_35
IO_L21N_T3_DQS_35
IO_L22P_T3_35
IO_L22N_T3_35
IO_L23P_T3_35
IO_L23N_T3_35
IO_L24P_T3_35
IO_L24N_T3_35
IO_25_35
PCIE_PERST
DOUT1_P
DOUT1_N
DOUT0_P
DOUT0_N
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DSCLK_N
DSYNC_P
DSYNC_N
S2_P
S2_N
S18_P
S18_N
S4_P
S4_N
S19_P
S19_N
SW7
SW8
S20_P
S20_N
S17_P
S17_N
S1_P
S1_N
S8_P
S8_N
S24_P
S24_N
S6_P
S6_N
S23_P
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S3_P
S3_N
S21_P
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S22_P
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S28_N
S26_P
S26_N
S5_P
S5_N
S12_N
SW10
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VCCO_14
VCCO_15
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VCCINT
VCCBATT_0
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VCCAUX
VCCBRAM
GND
XADCVCC
XADCGND
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GND
XC7A35T-2FGG484C
U16H
AVCC
AVTT
XC7A35T-2FGG484C
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NC
XC7A35T-2FGG484C
U16G
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MGTREFCLK1P_216
MGTREFCLK1N_216
MGTRREF_216
MGTPRXP0_216
MGTPRXN0_216
MGTPRXP1_216
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PCIe Timing Interface
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DCC D2000329
Rev: 0
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Time: 11:01:42 AM
Sheet: 6 of 12
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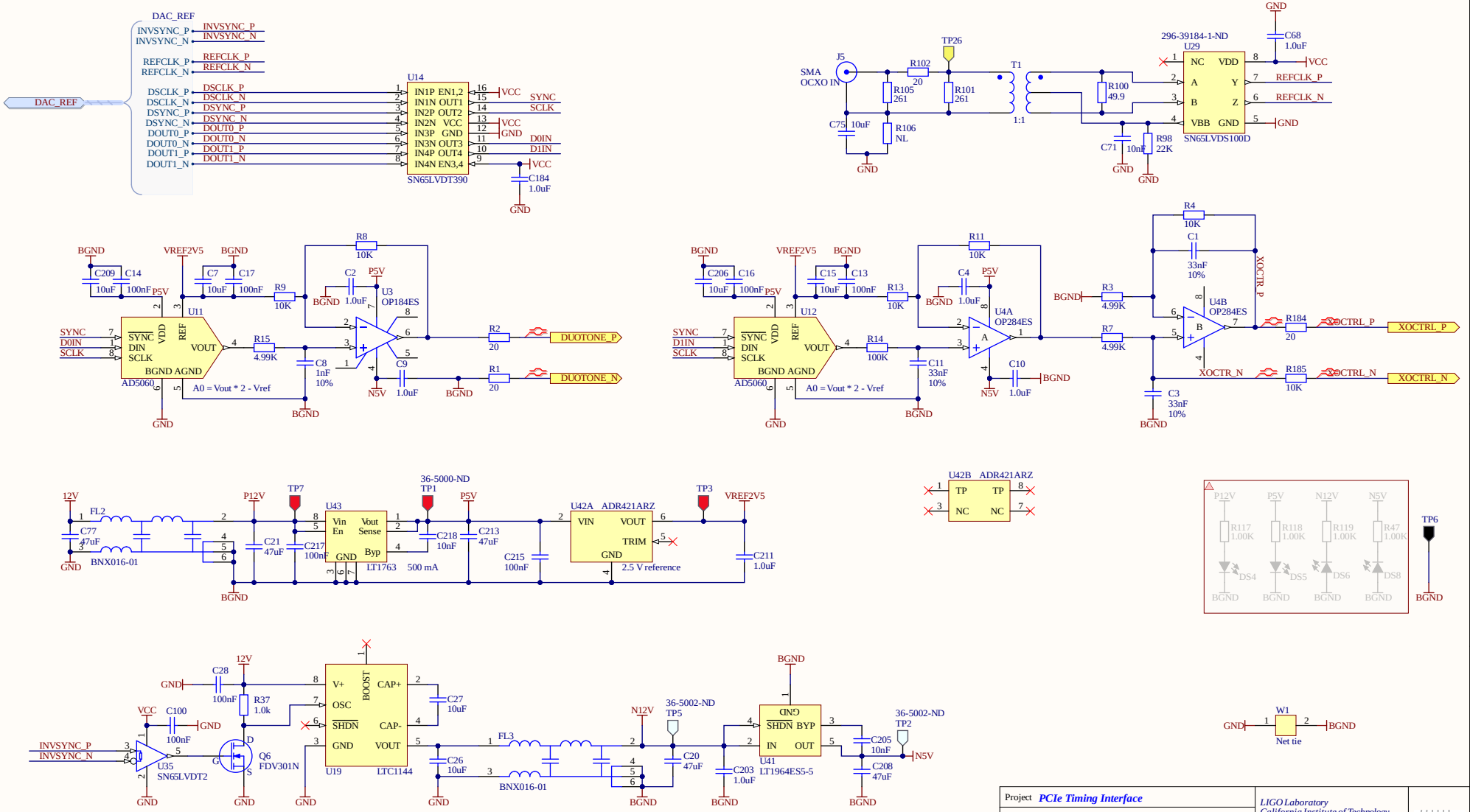
DrawnBy: M. Pirello
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
LIGO



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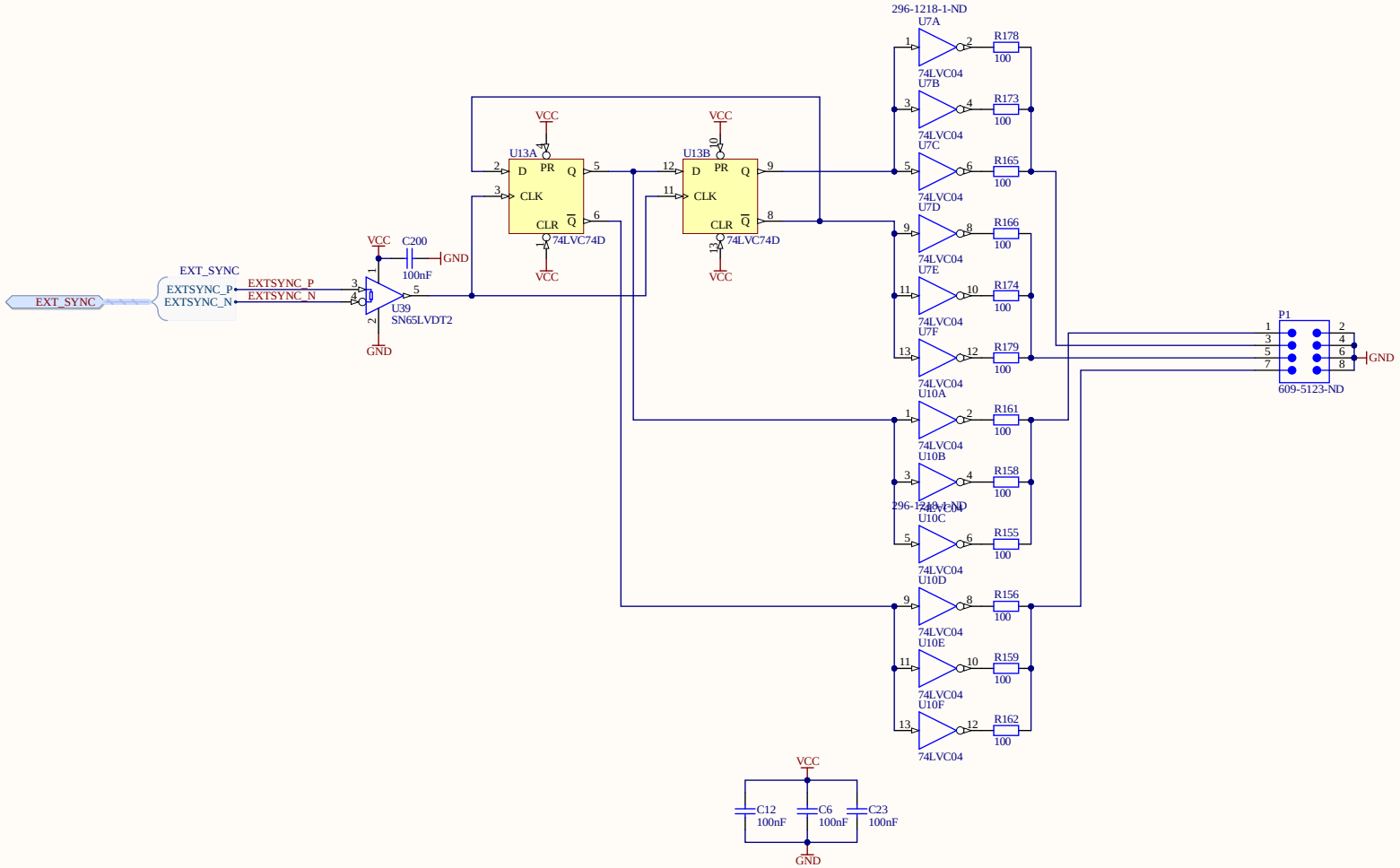

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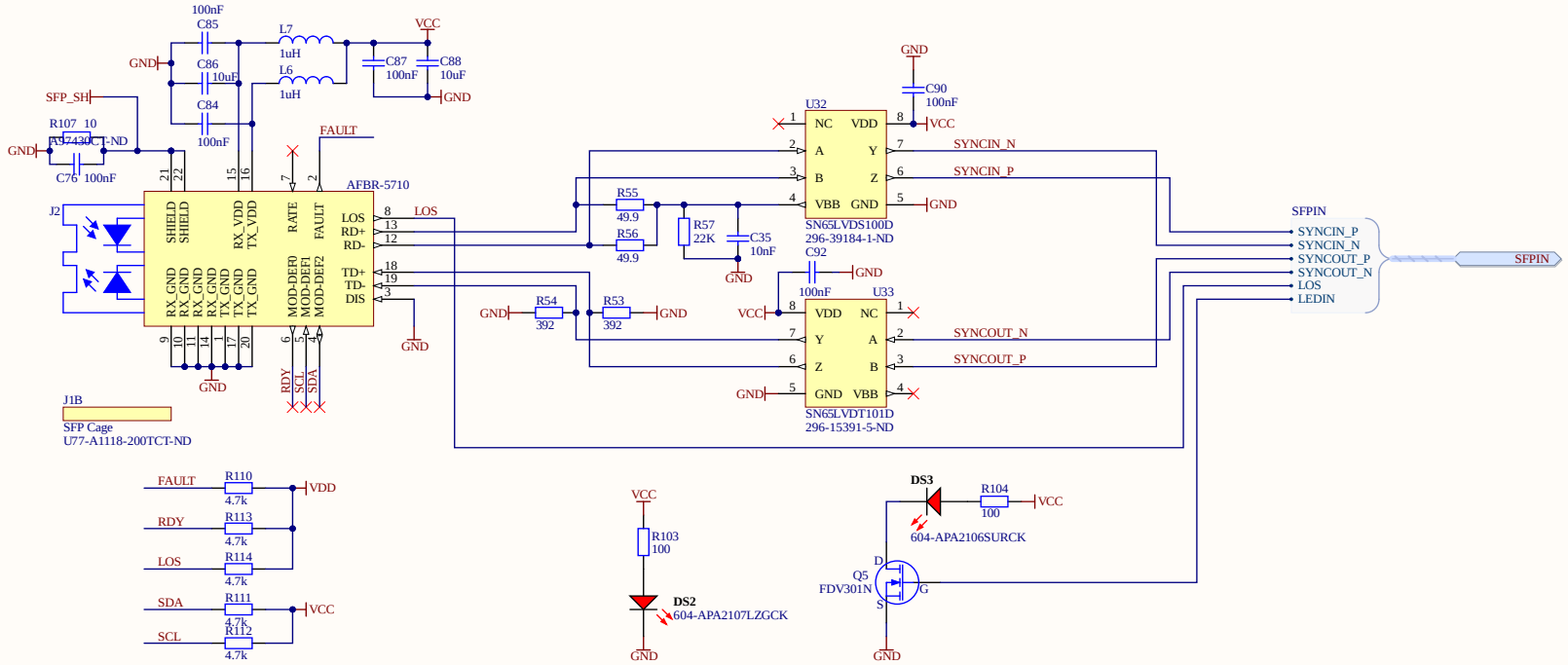
SFP Port



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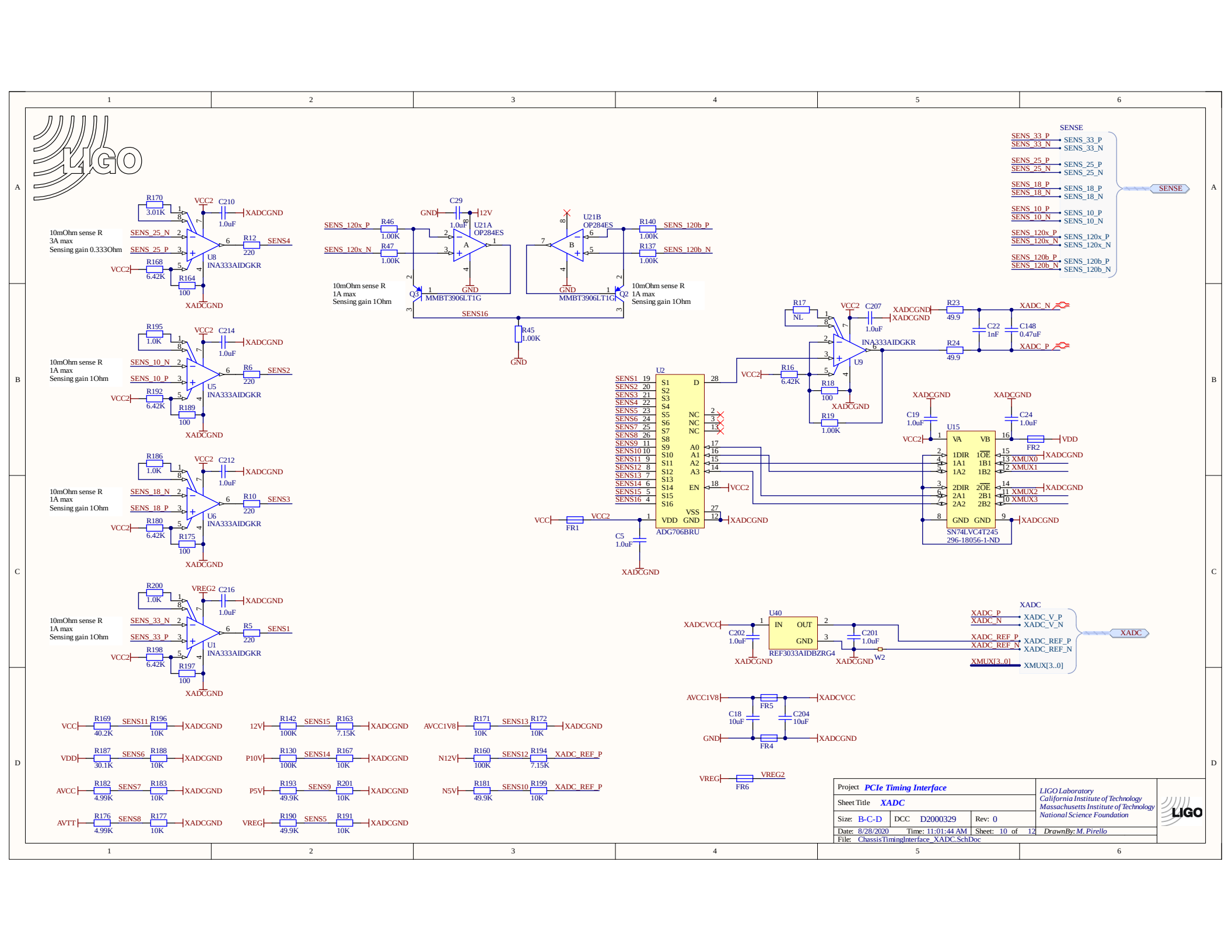
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SENS_10_P
SENS_10_N
SENS_120x_P
SENS_120x_N
SENS_120b_P
SENS_120b_N
10mOhm sense R
3A max
Sensing gain 0.333Ohm
10mOhm sense R
1A max
Sensing gain 1Ohm
SENS16
ADG706BRU
SN74LVC4T245
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INA333AIDGKR
MMBT3906LT1G
OP284ES
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XADC
XADCGND
VCC2
VREG2
12V
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VDD
AVCC
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DCC D2000329
Rev: 0
Date: 8/28/2020
Time: 11:01:44 AM
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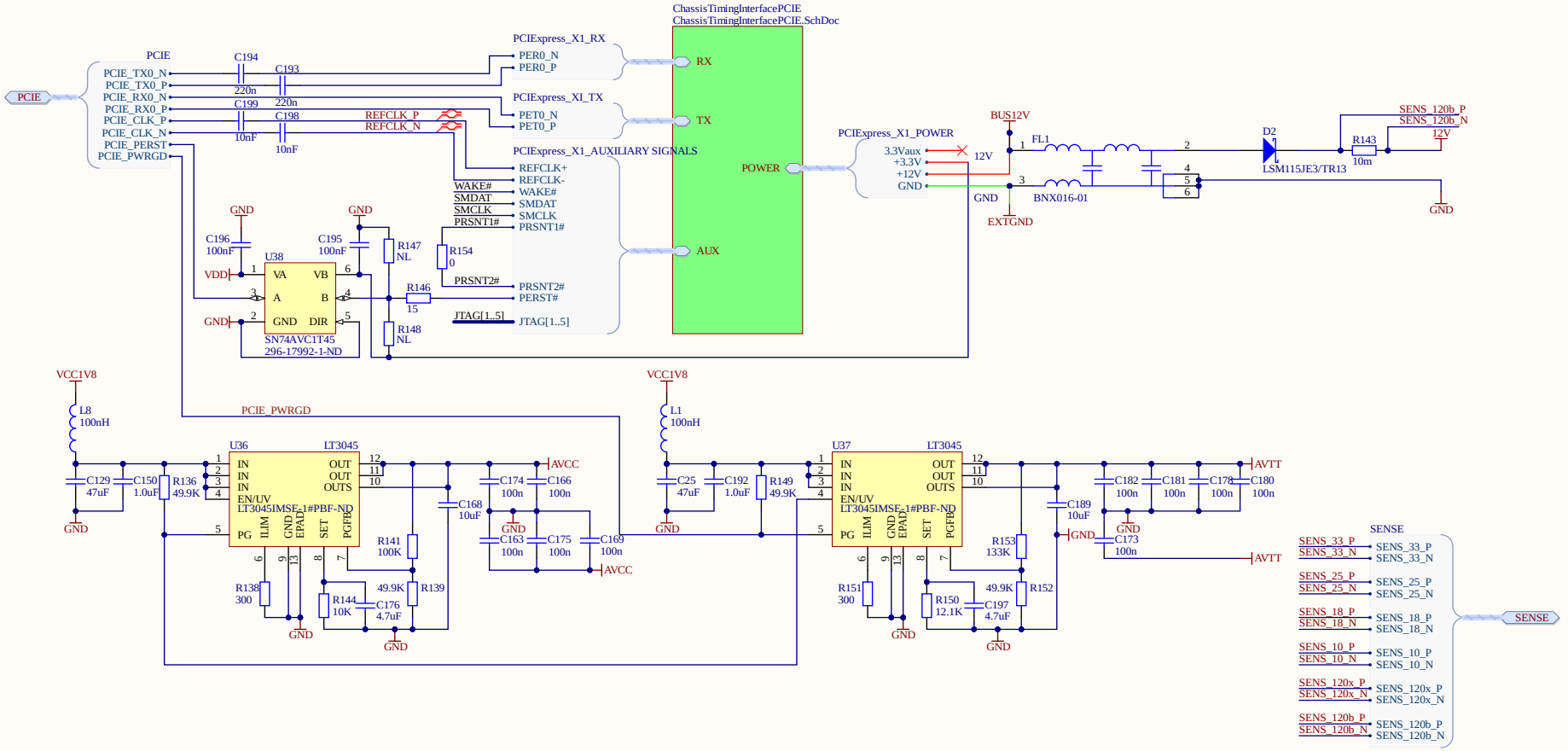
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello



- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*PCIe Interface*		
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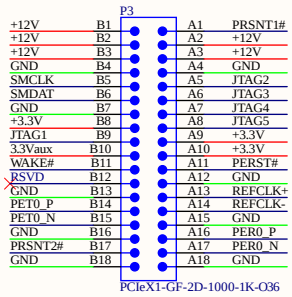

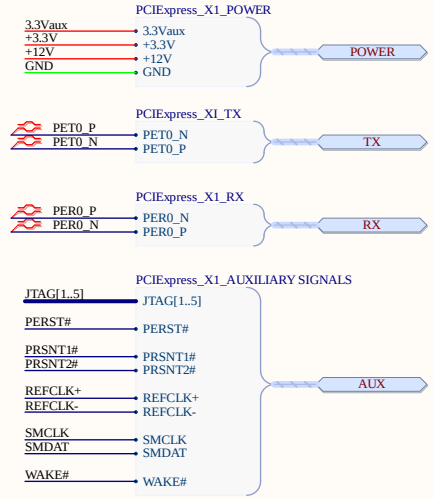

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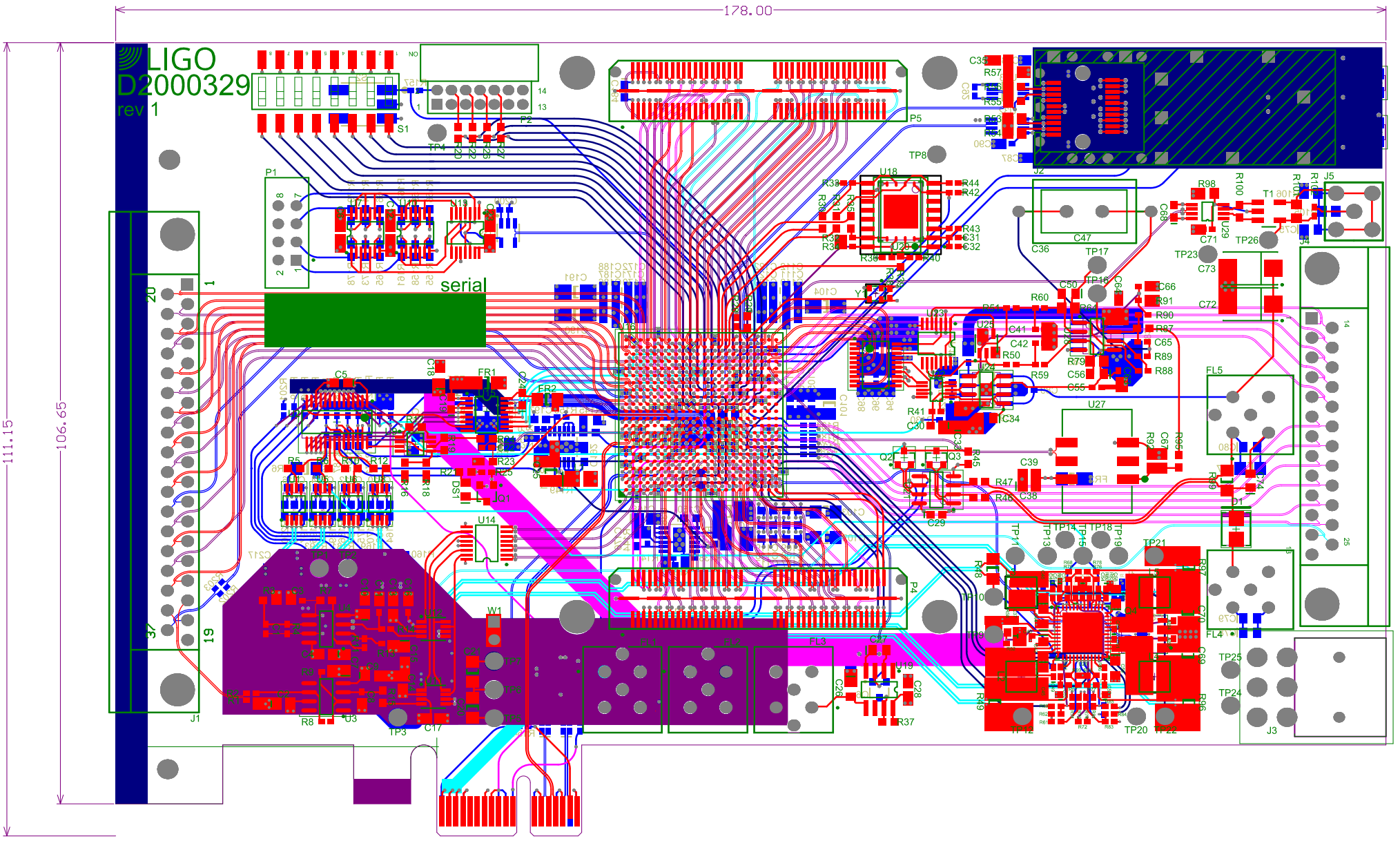
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rev 1
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