LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

LIGO Laboratory / LIGO Scientific Collaboration

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PCIe Timing Slave Implementation

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1 Introduction

This document will describe each aspect of the PCIe Timing Slave Implementation. The system was initially slated to replace the Timing Slave & Duotone currently installed in every IO chassis. This was expanded to incorporate CONTEC binary IO timing card replacement, 1PPS timing add on, additional SFP and a higher speed VCO.

2 Inputs & Outputs

2.1 Samtec Expansion Connector

We kept the legacy Samtec connector with the same spacing so that any old modules should work on the updated system. This allows for new modules as well.

2.2 SFP Master & SFP Slave

SFP Slave is essentially lifted from the prior board the Master is copied from this and should only be a difference in FPGA code to enable Master.

2.3 JTAG, SPI Flash, & USB

This section needs the most work, I am still looking for an example layout for the USB programming of this chip. JTAG and SPI function much the same as before, headers have not changed.

2.4 Power

The power input is 12V and the plug layout is the same as a PCIe external power connector you might find in a modern computer. The system can theoretically be powered from the PCIe bus, but I have left a provision for external power to reduce bus power consumption. This will be selected with a jumper on the final version.

2.5 Duotone

Duotone is handled exactly the same as before. The 40 pin header has not changed, other than the unnecessary signals were removed. After looking at the CONTEC configuration if we do redesign the backplane, we should include one 40 pin header to handle all of the signals and eliminate one of them. All of the required signals can be housed on one 40 pin IDC cable.

2.6 1PPS Locking

This section has a frequency input on SMA and an error signal output on LEMO.

2.7 CONTEC Binary IO

This section has a 40 pin IDC header same as what is on the existing backplane. We should consider merging these headers in any revised backplane. There are also 7 clock outputs located in this section which also route to the 40 pin IDC header.

2.8 PCIe Interface

This is a 1x PCIe interface and should be plenty fast enough for our needs.

3 Schematic Pages

3.1 ChassisTimingInterface1

Top Document, contains SAMTEC expansion connector along with the entry documents for each of the sub systems, to include FPGA Controls, VCO (Phase Detector), Duotone Output, Power System, Contec Binary IO Replacement, and 1PPS Timing.

3.2 ChassisTimingInterface2

VCO and Phase Detector. This section contains its own power system source from the 12V input voltage. This power is filtered and regulated down to 10V, and further referenced to 5V for the analog section. The ADC and supporting comparators adjust phase to align with the incoming 1pps from the FPGA. Both SFP top sheets are located here.

3.3 ChassisTimingInterface_SFP

SFP Master & Slave. Dual SFP port, generally unchanged from the previous version.

3.4 ChassisTimingInterface3

JTAG SPI Flash & US, contains easily sourced SPI memory module to program the FPGA. JTAG port and USB programmer located in this section.

3.5 ChassisTimingInterface4

FPGA Power Supply – Input is filtered 12V, output is 5V high Z reference, AVCC1V8 FPGA ADC Reference, VCC3V3 (VCC for the PCB), VCC1V8 FPGA internal voltage, VCC0V95 FPGA internal voltage, VCC2V5 for VDD & LVDS.

3.6 ChassisTimingInterface5

FPGA Caps and BUS Interface

3.7 FPGA_ARTIX7

FPGA BUS interface

3.8 ChassisTimingInterface6

Duotone – This section replicates the Duotone card from the previous system. The 40pin IDC header is laid out with the same signals.

3.9 ChassisTimingInterface7

1PPS Locking – This section has an OCXO input which is read into the FPGA and also has a OCXO control output which looks like an error signal for the OCXO and feed back to adjust the phase and frequency. There is also a TTL OK output.

3.10 ChassisTimingInterface8

Contec Binary IO – Contains 7 binary outputs which will be controlled by the FPGA, both SMA and UMCC. Also contains a 40 pin IDC header to maintain backward compatibly.

3.11 PCI Express_167651115_36PIN_Half length

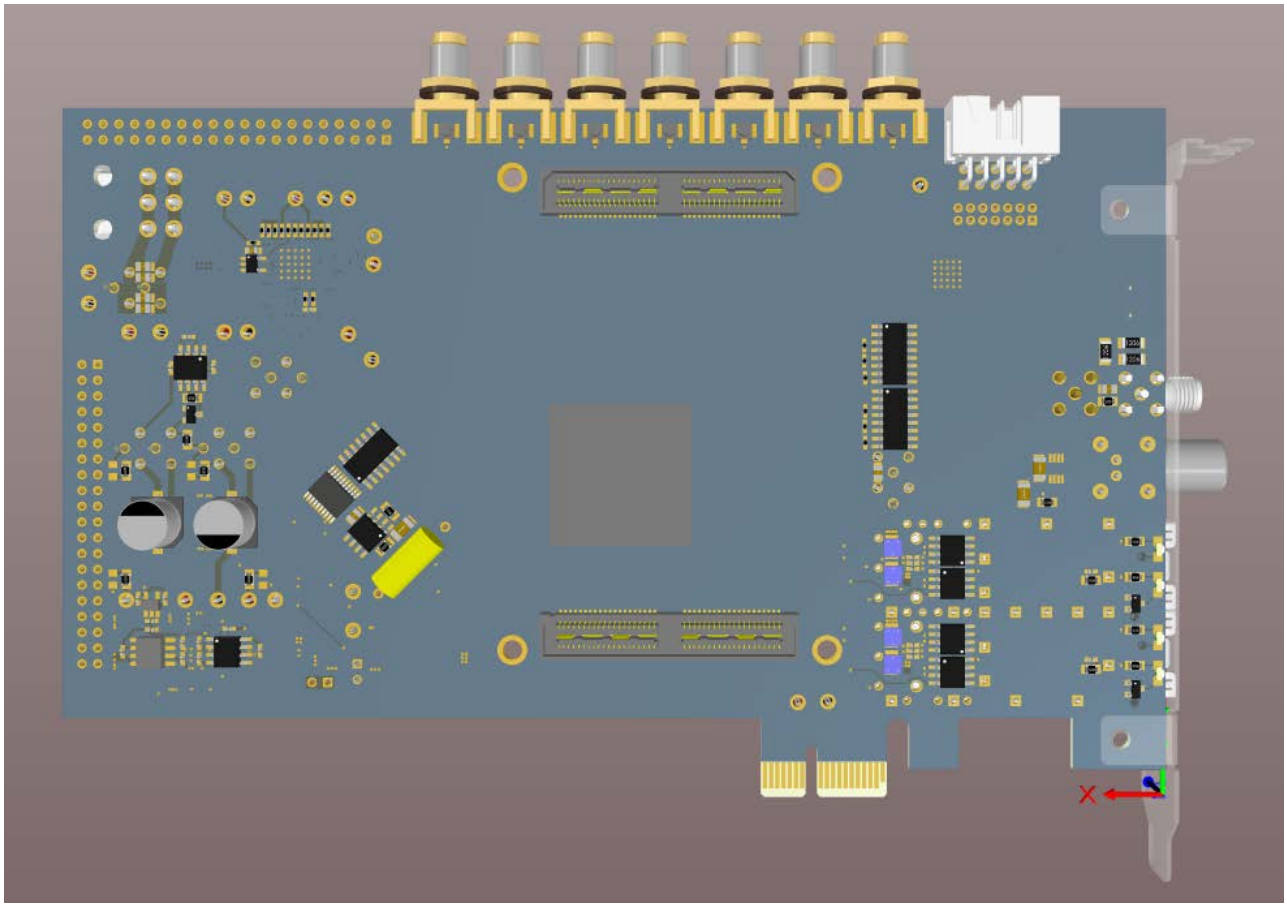
PCIe Interface – Premade PCIe interface from Altium.

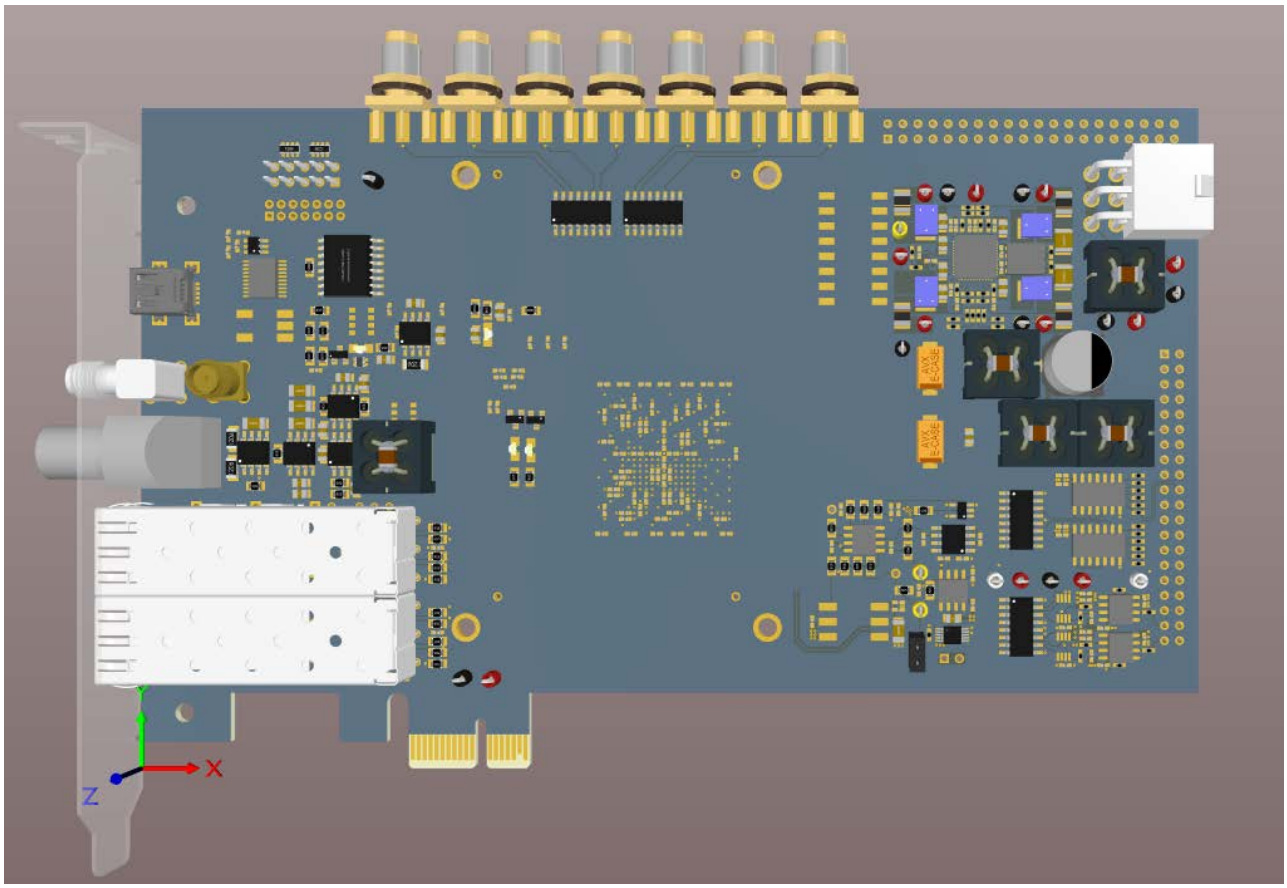
3.12 CON_PCI_Express_X1_36PIN

PCIe Interface – Premade PCIe interface from Altium.

3.13 PCB Document

Everything fits on the half-length PCIe card so far. Considering adding frequency counters to the layout and consolidating 40 pin IDC headers.

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