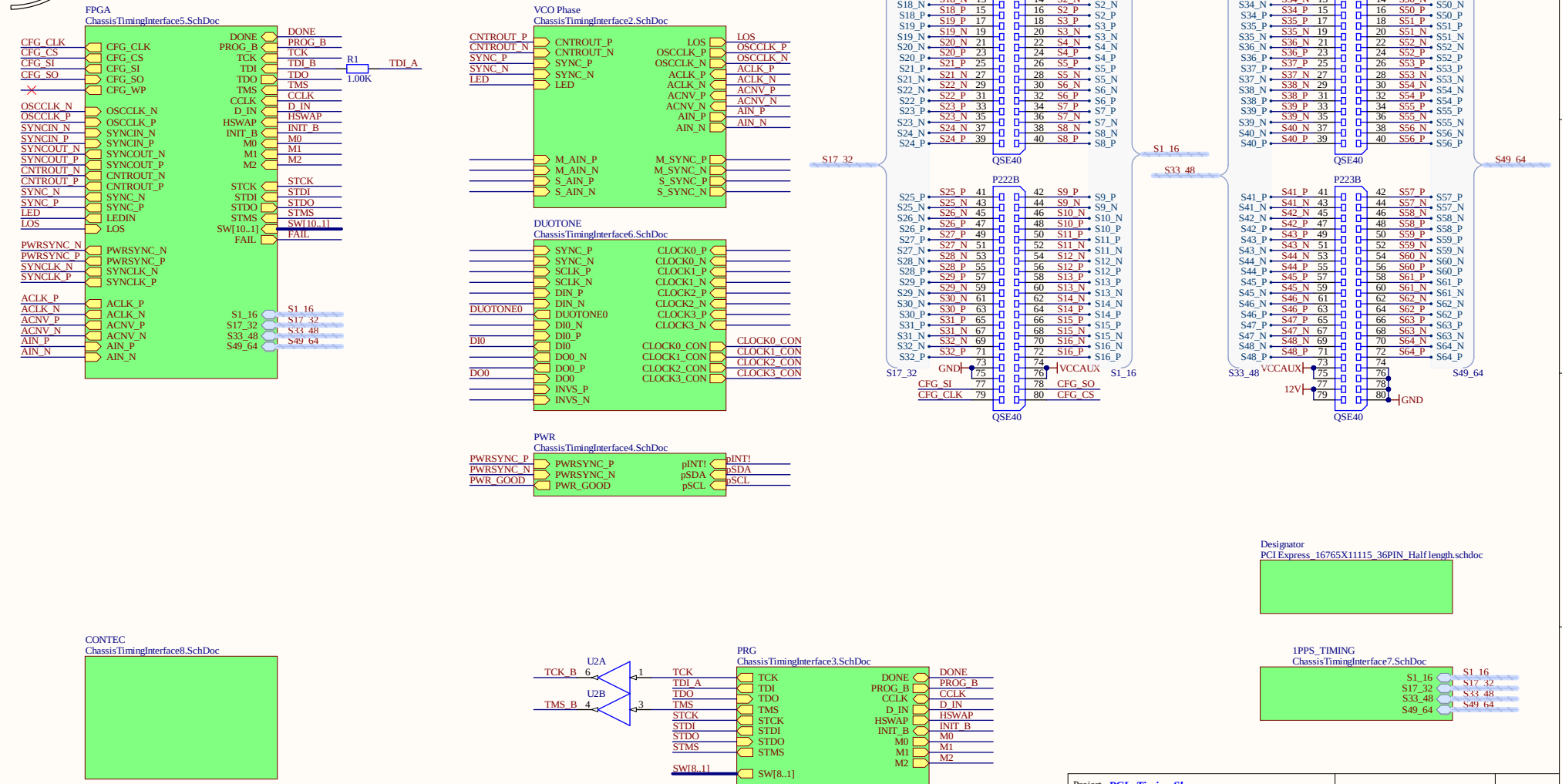
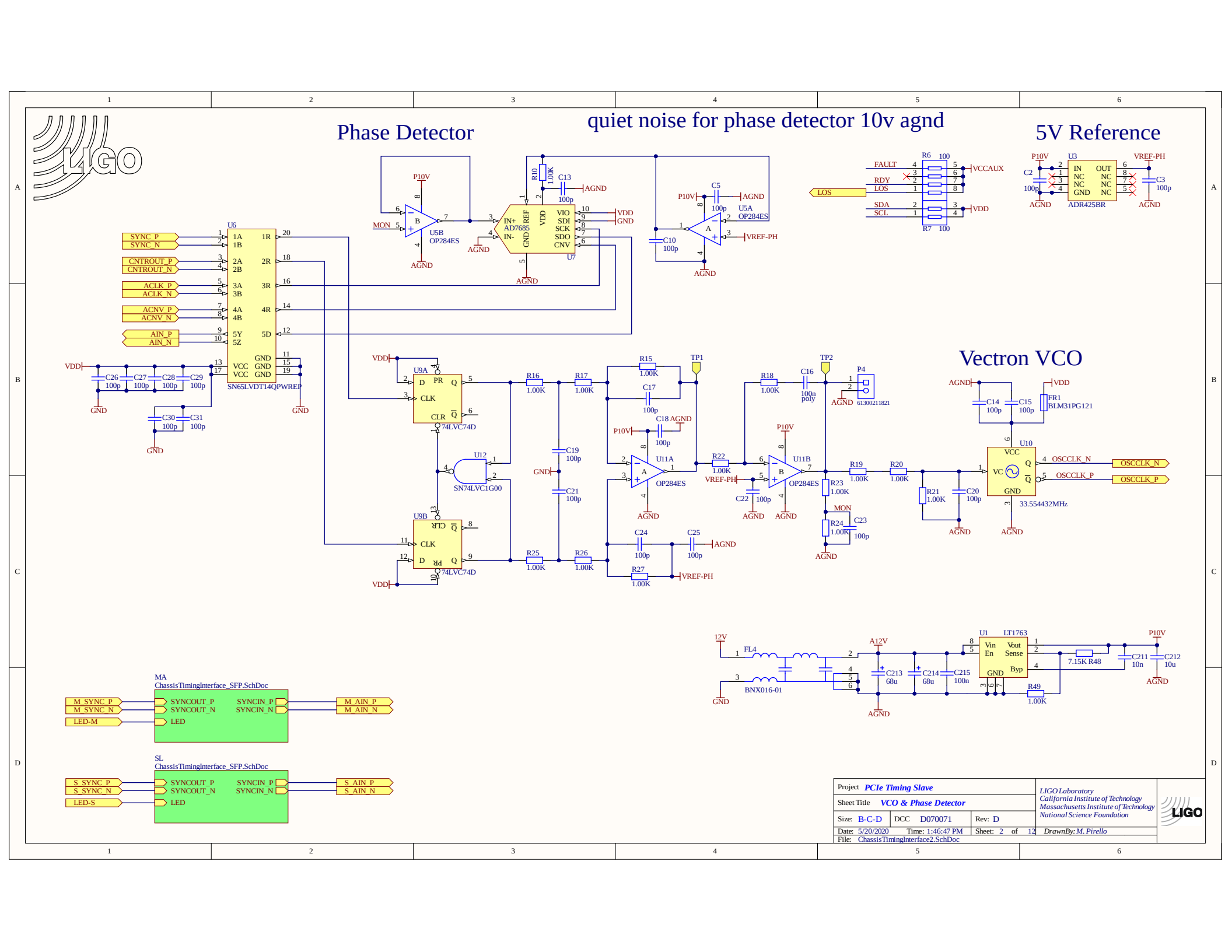
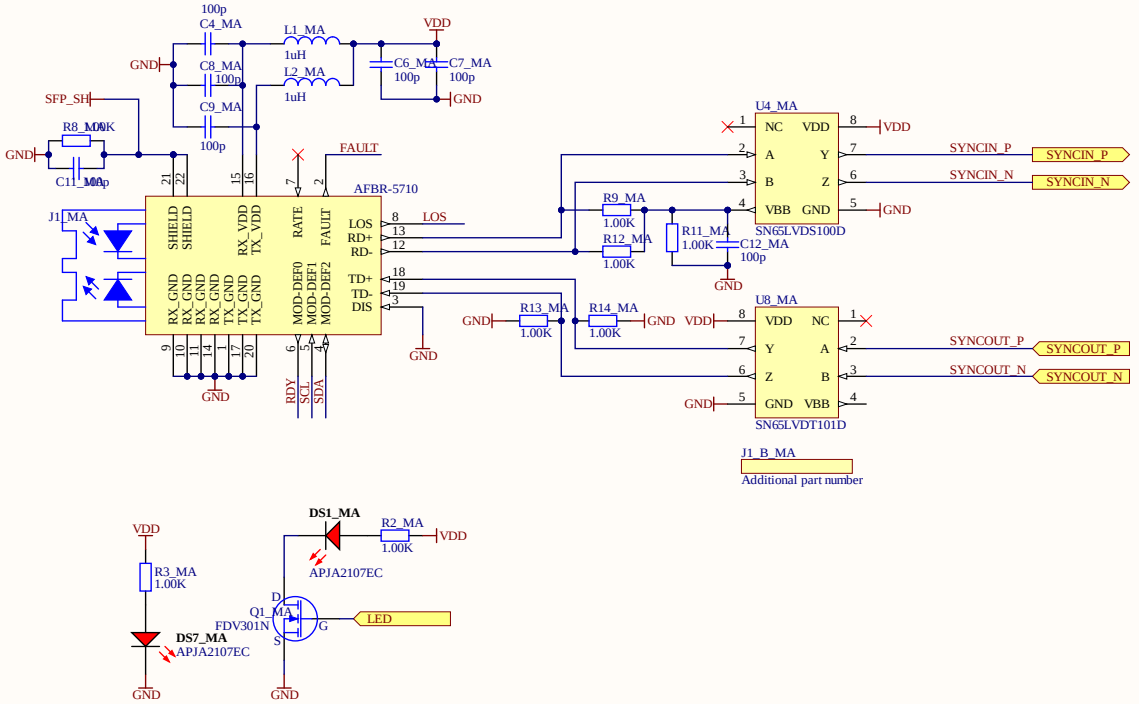
Samtec Expansion Port



Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Timing Interface*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 5/20/2020	Time: 1:46:46 PM	Sheet: 1 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface1.SchDoc			

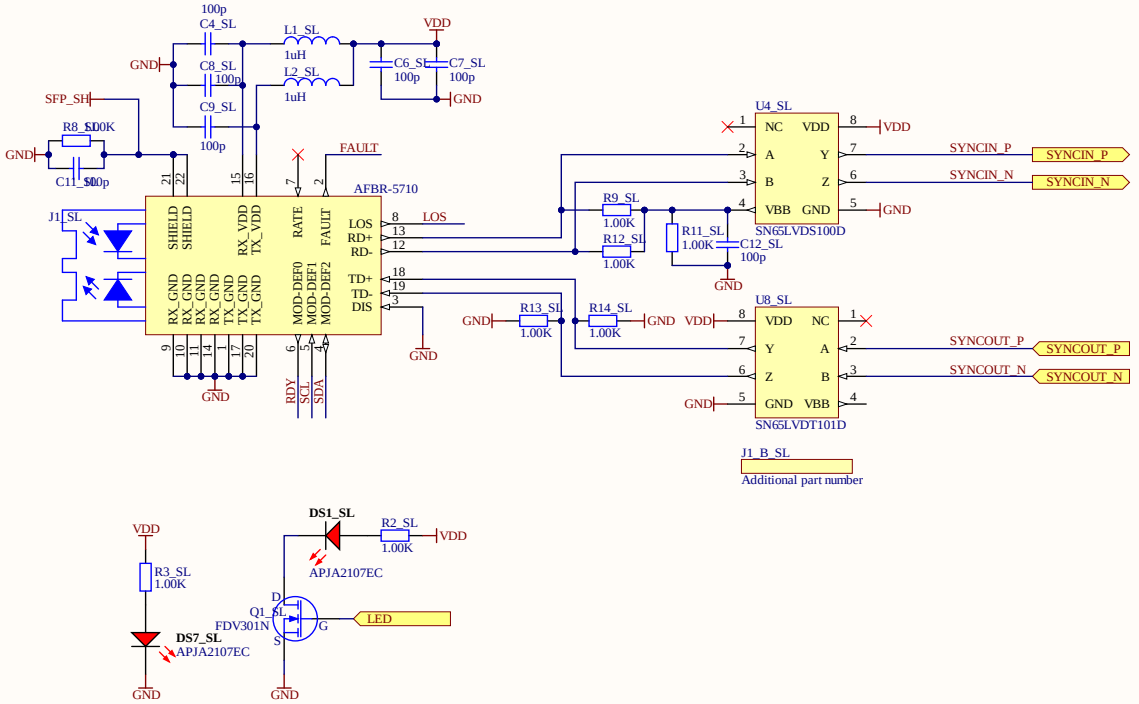

Phase Detector
quiet noise for phase detector 10v agnd
5V Reference
Vectron VCO
Project PCIe Timing Slave
Sheet Title VCO & Phase Detector
Size: B-C-D
DCC D070071
Rev: D
Date: 5/20/2020
Time: 1:46:47 PM
Sheet: 2 of 12
File: ChassisTimingInterface2.SchDoc
DrawnBy: M. Pirello
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
SN65LVDT14QPWREP
74LVC74D
SN74LVC1G00
OP284ES
U5A
U5B
U7
AD7685
ADR425BR
LT1763
BNX016-01
33.554432MHz
61300211821
BLM31PG121
MA
ChassisTimingInterface_SFP.SchDoc
SL
ChassisTimingInterface_SFP.SchDoc

SFP Port

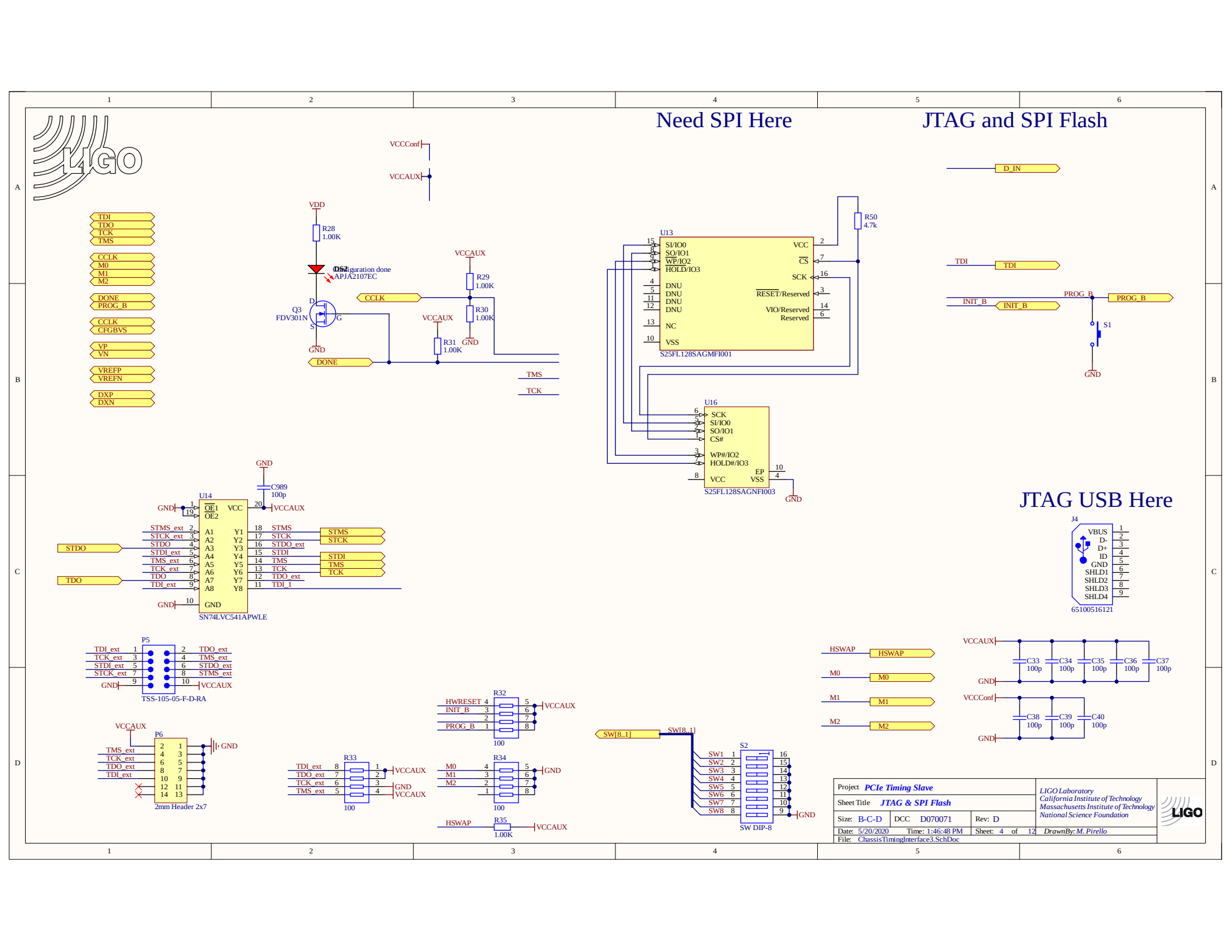


Project	***PCIe Timing Slave***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***SFP***		
Size: B-C-D	DCC D070071	Rev: D	
Date: 5/20/2020	Time: 1:46:47 PM	Sheet: 3 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface_SFP.SchDoc			

SFP Port



Project	***PCIe Timing Slave***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***SFP***		
Size: B-C-D	DCC D070071	Rev: D	
Date: 5/20/2020	Time: 1:46:47 PM	Sheet: 3 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface_SFP.SchDoc			



Project	*PCIe Timing Slave*
Sheet Title	*JTAG & SPI Flash*
Size: B-C-D	DCC D070071 Rev: D
Date: 5/20/2020	Time: 1:46:48 PM Sheet: 4 of 12
File: ChassisTimingInterface3.SchDoc	*DrawnBy: M. Pirello*

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Massachusetts Institute of Technology
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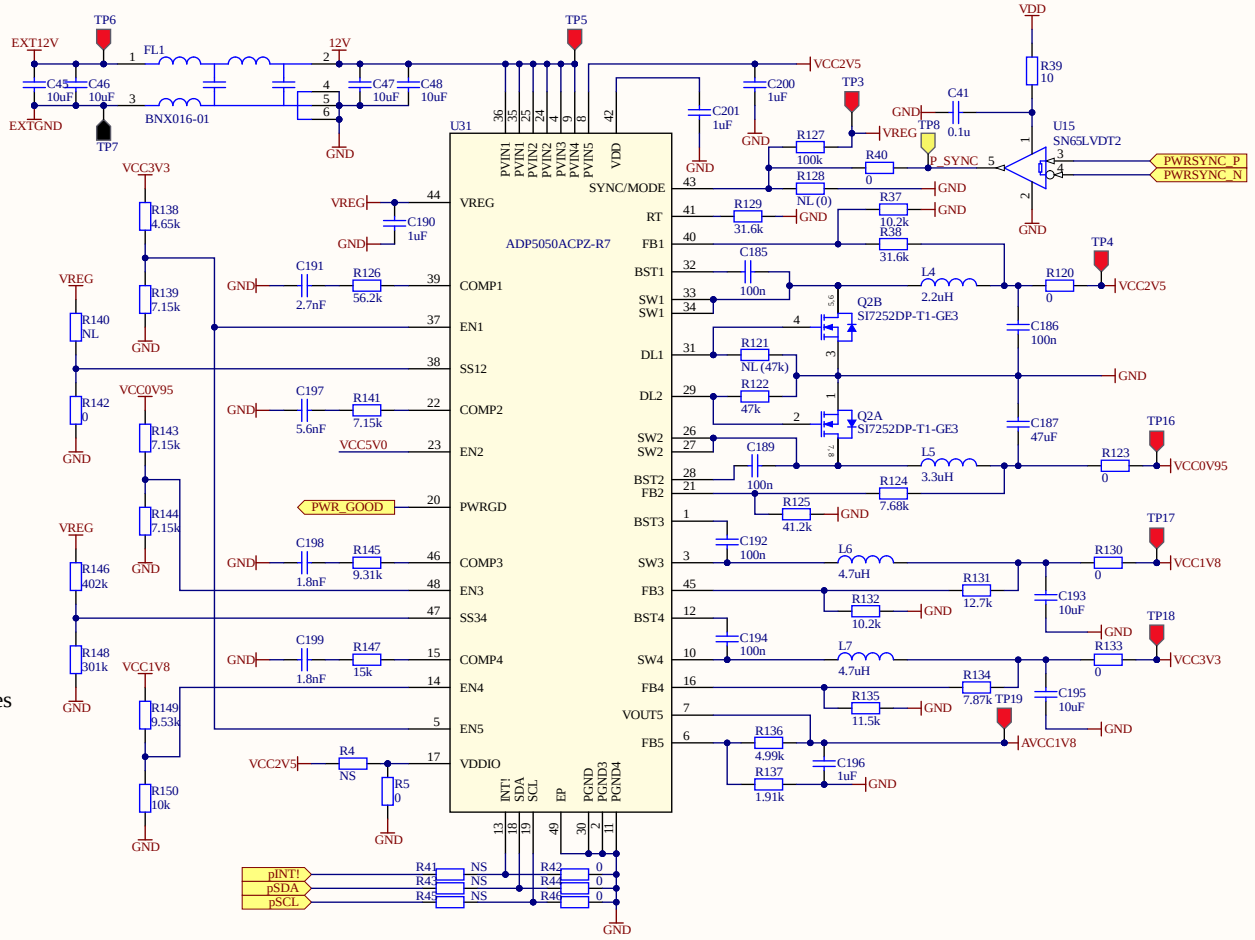
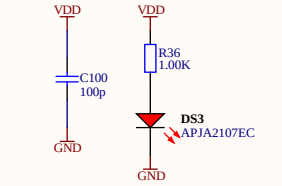
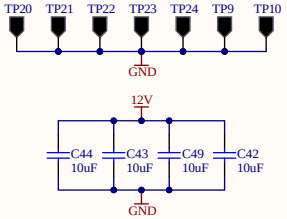
Switched FPGA Power



Evaluating These

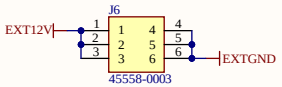




VCC Bridge

VDD Bridge

PCIe Power



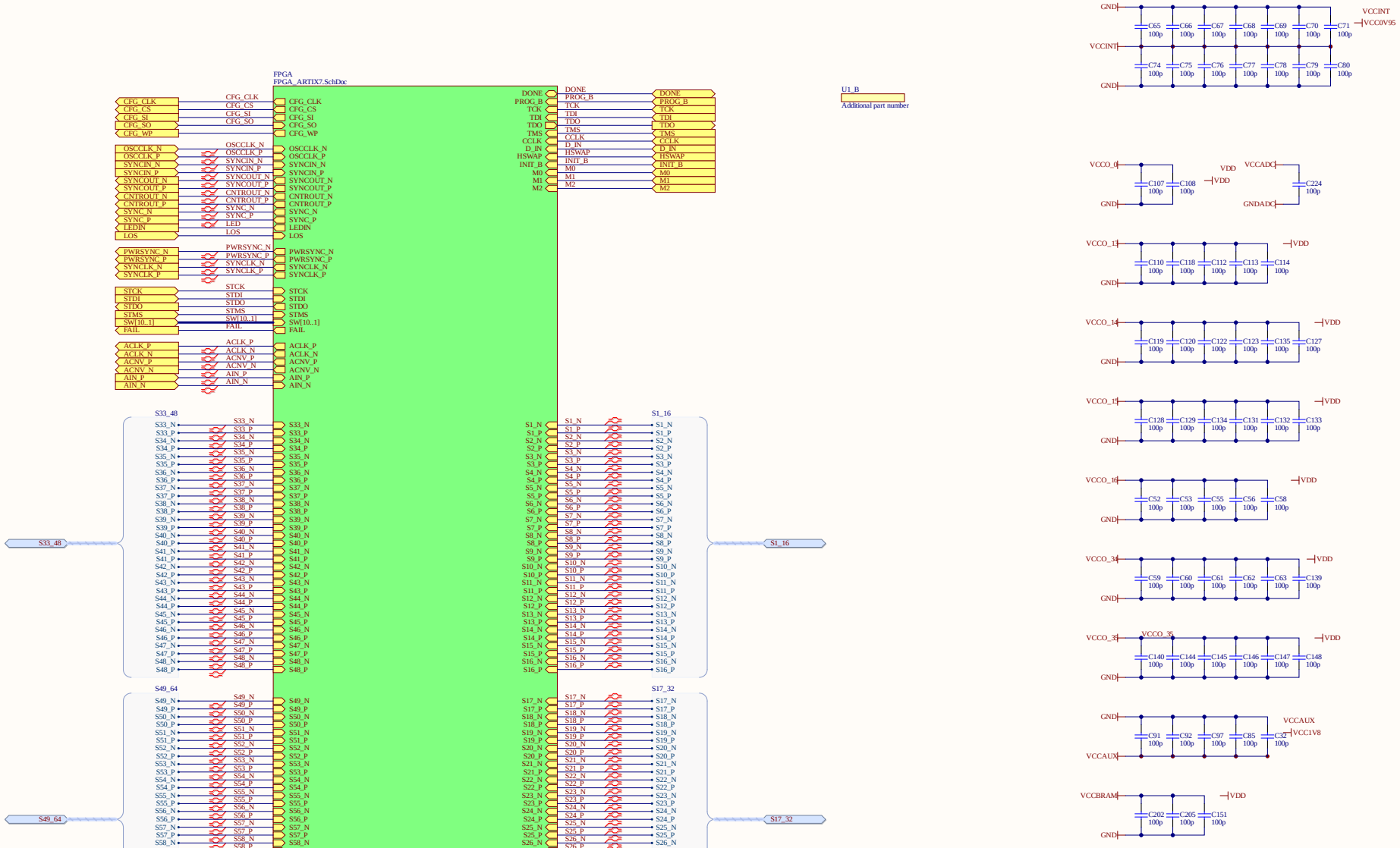
Voltage Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V

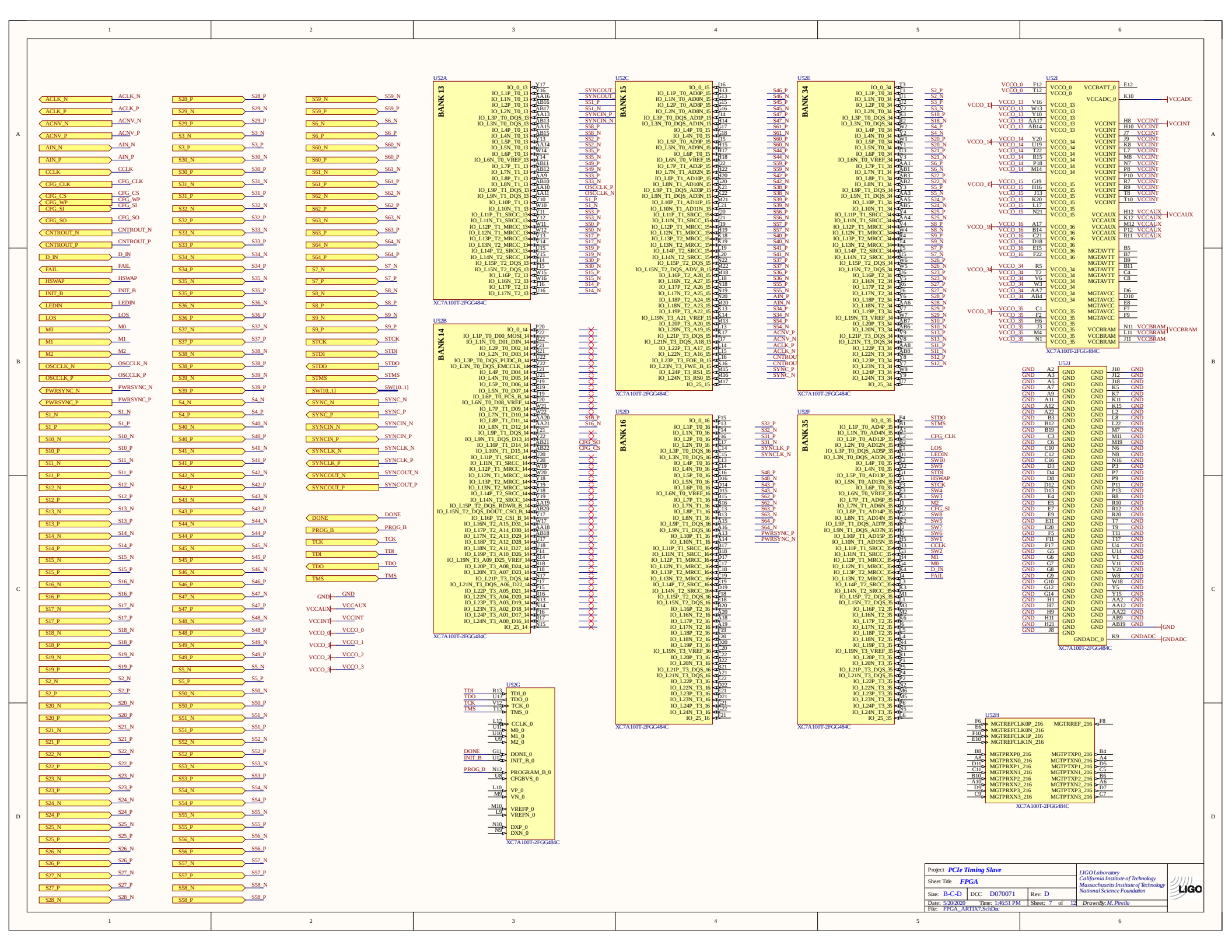
LVDS DC Specification
VCCO = 2.5
VOH = 1.675V
VOL = 0.7V

Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Power Supply*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 5/20/2020	Time: 1:46:48 PM	Sheet: 5 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface4.SchDoc			

FPGA Decoupling Caps



Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*FPGA Interface*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 5/20/2020	Time: 1:46:49 PM	Sheet: 6 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface5.SchDoc			


ACLK_N
ACLK_P
ACNV_N
ACNV_P
AIN_N
AIN_P
CCLK
CFG_CLK
CFG_CS
CFG_WP
CFG_SI
CFG_SO
CNTROUT_N
CNTROUT_P
D_IN
FAIL
HSWAP
INIT_B
LEDIN
LOS
M0
M1
M2
OSCCLK_N
OSCCLK_P
PWRSYNC_N
PWRSYNC_P
S1_N
S1_P
S10_N
S10_P
S11_N
S11_P
S12_N
S12_P
S13_N
S13_P
S14_N
S14_P
S15_N
S15_P
S16_N
S16_P
S17_N
S17_P
S18_N
S18_P
S19_N
S19_P
S2_N
S2_P
S20_N
S20_P
S21_N
S21_P
S22_N
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S24_N
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S25_N
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S29_N
S29_P
S3_N
S3_P
S30_N
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S31_N
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S62_P
S63_N
S63_P
S64_N
S64_P
S7_N
S7_P
S8_N
S8_P
S9_N
S9_P
STCK
STDI
STDO
STMS
SW[10..1]
SYNC_N
SYNC_P
SYNCIN_N
SYNCIN_P
SYNCLK_N
SYNCLK_P
SYNCOUT_N
SYNCOUT_P
DONE
PROG_B
TCK
TDI
TDO
TMS
GND
VCCAUX
VCCINT
VCCO_0
VCCO_1
VCCO_2
VCCO_3
U52A
BANK 13
XC7A100T-2FGG484C
U52B
BANK 14
XC7A100T-2FGG484C
U52C
BANK 15
XC7A100T-2FGG484C
U52D
BANK 16
XC7A100T-2FGG484C
U52E
BANK 34
XC7A100T-2FGG484C
U52F
BANK 35
XC7A100T-2FGG484C
U52G
XC7A100T-2FGG484C
U52I
XC7A100T-2FGG484C
U52J
XC7A100T-2FGG484C
U52H
XC7A100T-2FGG484C
Project PCIe Timing Slave
Sheet Title FPGA
Size: B-C-D
DCC D070071
Rev: D
Date: 5/20/2020
Time: 1:46:51 PM
Sheet: 7 of 12
File: FPGA_ARTIX7.SchDoc
DrawnBy: M. Pirello
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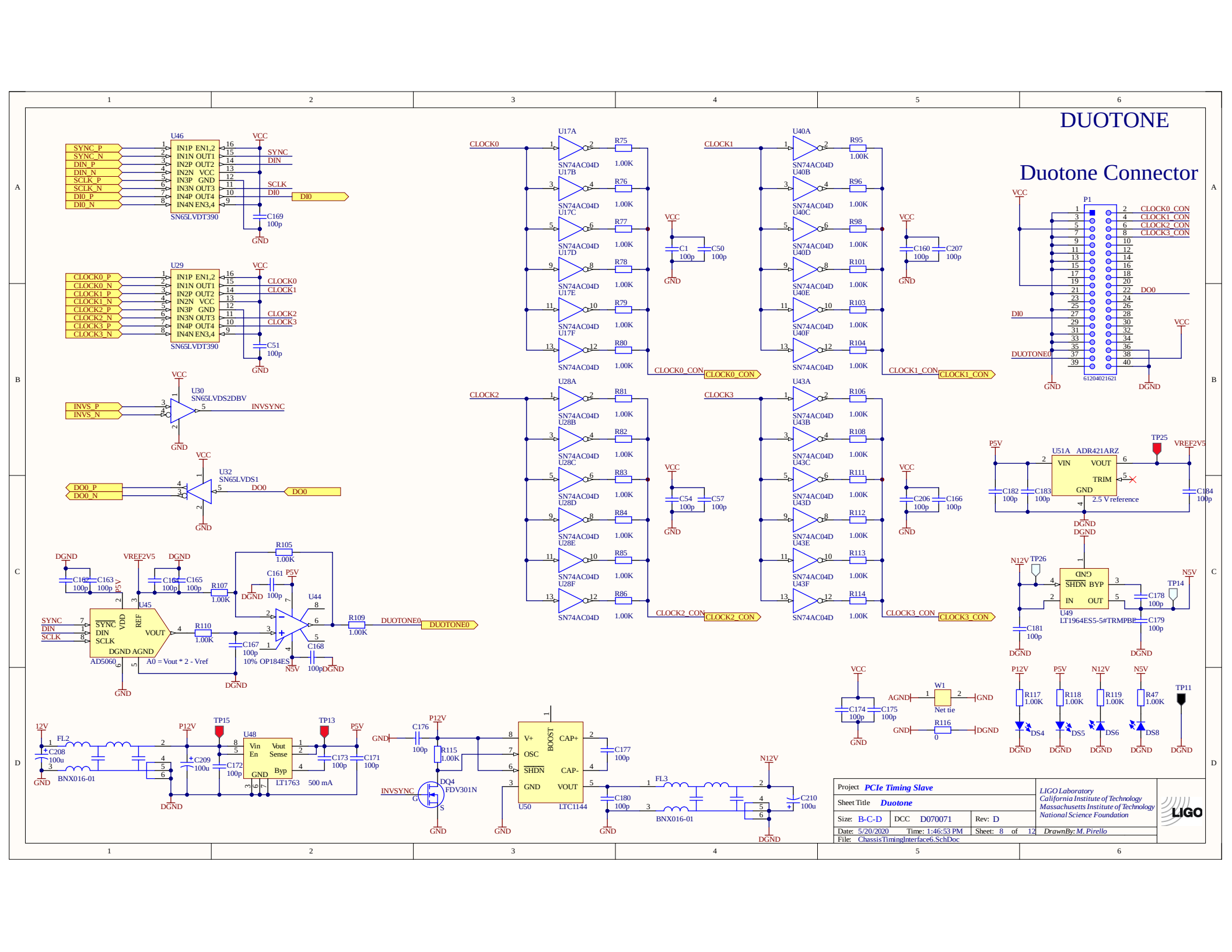
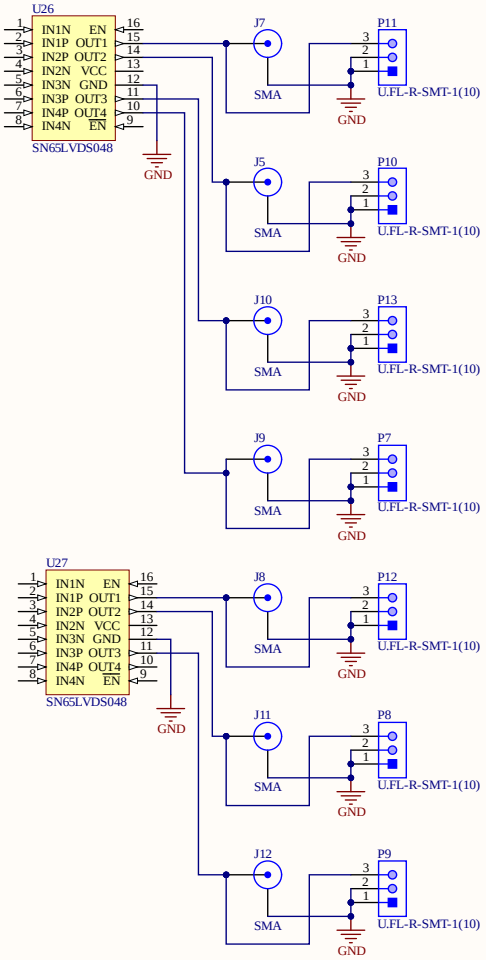
Massachusetts Institute of Technology
National Science Foundation
LIGO


DUOTONE
Duotone Connector
U46
SN65LVDT390
U29
SN65LVDT390
U30
SN65LVDS2DBV
U32
SN65LVDS1
U17A
U17B
U17C
U17D
U17E
U17F
U40A
U40B
U40C
U40D
U40E
U40F
U28A
U28B
U28C
U28D
U28E
U28F
U43A
U43B
U43C
U43D
U43E
U43F
SN74AC04D
U45
AD5060
A0 = Vout * 2 - Vref
U44
10% OP184ES
U48
LT1763
500 mA
U50
LTC1144
U51A ADR421ARZ
2.5 V reference
U49
LT1964ES5-5#TRMPBF
P1
61204021621
DQ4
FDV301N
W1
Net tie
BNX016-01
Project PCIe Timing Slave
Sheet Title Duotone
Size: B-C-D
DCC D070071
Rev: D
Date: 5/20/2020
Time: 1:46:53 PM
Sheet: 8 of 12
File: ChassisTimingInterface6.SchDoc
DrawnBy: M. Pirello
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
LIGO

Timing Connectors



Project	***PCIe Timing Slave***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***1PPS Timing***		
Size: B-C-D	DCC D070071	Rev: D	
Date: 5/20/2020 Time: 1:46:53 PM		Sheet: 9 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface7.SchDoc			

CONTEC & TIMING

CLOCK0_CON
CLOCK1_CON
CLOCK2_CON
CLOCK3_CON
DI0
DO0
DUOTONE0

DUOTONE_FB_MON
DUOTONE_SELECT0
DUOTONE_MON0
DUOTONE_FB_SELECT
DUOTONE_FB_MON_DAC

ADC_CLK_SRC_SELECT
DAC_CLK_SRC_SELECT
ADC_CLK_SRC_MON
ADC_CLK_POL_SELECT
DAC_CLK_SRC_MON
DAC_CLK_POL_SELECT
ADC_CLK_POL_MON
DAC_CLK_POL_MON
FROM_DUOTONE_DO0
TO_DUOTONE_DI0
WD_IN
TEMP_SW_MON

+12V

R51 1.00K
R52 1.00K
R53 1.00K
R54 1.00K
R55 1.00K
R56 1.00K
R57 1.00K

U18A
U18B
U18C
U18D
U18E
U18F
U19B
SN7406D

VCC

R58 1.00K
R59 1.00K
R60 1.00K
R61 1.00K
R62 1.00K
R63 1.00K
R64 1.00K

U19A
U20B
U19C
U19D
U19E
U19F
U20A
SN7406D

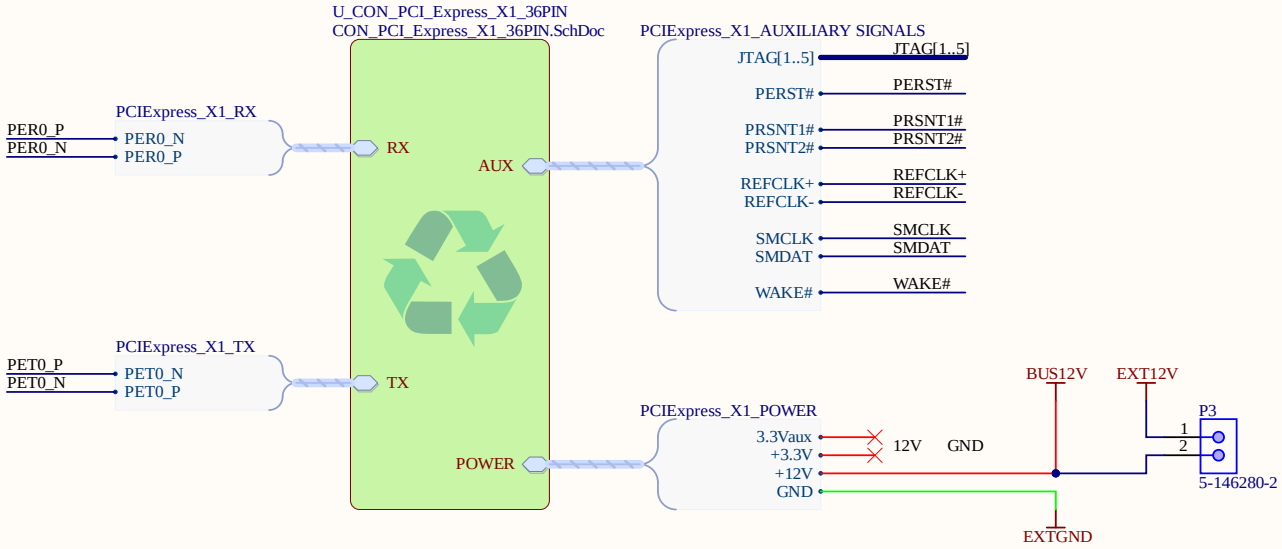
U18G
U19G
VCC GND
SN7406D

Contec Connector

J2
DB37F

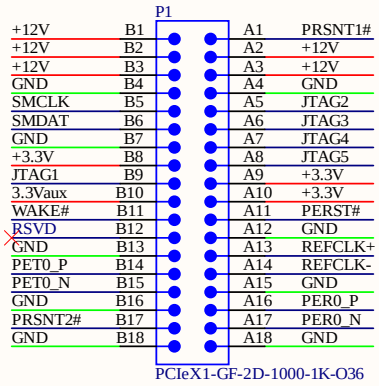
GND
DUOTONE_FB_MON_CON
DUOTONE_SELECT0_CON
DUOTONE_MON0_CON
DUOTONE_FB_SELECT_CON
DUOTONE_FB_MON_DAC_CON
ADC_CLK_SRC_SELECT_CON
DAC_CLK_SRC_SELECT_CON
ADC_CLK_SRC_MON_CON
ADC_CLK_POL_SELECT_CON
DAC_CLK_SRC_MON_CON
DAC_CLK_POL_SELECT_CON
ADC_CLK_POL_MON_CON
DAC_CLK_POL_MON_CON
FROM_DUOTONE_DO0_CON
TO_DUOTONE_DI0_CON
WD_IN_CON
TEMP_SW_MON
+12V

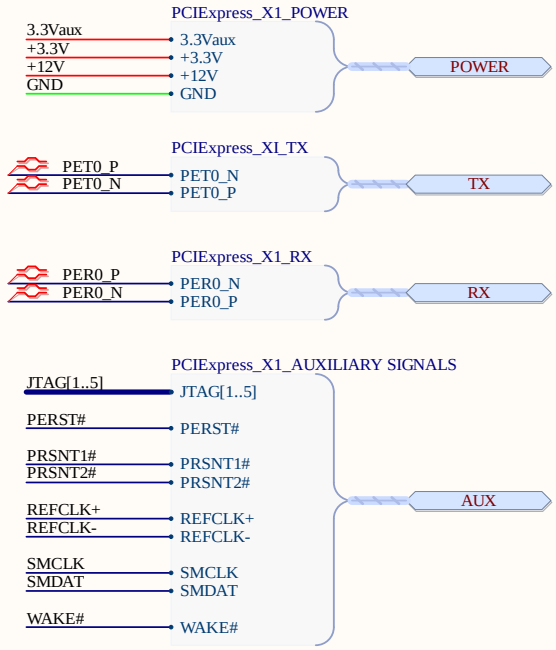
Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*CONTEC & Timing*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 5/20/2020	Time: 1:46:54 PM	Sheet: 10 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface8.SchDoc			



- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

Project	***PCIe Timing Slave***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***PCIe Interface***		
Size: B-C-D	DCC D070071	Rev: D	
Date: 5/20/2020	Time: 1:46:54 PM	Sheet: 11 of 12	*DrawnBy: M. Pirello*
File: PCI Express_16765X11115_36PIN_Half length.schdoc			





Title *			*
Size: A4	Number:*	Revision:*	*
Date: 5/20/2020	Time: 1:46:54 PM	Sheet* of *	*
File: C:\Users\marc.pirello\Altium\Solutions\ISC - PCIe Duotone\PCIe_ChassisTimingInterface\Managed\Sheets\02F33160-28.			