LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

CALIFORNIA INSTITUTE OF TECHNOLOGY

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Test Procedure	**T1700233-v1**	
PZT Driver Chassis Test Procedure		
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Performed by:_____
Date:_____
Board Serial Number: _____

1. **Overview**
   The PZT Driver Chassis (D1001200) houses four PZT Driver Boards (D1001203-V2), one PAZ Driver Interface Board (D1001204-v1) and one Low Noise Power Board (D0901846-rev.D) The function of this chassis is to drive 4 PZTs.

2. **Test Equipment**

   2.1 Power Supply capable of +/- 17V
   2.2 Power Supply capable of +/- 24V
   2.3 Power Supply capable of +200V (For the "HV" connector)
   2.4 Voltage Calibrator, or adjustable power supply
   2.5 SR785 Network Analyzer, or equivalent
   2.6 2 Dsub Breakout boards (15-pin)
   2.7 Digital Multimeter (DMM)
   2.8 Oscilloscope

3. **Preliminaries**

   3.1 Perform visual inspection of the Chassis to make sure nothing looks overtly broken.
   3.2 Before connecting the power to the box, set all power supplies to their correct Voltages and then turn them off. Connect the power supply to the chassis under test at the appropriate connectors. Turn on the 24V, then the 17V, then the High Voltage supply.
   3.3 Connect 15-pin Dsub Breakout boards to the "Controls" connector on the back panel, and the "Bias" connector on the front panel.
   3.4 Clip the -15V from TP6 on the low power board over to TP3 on the Interface Board.

4. **Electrical Tests**

To test the Low Noise Power Module (D0901846) with the PZT Driver Interface (D1001204).

4.1 Verify the proper current draw. Using a bench DC supply apply ±24Volts to P7 and ±17 Volts to P6 of the low noise power Module (D0901846). Measure the current draw of the board.

+24 Volt current _____0.03 A Nom.

–24 Volt current _____ 0.03 A Nom.

+17 Volt current _____ less than 0.3 A

–17 Volt current _____ less than 0.3 A

4.2 On the low noise power module check the voltage on TP 1-13.

TP1 (+17V) _____ TP2 (–17V) _____

TP3 , 4 (GND) TP5 (+ 5V)_____

TP6 (–15V) _____ TP7 (+24V) _____

TP8 (GND) TP9 (–24V) _____

TP10 (GND) TP11 (+15V) _____

TP12 (+VREF) _____ TP13 (–VREF) _____

4.3 If TP 1 , 2, 7 , 9 and 8 are correct then pin 5 on U1 and U7, TP14 (OK) should be Logic high ~3Volts. The front panel LED should be on.

Confirm._____

4.4 The noise on TP 12, 13, 11 and 6 should be measured with a SR785 using an rms power spectrum.

TP12 noise _____less than 20 nVrms/√Hz at 140 Hz

TP13 noise _____less than 30 nVrms/√Hz at 140 Hz

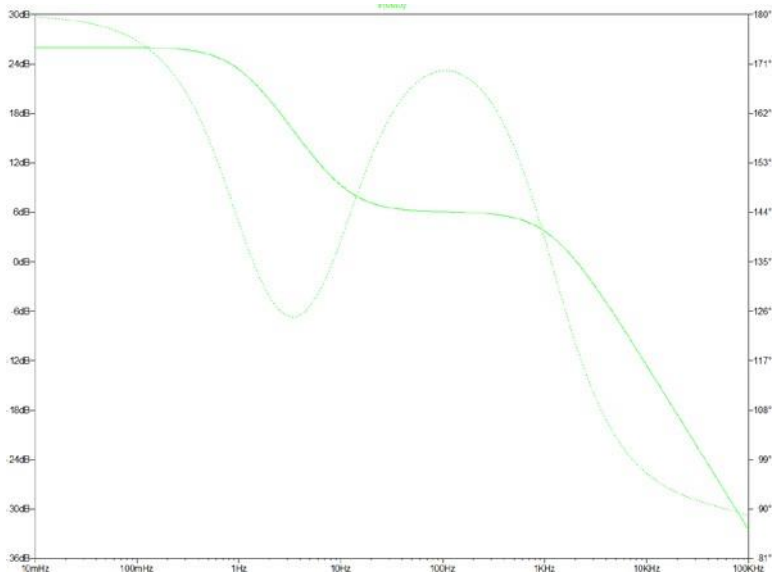
TP11 noise _____ less than 40 nVrms/√Hz at 140 Hz

TP6 noise _____ less than 60 nVrms/√Hz at 140 Hz.

4.5 Transfer Function Tests

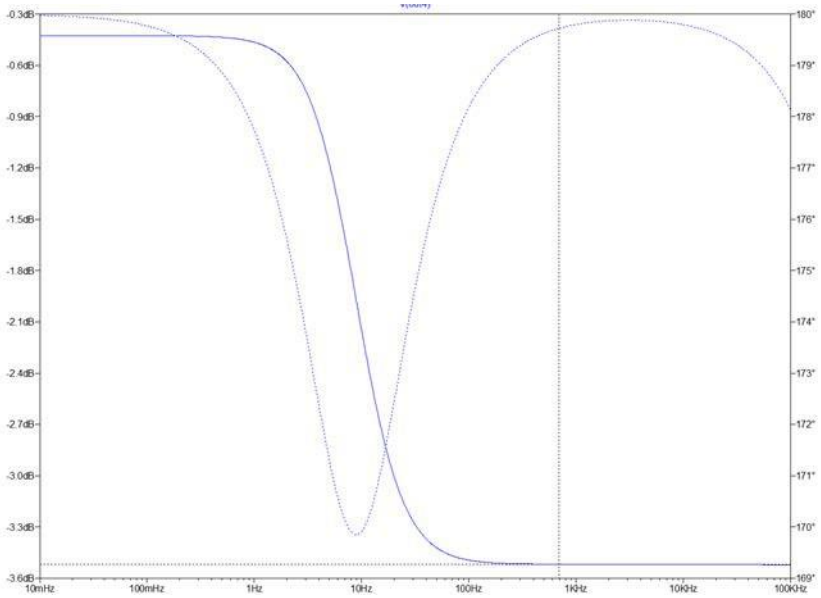
Take the transfer function from the appropriate channel "IN" TNC connector to the back panel "Output" connector, or the front panel "MON" connector as directed in the table below. Set the source to 200mV, and sweep from 0.1Hz to 100KHz, with 50 point steps. The traces should look like the simulation examples given. Record the amplitude at the frequency of each column. Passing values are nominal +/- .2dB, except for 100KHz, which can be +/-1dB. Before plugging the signal into the SR785, look at the signal on a scope, and apply the correct offset to the "Controls" breakout between the appropriate pins in the table below, to remove any offset on the signal. Unplug, and perform this zeroing for each signal, to make sure that there is no high voltage offset that might damage the SR785. The appropriate value is around -100mV. If it takes a much larger input than that, check to make sure nothing is damaged.

To back Panel “Output” connector:



Connector	Offset Pins	0.1Hz (25.9dB)	954mHz (23.5dB)	86Hz (6.05dB)	1.09KHz (3.3dB)	100KHz (-32.8dB)
Ch1	1(-), 9(+)					
Ch2	2(-), 10(+)					
Ch3	3(-), 11(+)					
Ch4	4(-), 12(+)					

To Front Panel “MON” connector:



Channel	1Hz (-0.6dB)	1.15KHz (-3.6dB)
Ch1		
Ch2		
Ch3		
Ch4		

4.6 Noise Tests

With the inputs to the PZT Drivers shorted together, and grounded, read the output noise levels on the appropriate "OUT" channels. Span the analyzer down to a 400Hz bandwidth. Fill out the appropriate cells in the table below:

Outputs	Level @ 100Hz (nom. Below 120nV/√Hz)
Ch1	
Ch2	
Ch3	
Ch4	

4.6.1 "Bias" Tests: Short pins 7&8 of the back panel "Controls" connector together to enable bias inputs, then put 1V onto the pins in the table below, to GND. Read the Voltage on TP4 on the appropriate PZT Driver Board, and record the results in the table below:

Input	Output	Voltage (-0.95V+/- 0.05V)
"Bias" Pin 2(+) to Pin 15(GND)	CH1 TP4	
"Bias" Pin 10(+) to Pin 15(GND)	CH2 TP4	
"Bias" Pin 5(+) to Pin 15(GND)	CH3 TP4	
"Bias" Pin 13(+) to Pin 15(GND)	CH4 TP4	

With a DMM, read the voltage between the pins in the table below. Nominal is +20V +/-0.1V

Pins	Voltage (20V+/- 0.1V)
"Bias" Pins 1(+) to 9(-)	
"Bias" Pins 3(+) to 11(-)	
"Bias" Pins 4(+) to 12(-)	
"Bias" Pins 6(+) to 14(-)	