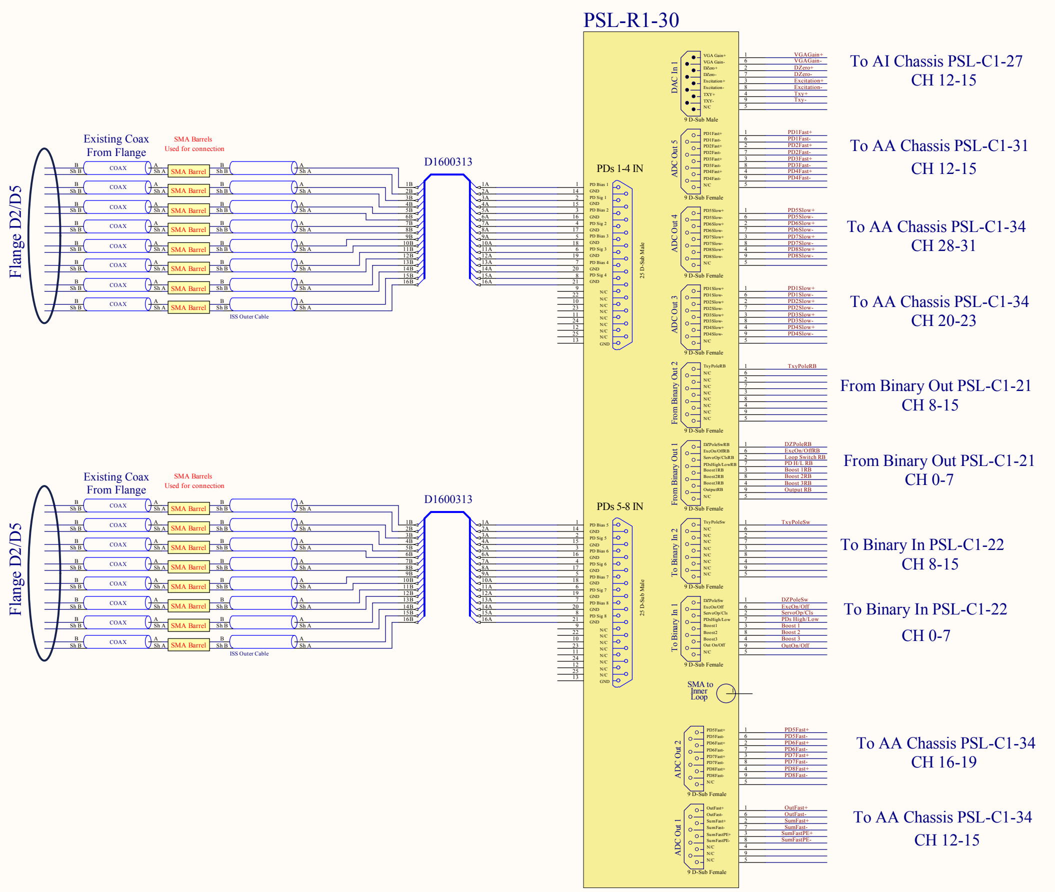
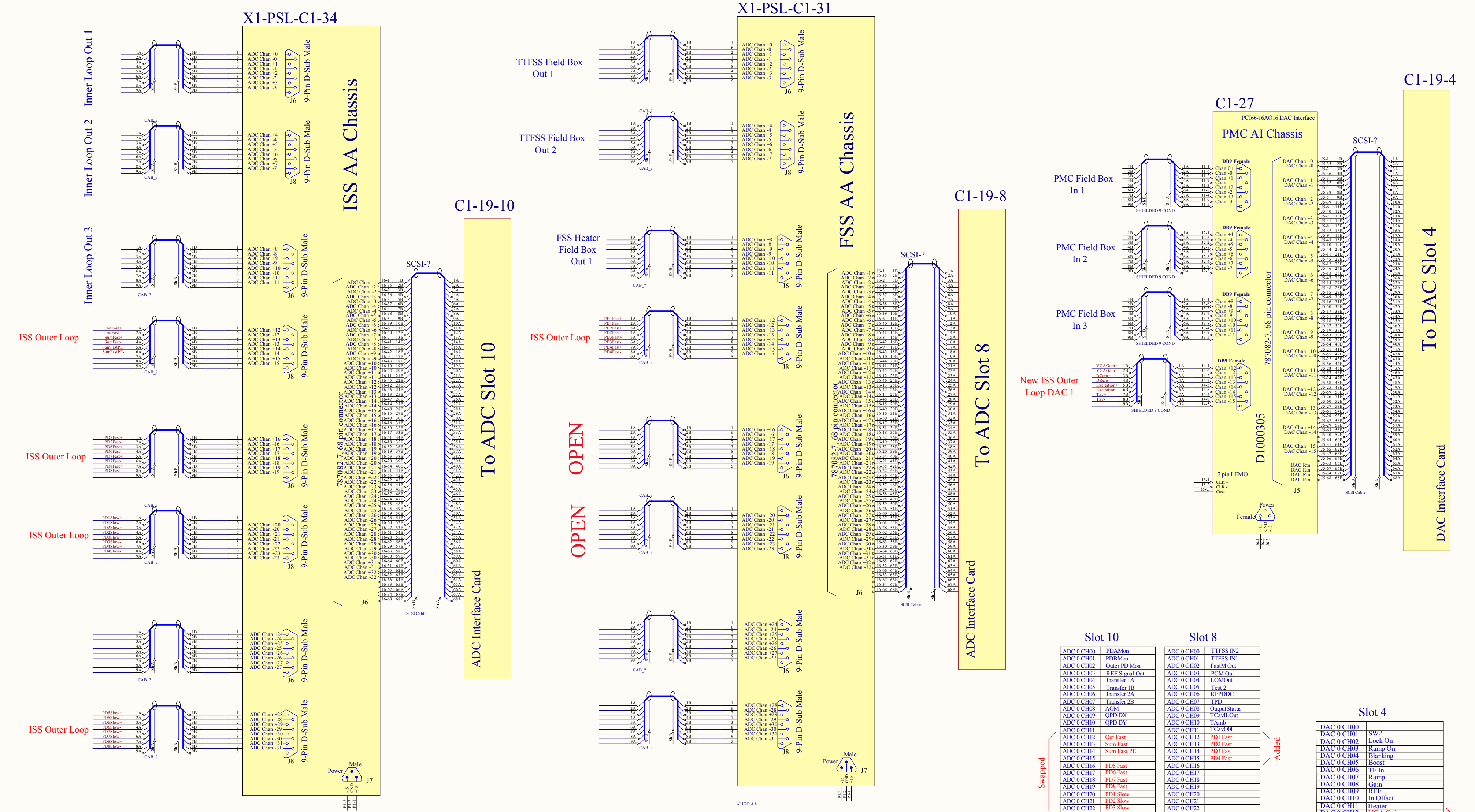
ISS Outer Loop Servo



PSL-R1-30
Flange D2/D5
Existing Coax From Flange
SMA Barrels Used for connection
SMA Barrel
COAX
ISS Outer Cable
D1600313
PDs 1-4 IN
PDs 5-8 IN
25 D-Sub Male
DAC In 1
ADC Out 5
ADC Out 4
ADC Out 3
From Binary Out 2
From Binary Out 1
To Binary In 2
To Binary In 1
ADC Out 2
ADC Out 1
9 D-Sub Male
9 D-Sub Female
SMA to Inner Loop
To AI Chassis PSL-C1-27 CH 12-15
To AA Chassis PSL-C1-31 CH 12-15
To AA Chassis PSL-C1-34 CH 28-31
To AA Chassis PSL-C1-34 CH 20-23
From Binary Out PSL-C1-21 CH 8-15
From Binary Out PSL-C1-21 CH 0-7
To Binary In PSL-C1-22 CH 8-15
To Binary In PSL-C1-22 CH 0-7
To AA Chassis PSL-C1-34 CH 16-19
To AA Chassis PSL-C1-34 CH 12-15

Title	*ISS Outer Loop Wiring*
Size: D	DCC Number: D1600321
Drawn by: Ben Abbott	Date: 8/5/2016
Revision: v1	Ligo Project, California Institute of Technology, Massachusetts Institute of Technology
File: C:\restored\Ben\ISS Outer Loop\System Schematics\ISS Outer Loop System Schematic.SchDoc	Sheet 1 of 4



Slot 10

ADC 0 CH00	PDAMon
ADC 0 CH01	PDBMon
ADC 0 CH02	Outer PD Mon
ADC 0 CH03	REF Signal Out
ADC 0 CH04	Transfer 1A
ADC 0 CH05	Transfer 1B
ADC 0 CH06	Transfer 2A
ADC 0 CH07	Transfer 2B
ADC 0 CH08	AOM
ADC 0 CH09	QPD DX
ADC 0 CH10	QPD DY
ADC 0 CH11	
ADC 0 CH12	Out Fast
ADC 0 CH13	Sum Fast
ADC 0 CH14	Sum Fast PE
ADC 0 CH15	
ADC 0 CH16	PD5 Fast
ADC 0 CH17	PD6 Fast
ADC 0 CH18	PD7 Fast
ADC 0 CH19	PD8 Fast
ADC 0 CH20	PD1 Slow
ADC 0 CH21	PD2 Slow
ADC 0 CH22	PD3 Slow
ADC 0 CH23	PD4 Slow
ADC 0 CH24	
ADC 0 CH25	
ADC 0 CH26	
ADC 0 CH27	
ADC 0 CH28	PD5 Slow
ADC 0 CH29	PD6 Slow
ADC 0 CH30	PD7 Slow
ADC 0 CH31	PD8 Slow

Swapped (CH12–CH23)
Added (CH28–CH31)

Slot 8

ADC 0 CH00	TTFSS IN2
ADC 0 CH01	TTFSS IN1
ADC 0 CH02	FastM Out
ADC 0 CH03	PCM Out
ADC 0 CH04	LOMOut
ADC 0 CH05	Test 2
ADC 0 CH06	RFPDDC
ADC 0 CH07	TPD
ADC 0 CH08	OutputStatus
ADC 0 CH09	TCavILOut
ADC 0 CH10	TAmb
ADC 0 CH11	TCavO0L
ADC 0 CH12	PD1 Fast
ADC 0 CH13	PD2 Fast
ADC 0 CH14	PD3 Fast
ADC 0 CH15	PD4 Fast
ADC 0 CH16	
ADC 0 CH17	
ADC 0 CH18	
ADC 0 CH19	
ADC 0 CH20	
ADC 0 CH21	
ADC 0 CH22	
ADC 0 CH23	
ADC 0 CH24	????????
ADC 0 CH25	????????
ADC 0 CH26	????????
ADC 0 CH27	????????
ADC 0 CH28	????????
ADC 0 CH29	????????
ADC 0 CH30	????????
ADC 0 CH31	????????

Added (CH12–CH15)

Slot 4

DAC 0 CH00	
DAC 0 CH01	SW2
DAC 0 CH02	Lock On
DAC 0 CH03	Ramp On
DAC 0 CH04	Blanking
DAC 0 CH05	Boost
DAC 0 CH06	TF In
DAC 0 CH07	Ramp
DAC 0 CH08	Gain
DAC 0 CH09	REF
DAC 0 CH10	In Offset
DAC 0 CH11	Heater
DAC 0 CH12	VGA Gain
DAC 0 CH13	Digital Zero
DAC 0 CH14	Excitation
DAC 0 CH15	TXY

Added (CH12–CH15)

Title: *ADCs and DACs*
Size: D
DCC Number: D1600321
Drawn by: Ben Abbott
Date: 8/5/2016
Revision: v1

Ligo Project
California Institute of Technology
Massachusetts Institute of Technology

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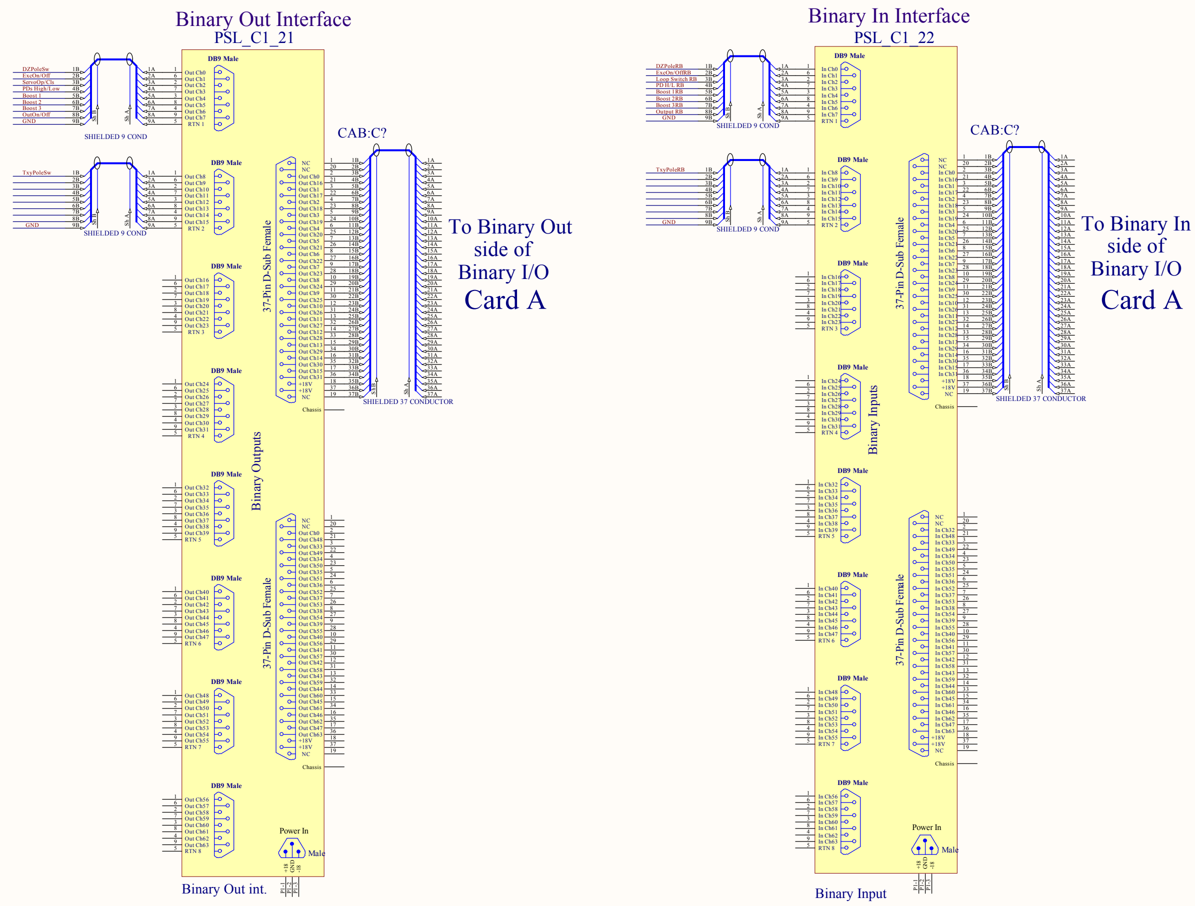
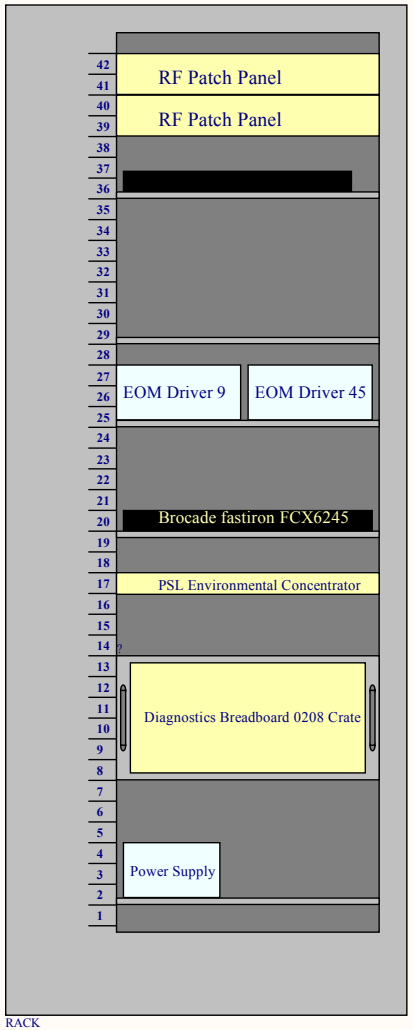
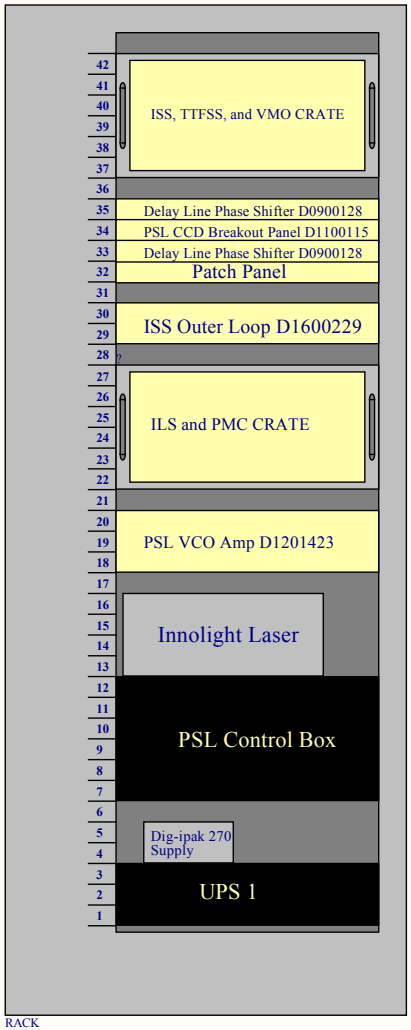


Title: *Binary I/O*			
Size: D	DCC Number: D1600321		Ligo Project California Institute of Technology Massachusetts Institute of Technology
Drawn by: Ben Abbott	Date: 8/5/2016	Revision: v1	
File: C:\restored\Ben\ISS Outer Loop\System Schematics\ISS Outer Loop System Schematic Binary.SchDoc	Time: 3:39:47 PM	Sheet 3 of 4	

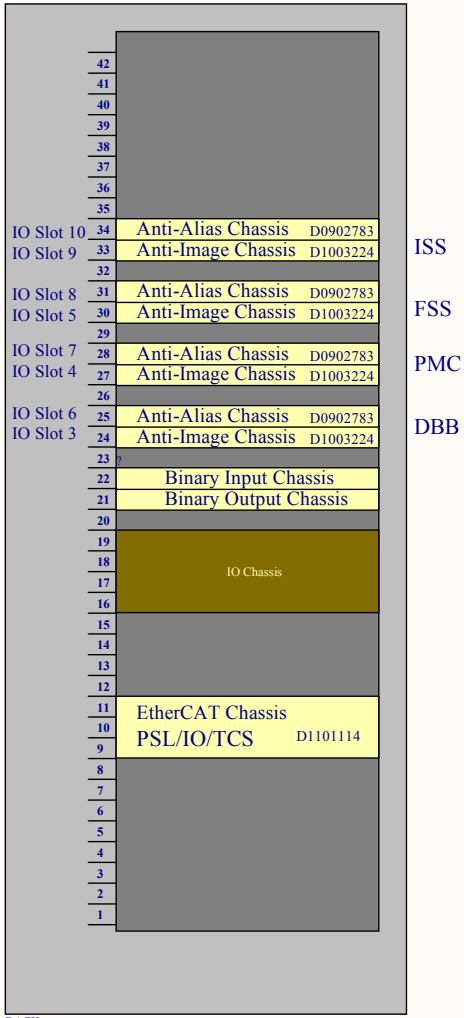
X1-PSL-R2



X1-PSL-R1



X1-PSL-C1



Title: ***PSL Racks***			
Size: B	DCC Number: D1600321	*Ligo Project* *California Institute of Technology* *Massachusetts Institute of Technology*	Cannot open file C:\Restored\Ben\miscellany\ligologo_t.jpg
Drawn by: Ben Abbott	Date: 8/5/2016	Revision: v1	
File: C:\restored\Ben\ISS Outer Loop\System Schematics\ISS Outer Loop System Schematic.vsd		Time: 3:39:47 PM Sheet 1 of 1	