Title	*Hardware Watchdog Chassis Analysis and Review*
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Overview

In July 2015, a team consisting of Vern Sandberg, Richard McCarthy, Ben Abbott, Dave Barker and Richard Abbott were convened to evaluate and report on the way forward to complete and deploy the Hardware Watchdog (HWWD) system. A unit (S1301701 of D1300642 containing D1201549-v3 PCB programmed with E1500315-v1, 2014 HWWD Code) was sent from LHO in order to evaluate an intermittent booting problem on power-up. As well as the boot problem, there is a need to invert the logic for the four status bits associated with this device. The issue with the logic bits relates to a normal condition being reported as a logic low; this condition is unsatisfactory as the same report can be obtained from an unpowered or disconnected chassis.

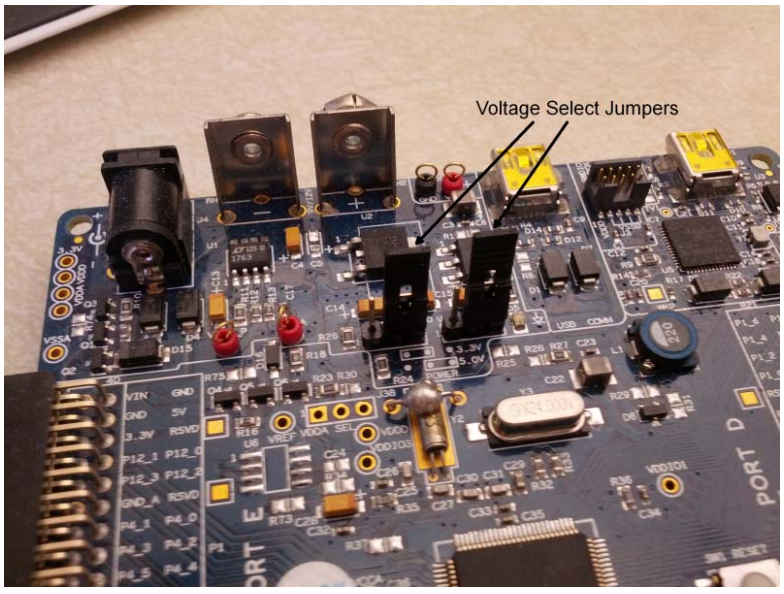
The HWWD chassis utilizes a dedicated Programmable System on a Chip (PSoC). This device is a hybrid of programmable analog hardware and software. As the fundamental nature of this device is to be programmed by software, there exists a need to verify installed code version and to maintain configuration control of the software.

Along with the above investigations, a brief verification of key functional parameters was also conducted. The rms trip setpoint was measured as well as the gain of the BNC rms monitor.

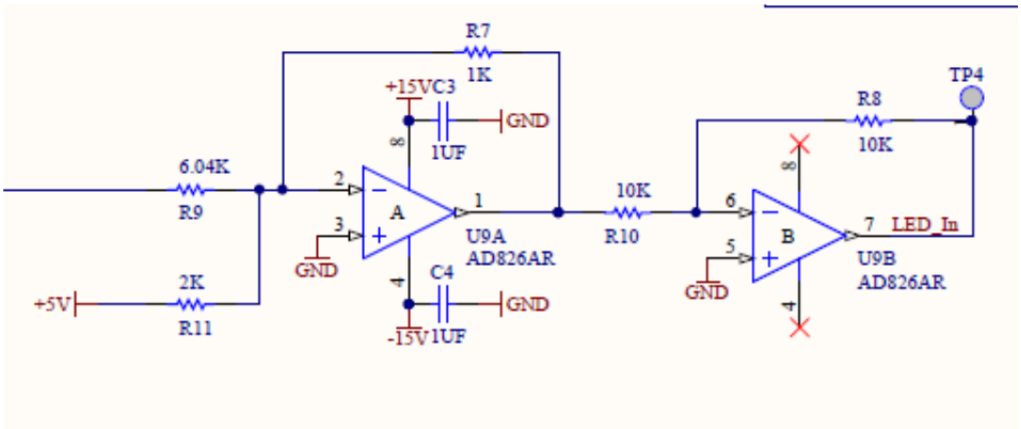
Boot Problem

The issue of intermittent booting upon initial power up was reported as only existing in certain units, and only when connected to an operational Satellite Amplifier through the field cabling. Bench testing of S1301701 did indeed reveal the existence of this problem. With a handheld voltage source, a voltage (ranging from 1 to several volts) was applied to the HWWD LED Monitors during boot to simulate the voltage coming from the satellite module. The HWWD was connected to the voltage source through the standard field cabling used at the observatories. The HWWD would not boot properly while the voltage was applied. The problem was traced down to a pair of jumpers on the PSoC board being configured for 3.3V operation, vs. 5.0V operation. The jumpers seen below are in the correct (5.0V) position. All units should be configured as shown below.

Figure 1



After moving the jumpers to the 5.0V position, repeated tests were conducted and no boot issues were seen. The applied voltage was increased to 13VDC and still no boot problems were seen. It is worthy of note that the output impedance of the satellite module monitor channels that feed the HWWD is 4.7kΩ. This series resistance, in conjunction with the 300Ω resistor forming the inverting input of an opamp stage in the HWWD, forms a unity gain stage. The absence of the 4.7kΩ resistor in the satellite module would result in a gross gain error.

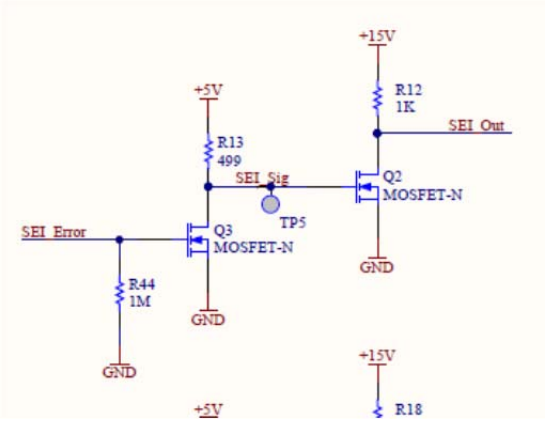


The schematic shown above is an excerpt of D1201549-v3. The component values shown for R7, R9, and R11 are not correct. The correct values are: R7 = 5kΩ, R9 = 300Ω, R11 = 10kΩ. The parameter on the right named "LED_In" is compared internally by the PSoC to a reference voltage (2.640V) as a measure of satisfactory operation of the satellite module LED current monitors. With a nominal current flowing in the OSEM LEDs as driven by the satellite module, the measured voltage present at TP4 is 3.5VDC

Logic Monitor Changes

The existing logic monitors for D1201549-v3 are shown below. The left-hand node labeled SEI_Error is at a logic low during normal operation. This logic state creates a logic high at the node labeled SEI_Sig, and a logic low at SEI_Out. SEI_Sig is used to drive a front panel green LED to provide a visual indication of the normal condition. SEI_Out is sent to binary monitors to remotely annunciate the state of the HWWD. It is obvious by inspection that this circuit is not easy to change if the goal is to preserve the functionality of the LED. What is needed would be another logical inversion after SEI_Out such that the normal state is indicated by a logic high voltage level.

Figure 2



A small circuit board (see D1500215-v1) has been built that accomplishes the logic flip. A MOSFET is used in a similar manner to those seen in Figure 2. The overall topology of the circuit board is shown in Figure 3. Power to the MOSFETS is provided from spare DC power supply outputs within the HWWD chassis. This circuit board is small enough to go in line with the existing cabling interior to the HWWD chassis in a plug-and-play fashion.

Figure 3, logic inverter topology

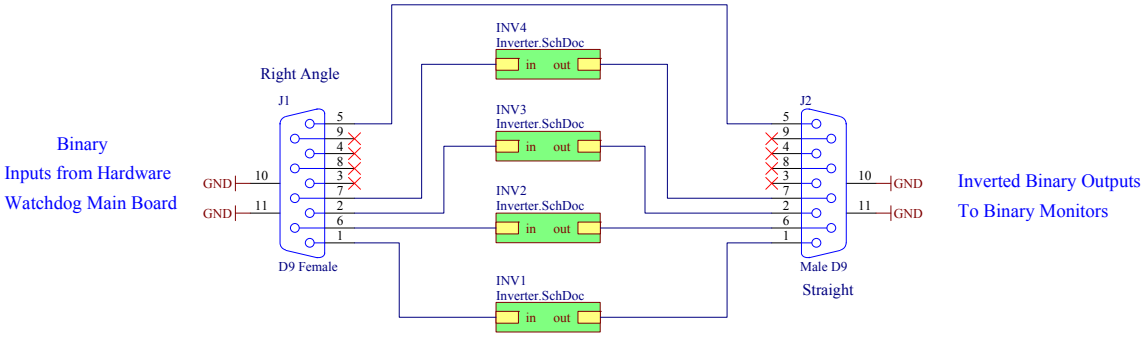
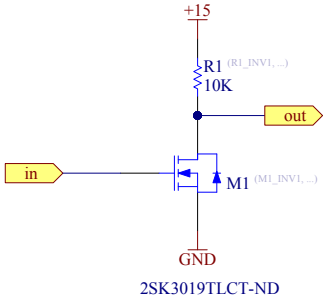


Figure 4, logic inverter detail



Parameter Verification

A function generator was used to apply a 1Hz sine wave to the PDmon input simulating a signal from the satellite module as would be seen during operation of the suspension controls. The function generator was coupled through a 4.64kΩ resistor to simulate the output impedance of the satellite module. The amplitude of the sine wave was increased incrementally to find the value at which the rms trip threshold triggers. Also, during this time, the DC output of the rms monitor BNC present on the rear panel was monitored to establish the gain of the rms monitor function. The results are summarized below.

Table 1 rms Data

Parameter	Measured Value
RMS Trip Threshold	2.8Vrms at 1Hz
RMS Monitor Gain	36mVDC/Vrms

Code Version Verification

There is no external method to verify the version of the installed code in the existing HWWD chassis. For this reason, additional code has been added to the PSoC to blink the front panel LED light at 1 second intervals on initial power up. The number of blinks will correspond to the version number of E1500315 PSoC Programming Code. At time of writing, the active version is v2, thus two blinks will be seen followed by a 3 second pause before continuing with the normal startup routine.