

<i>Title</i>	<i>ETM Low Voltage ESD Driver Chassis Test Procedure</i>
<i>Author</i>	<i>R. Abbott, Caltech</i>
<i>Date</i>	<i>10 July 2015</i>
<i>Hardware Version</i>	<i>PCB D1500016-v1 and v2, D1500128-v1 in Chassis D1500129</i>

1 Overview

This procedure is used to verify proper operation of the D1500129 Low Voltage Low Noise ESD Driver Chassis. This chassis operates at voltages up to 430VDC and portions of this procedure assume that the person performing the test is familiar with high voltage circuit testing. **The Test Technician or Engineer MUST be a LIGO approved Qualified Electrical Worker specifically authorized to work on energized equipment to perform high voltage measurements on exposed equipment.**

Table 1

Chassis Serial Number	S1500068	
Main Board Serial Number	S1500059	
Back Board Serial Number	S1500083	
DC Power Board Serial Number	S1500086	
Date	14 July 2015	
Tested By	Dylan Hanel	
Overall Test Result	PASS	FAIL
	<input checked="" type="checkbox"/>	<input type="checkbox"/>

2 DC Measurements Section

2.1 Quiescent current draw

External to the chassis under test insert a Fluke Multi-meter in series with each power form and measure the power supply current (test board attached). Record the results in the following table. Mark each measurement as Pass or Fail. Remove meter after completion of the quiescent current measurements.

Table 2 Quiescent Current Draw and Regulated Voltages

Quiescent Current/Voltage	Specified Value	Measured Value	Pass	Fail
+18V Supply	370mA +/- 20mA	370mA	<input checked="" type="checkbox"/>	<input type="checkbox"/>
-18V Supply	-190mA +/- 20mA	-190mA	<input checked="" type="checkbox"/>	<input type="checkbox"/>
+15V Supply (internal)	14.8VDC +/- 200mV	14.8	<input checked="" type="checkbox"/>	<input type="checkbox"/>
-15V Supply (internal)	-15.1VDC +/- 200mV	-15.02	<input checked="" type="checkbox"/>	<input type="checkbox"/>
+V (+24V) Supply	20mA +/- 10mA	20mA	<input checked="" type="checkbox"/>	<input type="checkbox"/>
-V (-24V) Supply	-20mA +/- 10mA	-20mA	<input checked="" type="checkbox"/>	<input type="checkbox"/>

3 Transfer Functions and Configuration Switch Functionality

There are 15 separate control lines to configure the ETM LV ESD Driver. For this reason, a test fixture (D1500130) has been created to allow simple bench-top control. Attach the control board to the chassis under test using a 37 pin D-sub cable. The active state for each option corresponds to the UP position on the individual selector switches. Likewise, the status LEDs are lit when the corresponding function is active. While the term *active* may be vague in some cases, for the most part it should be eventually intuitive. Establish the proper switch state as dictated in the following sections. Start with all switches in the OFF or DOWN position.

3.1 Test Board Functionality

LEDs on the Test Fixture indicate the logic state of each switch function. When each switch is closed (in the UP or ON position), the logic level will be low, and the LED will no longer be lit. With all switches on the D1500130 Test Fixture in the DOWN (D) position, sequentially toggle each switch from D to UP (U) and verify that the LED associated with each function goes out when the switch is U. This verifies that the read-back functionality for each command line is operational. Record the result as PASS or FAIL below.

Table 3, Monitor LEDs

	Pass	Fail
Test Board Monitor LED Functional Check	<input checked="" type="checkbox"/>	<input type="checkbox"/>

3.2 Quadrant Path Input Relay Functional Test

The purpose of the input relay is to provide ON/OFF functionality to the command signals sent to the HV ESD amplifier inputs. Each respective HVLV Switch in the D state results in no connection between the input labeled “ESD Drive from DAC” and the output labeled “ESD Drive to ESD Amp”. Also, in this state, each drive pin to the ESD amplifier is grounded. This next section verifies that functionality. A multimeter is sufficient for a functional check of this path by simply measuring the resistance. As instructed below, measure each function and record PASS or FAIL as appropriate.

Table 4, Input Relay Tests

1 st lead of meter	2 nd lead of meter	Switch State	Predicted Response	Pass	Fail
GND	Drive Output, pin 2	UR Input Relay D then U	Short/100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
GND	Drive Output, pin 10	UR Input Relay D then U	Short/100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
GND	Drive Output, pin 3	LR Input Relay D then U	Short/100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
GND	Drive Output, pin 11	LR Input Relay D then U	Short/100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
GND	Drive Output, pin 4	UL Input Relay D then U	Short/100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
GND	Drive Output, pin 12	UL Input Relay D then U	Short/100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
GND	Drive Output, pin 5	LL Input Relay D then U	Short/100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
GND	Drive Output, pin 13	LL Input Relay D then U	Short/100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 1	Drive Output, pin 1	n/a	short	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 9	Drive Output, pin 9	n/a	short	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 2	Drive Output, pin 2	UR Input Relay D	100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 10	Drive Output, pin 10	UR Input Relay D	100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 3	Drive Output, pin 3	LR Input Relay D	100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 11	Drive Output, pin 11	LR Input Relay D	100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 4	Drive Output, pin 4	UL Input Relay D	100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 12	Drive Output, pin 12	UL Input Relay D	100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 5	Drive Output, pin 5	LL Input Relay D	100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 13	Drive Output, pin 13	LL Input Relay D	100kΩ	<input checked="" type="checkbox"/>	<input type="checkbox"/>

1 st lead of meter	2 nd lead of meter	Switch State	Predicted Response	Pass	Fail
DAC Input, pin 2	Drive Output, pin 2	UR Input Relay U	short	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 10	Drive Output, pin 10	UR Input Relay U	short	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 3	Drive Output, pin 3	LR Input Relay U	short	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 11	Drive Output, pin 11	LR Input Relay U	short	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 4	Drive Output, pin 4	UL Input Relay U	short	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 12	Drive Output, pin 12	UL Input Relay U	short	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 5	Drive Output, pin 5	LL Input Relay U	short	<input checked="" type="checkbox"/>	<input type="checkbox"/>
DAC Input, pin 13	Drive Output, pin 13	LL Input Relay U	short	<input checked="" type="checkbox"/>	<input type="checkbox"/>

3.3 Quadrant Path Main Signal Chain

A signal applied to the “ESD Drive from DAC” connector on the front panel propagates through the Pole-zero stage and eventually emerges at the front panel SHV connectors labeled “To ETM” for each respective quadrant. A Pole-zero bypass function exists to allow modes of operation without the Pole-zero stage present. Also, the last stage in this chain is a selector switch (HVLV Switch) allowing selection between high voltage drive and low voltage drive. Selecting *high voltage* mode will effectively open the main low voltage signal path in this chassis.

In the following section, the transfer function will be taken of the main signal path. The functionality of the HVLV and Pole-zero bypass switches will be verified. Use an SR785 dynamic signal analyzer to obtain the transfer function over the frequency ranges identified in the following data tables. Mark each test as PASS or FAIL as appropriate.

Using an SR785 Dynamic Signal Analyzer in transfer function mode, apply a signal to the front panel connector labeled “ESD Drive from DAC” according to the following pin map. The output for each measurement will be taken from the associated SHV connector indicating “To ETM” for that function:

Table 5, DAC Input Pin Map

Pin (+,-)	Function
1,9	Bias Path Input
2,10	UR Path Input
3,11	LR Path Input
4,12	UL Path Input
5,13	LL Path Input

Using the Test Fixture, for each channel indicated below, set the appropriate configuration switches as prompted. Set all Input Relay switches D. Mark each channel as PASS or FAIL.

For all measurements place the UR/LR Quadrant Select Switches DOWN (D) on the Test Fixture.

Table 6, Main Path Transfer Function

Function	Gain at 10Hz	Phase at 10Hz	Gain at 100Hz	Phase at 100Hz	Pass	Fail
UR Path HVLV - D PZ Bypass - U	-21dB +/- 1dB	-136 +/- 3 deg.	-48dB +/- 3dB	-80 +/- 5 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
UR Path HVLV - D PZ Bypass - D	5.6dB +/- 1dB	-4 +/- 3 deg.	3.8dB +/- 1dB	-31 +/- 3 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
UR Path HVLV - U PZ Bypass - D	OPEN Circuit	OPEN Circuit	OPEN Circuit	OPEN Circuit	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LR Path HVLV - D PZ Bypass - U	-21dB +/- 1dB	-136 +/- 3 deg.	-48dB +/- 3dB	-80 +/- 5 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LR Path HVLV - D PZ Bypass - D	5.6dB +/- 1dB	-4 +/- 3 deg.	3.8dB +/- 1dB	-31 +/- 3 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LR Path HVLV - U PZ Bypass - D	OPEN Circuit	OPEN Circuit	OPEN Circuit	OPEN Circuit	<input checked="" type="checkbox"/>	<input type="checkbox"/>
UL Path HVLV - D PZ Bypass - U	-21dB +/- 1dB	-136 +/- 3 deg.	-48dB +/- 3dB	-80 +/- 5 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
UL Path HVLV - D PZ Bypass - D	5.6dB +/- 1dB	-4 +/- 3 deg.	3.8dB +/- 1dB	-31 +/- 3 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
UL Path HVLV - U PZ Bypass - D	OPEN Circuit	OPEN Circuit	OPEN Circuit	OPEN Circuit	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LL Path HVLV - D PZ Bypass - U	-21dB +/- 1dB	-136 +/- 3 deg.	-48dB +/- 3dB	-80 +/- 5 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LL Path HVLV - D PZ Bypass - D	5.6dB +/- 1dB	-4 +/- 3 deg.	3.8dB +/- 1dB	-31 +/- 3 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LL Path HVLV - U PZ Bypass - D	OPEN Circuit	OPEN Circuit	OPEN Circuit	OPEN Circuit	<input checked="" type="checkbox"/>	<input type="checkbox"/>

3.4 Monitoring Amplifier Transfer Function

The next section verifies the transfer function of the monitoring amplifiers connected to each respective low voltage output channel. The Test Fixture switch positions should be: Input Relay D, HVLV Switch D, PZ Bypass Switch D, Quadrant Select Switches D for each channel under test. Using an SR-785, measure the transfer function from the front panel connector labeled “ESD Drive from DAC. The output for each measurement will be taken differentially from the front panel DB-9 connector labeled “Monitor Outputs to ADC”. The pin map for the monitor channels is as follows:

Table 7, Front Panel Monitor Amplifier Connector Pin Map

Pin (+,-)	Function
1,6	UR Path Input
2,7	LR Path Input
3,8	UL Path Input
4,9	LL Path Input

Table 8

Function	State
All HVLV Switches	D
All Quadrant Select Switches	D
All Input Relay Switches	D
All PZ Bypass Switches	D

Table 9 Monitor Amplifier Transfer Function

Function	Gain at 1kHz	Phase at 1kHz	Pass	Fail
UR Path	-44dB +/- 2dB	-152 +/- 3 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LR Path	-44dB +/- 2dB	-152 +/- 3 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
UL Path	-44dB +/- 2dB	-152 +/- 3 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LL Path	-44dB +/- 2dB	-152 +/- 3 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>

3.5 Parametric Instability (PI) Path Transfer Function

Drive signals to the PI path are applied to a front panel DB-15 connector labeled “PI Correction from DAC”. There are only two input channels for the PI path, but these two channels can be routed to different outputs by use of the Quadrant Selector switch function. The following section of this test procedure verifies the transfer function of the PI path, and checks that the Quadrant Selector switches are functioning correctly. For each of the paths indicated in the following table, configure the test switches as indicated, and verify the transfer function between the front panel PI DB-15 and the associated SHV output.

Table 10, Front Panel PI Input Pin Map

Pin (+,-)	Function
1,9	PI Input 1
2,10	PI Input 2

Table 11

Function	State
All HVLV Switches	D
All Quadrant Select Switches	As Prompted
All Input Relay Switches	D
All PZ Bypass Switches	D

Using an SR-785 in transfer function mode, apply a signal to the PI input and take the output from the “To ETM” SHV output for each path as indicated below. Configure the Quadrant Selector switches on the Test Fixture as prompted in the data table. Mark each test PASS or FAIL as appropriate.

Table 12, PI Path Transfer Functions and Selector Switch Functionality

Input	Gain at 1kHz	Phase at 1kHz	Gain at 30kHz	Phase at 30kHz	Pass	Fail
PI Input 1 (UR/LR Quad Selector D)	“UR to ETM” -37dB +/- 3dB	“UR to ETM” -179 +/- 3 deg.	“UR to ETM” 5.3dB +/- 1dB	“UR to ETM” 32 +/- 6 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
PI Input 1 (UR/LR Quad Selector U)	“UR to ETM” OPEN	“UR to ETM” OPEN	“UR to ETM” OPEN	“UR to ETM” OPEN	<input checked="" type="checkbox"/>	<input type="checkbox"/>
PI Input 1 (UR/LR Quad Selector U)	“LR to ETM” -37dB +/- 3dB	“LR to ETM” -179 +/- 3 deg.	“LR to ETM” 5.3dB +/- 1dB	“LR to ETM” 32 +/- 6 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
PI Input 1 (UR/LR Quad Selector D)	“LR to ETM” Open	“LR to ETM” Open	“LR to ETM” Open	“LR to ETM” Open	<input checked="" type="checkbox"/>	<input type="checkbox"/>
PI Input 2 (UL/LL Quad Selector D)	“UL to ETM” -37dB +/- 3dB	“UL to ETM” -179 +/- 3 deg.	“UL to ETM” 5.3dB +/- 1dB	“UL to ETM” 32 +/- 6 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
PI Input 2 (UL/LL Quad Selector U)	“UL to ETM” OPEN	“UL to ETM” OPEN	“UL to ETM” OPEN	“UL to ETM” OPEN	<input checked="" type="checkbox"/>	<input type="checkbox"/>
PI Input 2 (UL/LL Quad Selector U)	“LL to ETM” -37dB +/- 3dB	“LL to ETM” -179 +/- 3 deg.	“LL to ETM” 5.3dB +/- 1dB	“LL to ETM” 32 +/- 6 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
PI Input 2 (UL/LL Quad Selector D)	“LL to ETM” Open	“LL to ETM” Open	“LL to ETM” Open	“LL to ETM” Open	<input checked="" type="checkbox"/>	<input type="checkbox"/>

3.6 Test Input Transfer Function

A series of BNC inputs are provided on the front panel to inject test signals into the quadrant path signal chains. The following section verifies functionality of the test path by measuring the transfer function from the BNC test input, though to the SHV “To ETM” output associated with each path. Establish the Test Fixture switch settings as indicated in Table 13, and record PASS or FAIL as appropriate in the data table below.

Table 13 Test Input Switch Settings

Function	State
All HVLV Switches	D
All Quadrant Select Switches	D
All Input Relay Switches	D
All PZ Bypass Switches	D

Table 14, Test Path Transfer Function

Input (BNC)	Output (SHV)	Gain at 1kHz	Phase at 1kHz	Pass	Fail
UR Test-In	UR To ETM	-10.1dB +/- 1dB	-66 +/- 5 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LR Test-In	UR To ETM	-10.1dB +/- 1dB	-66 +/- 5 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
UL Test-In	UR To ETM	-10.1dB +/- 1dB	-66 +/- 5 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LL Test-In	UR To ETM	-10.1dB +/- 1dB	-66 +/- 5 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>

3.7 Bias Path Transfer Function

A low-pass filter is included for noise reduction in the Bias Path. This section of the test procedure verifies the transfer function of the Bias Path. Using an SR-785 Dynamic Signal Analyzer in transfer function mode, measure the transfer function from the front panel SHV connector labeled “Bias from ESD Amp” to the front panel SHV connector labeled “Bias to ETM”. Verify the transfer function conforms to the following table, and mark PASS or FAIL accordingly.

Table 15, Bias Path Low-pass Filter Transfer Function

Function	Gain at 10Hz	Phase at 10Hz	Gain at 100Hz	Phase at 100Hz	Pass	Fail
Bias Path	-32dB +/- 2dB	-149 +/- 3 deg.	-70dB +/- 2dB	-181 +/- 3 deg.	<input checked="" type="checkbox"/>	<input type="checkbox"/>

4 Output Noise Analysis

The following section verifies that the output noise of the driver amplifiers is within specification. Only the quadrant drive portions of the signal chains are measured, and of the many possible switch configurations, only the configuration used for low noise control of the test mass will be measured.

Each leg of the differential inputs associated with the “ESD Drive from DAC” DB-15 connector must be shorted to circuit board ground during these noise measurements. Using an SR-785 Dynamic Signal Analyzer in power spectral density mode, measure and record each output noise as prompted and mark each measurement PASS or FAIL as appropriate. Establish the switch settings according to Table 16 prior to measuring the noise.

Table 16, Noise Measurement Test Fixture Switch Settings

Function	State
All HVLV Switches	D
All Quadrant Select Switches	D
All Input Relay Switches	D
All PZ Bypass Switches	U

Table 17 Output Noise Data Table

Output	Noise at 20Hz	Noise at 100Hz	Pass	Fail
UR to ETM (SHV)	< 40nV/√Hz	< 40nV/√Hz	-	-
UR Measured	27nVrms/√Hz	20nVrms/√Hz	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LR to ETM (SHV)	< 40nV/√Hz	< 40nV/√Hz	-	-
LR Measured	27nVrms/√Hz	17nVrms/√Hz	<input checked="" type="checkbox"/>	<input type="checkbox"/>
UL to ETM (SHV)	< 40nV/√Hz	< 40nV/√Hz	-	-
UL Measured	27nVrms/√Hz	20nVrms/√Hz	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LL to ETM (SHV)	< 40nV/√Hz	< 40nV/√Hz	-	-
LL Measured	25nVrms/√Hz	15nVrms/√Hz	<input checked="" type="checkbox"/>	<input type="checkbox"/>

5 High Potential Testing (HIPOT)

Each high voltage channel of the LV ESD Driver (bias, UR, LR, UL, and LL) must operate reliably without high voltage breakdown up to the operating limit of the high voltage power amplifier driving each of these channels (430V). The circuit components used in the LV ESD Driver are rated for continuous service up to 700VDC. A HIPOT test will be performed on each leg at 700VDC. It is important that no more than 700VDC is ever applied to the LV ESD Driver to avoid damage to the high voltage capacitors used in the filter circuitry.

Establish the switch settings as indicated in Table 18 below and using a current limited HIPOT tester similar to the Vitrek Inc. V74 HIPOT Tester, test the each channel and mark PASS or FAIL as appropriate. Suggested V74 settings are 700VDC Max, 10 second ramp, 2 second dwell, and 1mA trip threshold.

Table 18 HIPOT Test, Test Fixture Switch Settings

Function	State
All HVLV Switches	U
All Quadrant Select Switches	D
All Input Relay Switches	D
All PZ Bypass Switches	D

Table 19, 700VDC HIPOT Test Results

Input (SHV)	Pass	Fail
BIAS To ETM	<input checked="" type="checkbox"/>	<input type="checkbox"/>
UR To ETM	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LR To ETM	<input checked="" type="checkbox"/>	<input type="checkbox"/>
UL To ETM	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LL To ETM	<input checked="" type="checkbox"/>	<input type="checkbox"/>

6 HV ESD Amplifier Remote Reset Function

A DB-9 Female connector labeled “Reset to ESD Amp” exists on the front panel of the LV ESD Driver. This connector delivers a reset signal to the HV ESD Amplifier Chassis to facilitate remote ENABLE and DISABLE functions for the HV ESD Amplifier. A simple set of resistance measurements are sufficient to verify the functionality of this feature. Using a multimeter, verify the following connections are as specified and exercise the Test Fixture switches as indicated. Mark each measurement as PASS or FAIL as appropriate.

Table 20

1 st lead of meter	2 nd lead of meter	HV ESD ON/OFF Switch State	Predicted Response	Pass	Fail
Pin 2	Pin 3	D	OPEN	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Pin 2	Pin 3	U	SHORT	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Pin 2	Pin 8	U	22k Ω	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Pin 2	Pin 9	U	22k Ω	<input checked="" type="checkbox"/>	<input type="checkbox"/>