PSoC® Creator™
Project Datasheet for CPSSynch

Creation Time: 01/21/2015 11:44:00
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Project: CPSSynch

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Table of Contents

1 Overview

The Cypress PSoC 3 is a family of 8-bit devices with the following characteristics:

- An 8-bit single cycle pipelined 8051 processor, running up to 67 MHz, with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor.
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, CAN and I2C
- Analog subsystem that includes configurable switched (SC) and continuous time (CT) blocks, up to 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, op amps, comparators, PGAs, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C38 family member PSoC 3 device. For details on all the systems listed above, please refer to the PSoC 3 Technical Reference Manual .

Figure 1. CY8C38 Device Family Block Diagram

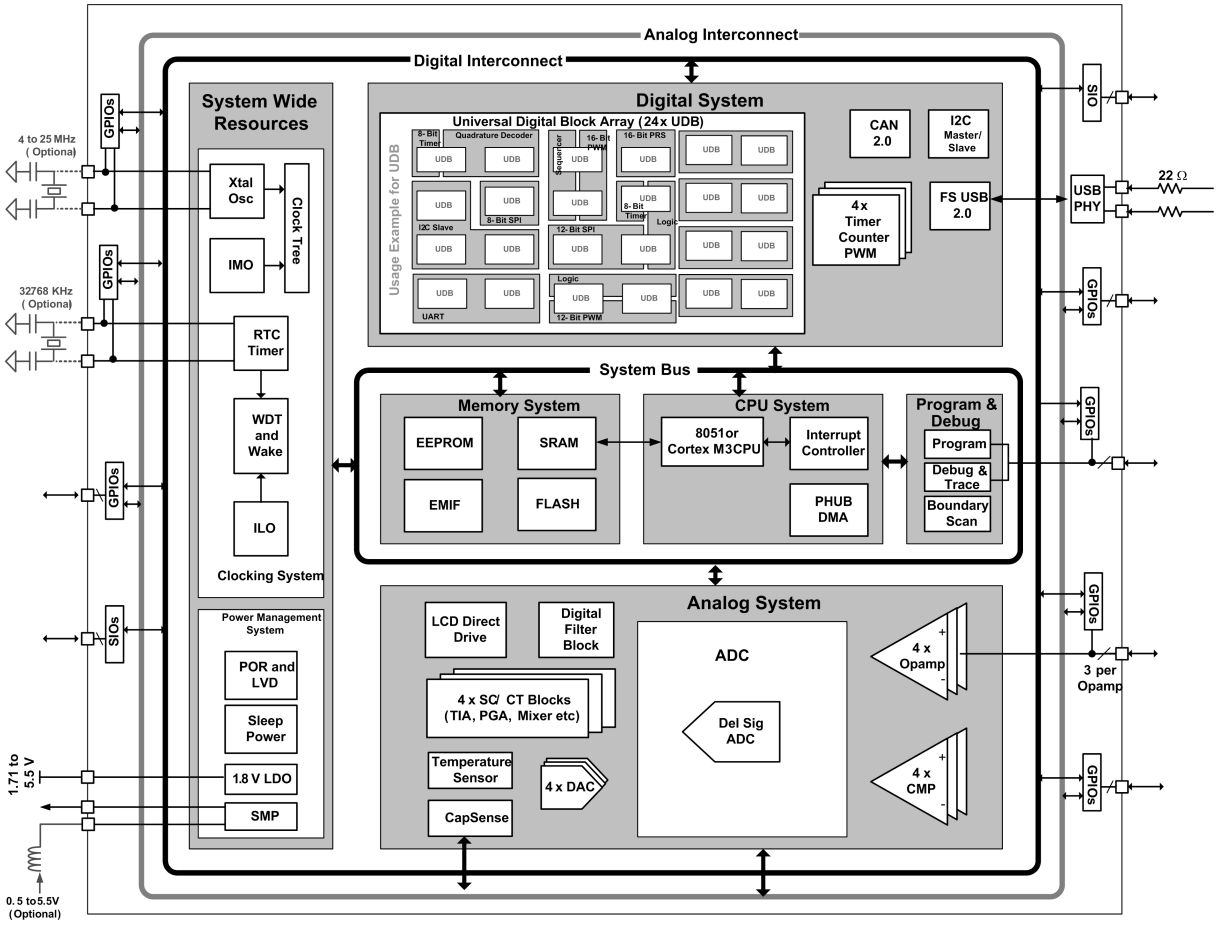


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Architecture	PSoC 3
Family	CY8C38
CPU speed (MHz)	67
Flash size (kBytes)	64
SRAM size (kBytes)	8
EEPROM size (Bytes)	2048
Trace Buffer (kBytes)	4
Vdd range (V)	1.7 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x1E028069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by BUS_CLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

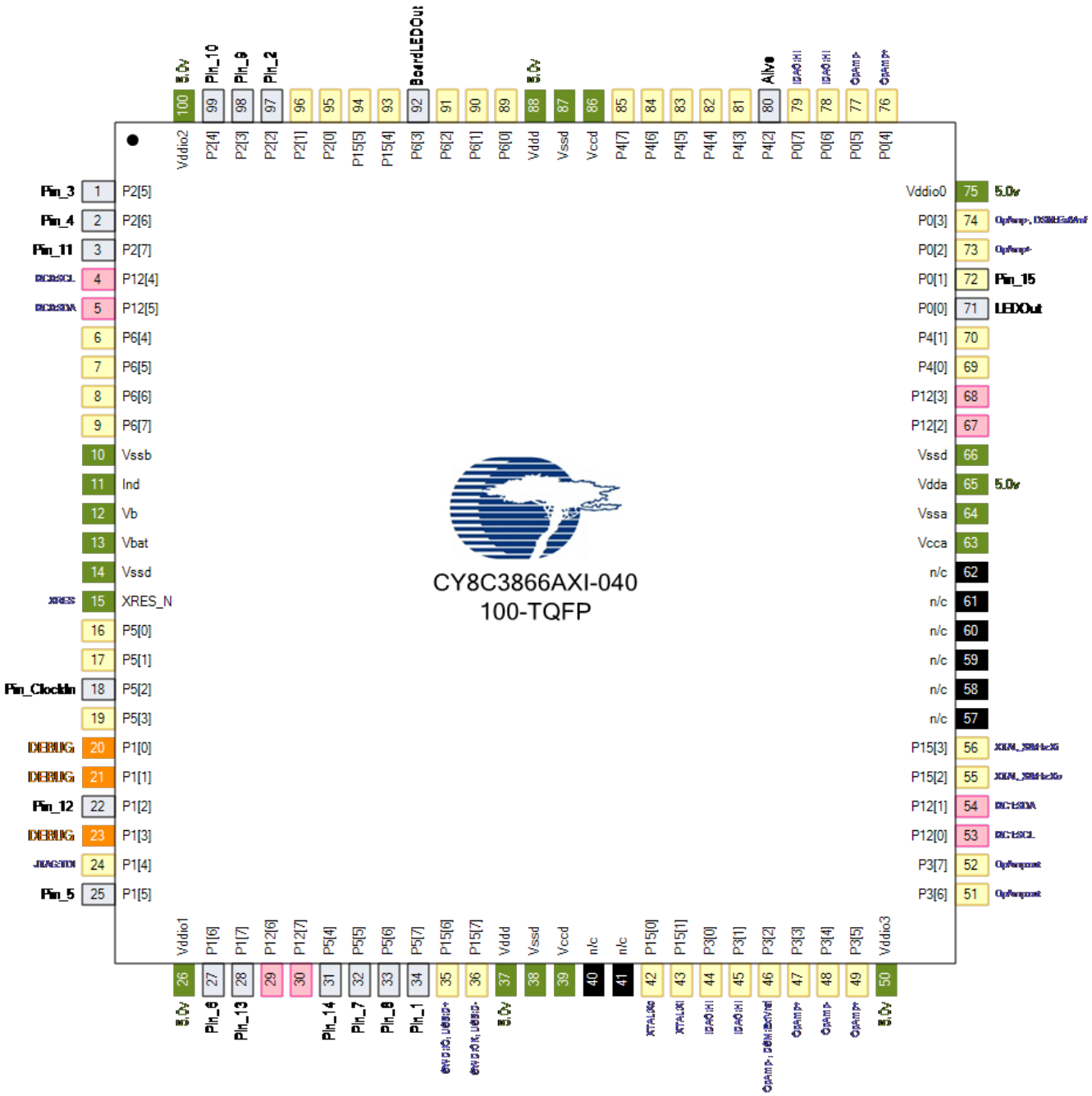
Table 2. Device Resources

Name	Resources in Use	Total Resources Available
Digital clock dividers	1 (12.5%)	8
Analog clock dividers	0 (0.0%)	4
Pins	22 (30.6%)	72
UDB Macrocells	8 (4.2%)	192
UDB Unique Pterms	12 (3.1%)	384
UDB Datapath Cells	0 (0.0%)	24
UDB Status Cells	1 (4.2%)	24
UDB Control Cells	0 (0.0%)	24
DMA Channels	0 (0.0%)	24
Interrupts	0 (0.0%)	32
DSM Fixed Blocks	0 (0.0%)	1
VIDAC Fixed Blocks	0 (0.0%)	4
SC Fixed Blocks	0 (0.0%)	4
Comparator Fixed Blocks	0 (0.0%)	4
Opamp Fixed Blocks	0 (0.0%)	4
CapSense Buffers	0 (0.0%)	2
CAN Fixed Blocks	0 (0.0%)	1
Decimator Fixed Blocks	0 (0.0%)	1
I2C Fixed Blocks	0 (0.0%)	1
Timer Fixed Blocks	0 (0.0%)	4
DFB Fixed Blocks	0 (0.0%)	1
USB Fixed Blocks	0 (0.0%)	1
LCD Fixed Blocks	0 (0.0%)	1
EMIF Fixed Blocks	0 (0.0%)	1
LPF Fixed Blocks	0 (0.0%)	2

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	Pin_3	Dgtl Out	Strong drive	HiZ Analog Unb
2	P2[6]	Pin_4	Dgtl Out	Strong drive	HiZ Analog Unb
3	P2[7]	Pin_11	Dgtl Out	Strong drive	HiZ Analog Unb
4	P12[4]	SIO [unused]			HiZ Analog Unb
5	P12[5]	SIO [unused]			HiZ Analog Unb
6	P6[4]	GPIO [unused]			HiZ Analog Unb
7	P6[5]	GPIO [unused]			HiZ Analog Unb
8	P6[6]	GPIO [unused]			HiZ Analog Unb
9	P6[7]	GPIO [unused]			HiZ Analog Unb
10	Vssb	Vssb	Power		
11	Ind	Power			
12	Vb	Vb	Power		
13	Vbat	Vbat	Power		
14	Vssd	Vssd	Power		
15	XRES_N	XRES_N	Power		
16	P5[0]	GPIO [unused]			HiZ Analog Unb
17	P5[1]	GPIO [unused]			HiZ Analog Unb
18	P5[2]	Pin_ClockIn	Dgtl In	HiZ digital	HiZ Analog Unb
19	P5[3]	GPIO [unused]			HiZ Analog Unb
20	P1[0]	GPIO [unused]			HiZ Analog Unb
21	P1[1]	GPIO [unused]			HiZ Analog Unb
22	P1[2]	Pin_12	Dgtl Out	Strong drive	HiZ Analog Unb
23	P1[3]	GPIO [unused]			HiZ Analog Unb
24	P1[4]	GPIO [unused]			HiZ Analog Unb
25	P1[5]	Pin_5	Dgtl Out	Strong drive	HiZ Analog Unb
26	Vio1	Vio1	Power		
27	P1[6]	Pin_6	Dgtl Out	Strong drive	HiZ Analog Unb
28	P1[7]	Pin_13	Dgtl Out	Strong drive	HiZ Analog Unb
29	P12[6]	SIO [unused]			HiZ Analog Unb
30	P12[7]	SIO [unused]			HiZ Analog Unb
31	P5[4]	Pin_14	Dgtl Out	Strong drive	HiZ Analog Unb
32	P5[5]	Pin_7	Dgtl Out	Strong drive	HiZ Analog Unb
33	P5[6]	Pin_8	Dgtl Out	Strong drive	HiZ Analog Unb
34	P5[7]	Pin_1	Dgtl Out	Strong drive	HiZ Analog Unb
35	P15[6]	USB [unused]			HiZ Analog Unb
36	P15[7]	USB [unused]			HiZ Analog Unb
37	Vddd	Vddd	Power		
38	Vssd	Vssd	Power		
39	Vccd	Vccd	Power		
42	P15[0]	GPIO [unused]			HiZ Analog Unb
43	P15[1]	GPIO [unused]			HiZ Analog Unb
44	P3[0]	GPIO [unused]			HiZ Analog Unb
45	P3[1]	GPIO [unused]			HiZ Analog Unb
46	P3[2]	GPIO [unused]			HiZ Analog Unb
47	P3[3]	GPIO [unused]			HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
48	P3[4]	GPIO [unused]			HiZ Analog Unb
49	P3[5]	GPIO [unused]			HiZ Analog Unb
50	Vio3	Vio3	Power		
51	P3[6]	GPIO [unused]			HiZ Analog Unb
52	P3[7]	GPIO [unused]			HiZ Analog Unb
53	P12[0]	SIO [unused]			HiZ Analog Unb
54	P12[1]	SIO [unused]			HiZ Analog Unb
55	P15[2]	GPIO [unused]			HiZ Analog Unb
56	P15[3]	GPIO [unused]			HiZ Analog Unb
63	Vcca	Vcca	Power		
64	Vssa	Vssa	Power		
65	Vdda	Vdda	Power		
66	Vssd	Vssd	Power		
67	P12[2]	SIO [unused]			HiZ Analog Unb
68	P12[3]	SIO [unused]			HiZ Analog Unb
69	P4[0]	GPIO [unused]			HiZ Analog Unb
70	P4[1]	GPIO [unused]			HiZ Analog Unb
71	P0[0]	LEDOut	Dgtl Out	Strong drive	HiZ Analog Unb
72	P0[1]	Pin_15		HiZ analog	HiZ Analog Unb
73	P0[2]	GPIO [unused]			HiZ Analog Unb
74	P0[3]	GPIO [unused]			HiZ Analog Unb
75	Vio0	Vio0	Power		
76	P0[4]	GPIO [unused]			HiZ Analog Unb
77	P0[5]	GPIO [unused]			HiZ Analog Unb
78	P0[6]	GPIO [unused]			HiZ Analog Unb
79	P0[7]	GPIO [unused]			HiZ Analog Unb
80	P4[2]	Alive	Dgtl In	Res pull down	HiZ Analog Unb
81	P4[3]	GPIO [unused]			HiZ Analog Unb
82	P4[4]	GPIO [unused]			HiZ Analog Unb
83	P4[5]	GPIO [unused]			HiZ Analog Unb
84	P4[6]	GPIO [unused]			HiZ Analog Unb
85	P4[7]	GPIO [unused]			HiZ Analog Unb
86	Vccd	Vccd	Power		
87	Vssd	Vssd	Power		
88	Vddd	Vddd	Power		
89	P6[0]	GPIO [unused]			HiZ Analog Unb
90	P6[1]	GPIO [unused]			HiZ Analog Unb
91	P6[2]	GPIO [unused]			HiZ Analog Unb
92	P6[3]	BoardLEDOut	Dgtl Out	Strong drive	HiZ Analog Unb
93	P15[4]	GPIO [unused]			HiZ Analog Unb
94	P15[5]	GPIO [unused]			HiZ Analog Unb
95	P2[0]	GPIO [unused]			HiZ Analog Unb
96	P2[1]	GPIO [unused]			HiZ Analog Unb
97	P2[2]	Pin_2	Dgtl Out	Strong drive	HiZ Analog Unb
98	P2[3]	Pin_9	Dgtl Out	Strong drive	HiZ Analog Unb
99	P2[4]	Pin_10	Dgtl Out	Strong drive	HiZ Analog Unb
100	Vio2	Vio2	Power		

Abbreviations used in Table 3 have the following meanings:

- Dgtl Out = Digital Output
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- HiZ digital = High impedance digital

- HiZ analog = High impedance analog
- Res pull down = Resistive pull down

2.2 Software Pins

Table 4 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 4. Software Pins

Name	Port	Type	Reset State
Alive	P4[2]	Dgtl In	HiZ Analog Unb
BoardLEDOut	P6[3]	Dgtl Out	HiZ Analog Unb
LEDOut	P0[0]	Dgtl Out	HiZ Analog Unb
Pin_1	P5[7]	Dgtl Out	HiZ Analog Unb
Pin_10	P2[4]	Dgtl Out	HiZ Analog Unb
Pin_11	P2[7]	Dgtl Out	HiZ Analog Unb
Pin_12	P1[2]	Dgtl Out	HiZ Analog Unb
Pin_13	P1[7]	Dgtl Out	HiZ Analog Unb
Pin_14	P5[4]	Dgtl Out	HiZ Analog Unb
Pin_15	P0[1]		HiZ Analog Unb
Pin_2	P2[2]	Dgtl Out	HiZ Analog Unb
Pin_3	P2[5]	Dgtl Out	HiZ Analog Unb
Pin_4	P2[6]	Dgtl Out	HiZ Analog Unb
Pin_5	P1[5]	Dgtl Out	HiZ Analog Unb
Pin_6	P1[6]	Dgtl Out	HiZ Analog Unb
Pin_7	P5[5]	Dgtl Out	HiZ Analog Unb
Pin_8	P5[6]	Dgtl Out	HiZ Analog Unb
Pin_9	P2[3]	Dgtl Out	HiZ Analog Unb
Pin_ClockIn	P5[2]	Dgtl In	HiZ Analog Unb
Power	Ind		

Abbreviations used in Table 4 have the following meanings:

- Dgtl In = Digital Input
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 5. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Clear SRAM During Startup	True
Unused Bonded IO	Allow but warn

3.2 System Debug Settings

Table 6. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 7. System Operating Conditions

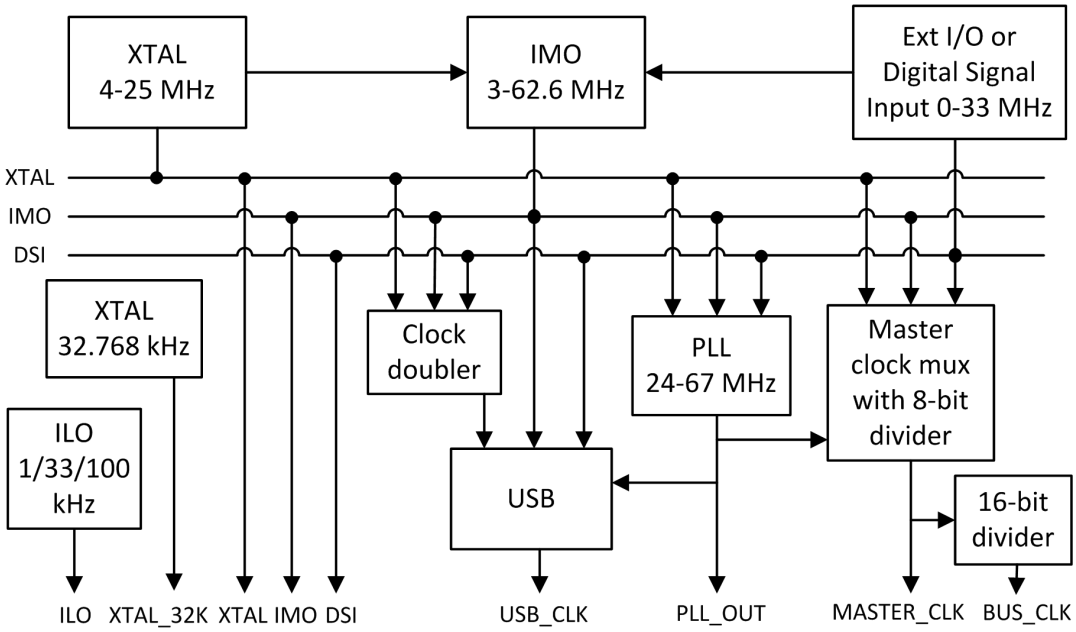
Name	Value
Vddd (V)	5.0
Vdda (V)	5.0
Variable Vdda	False
Vddio0 (V)	5.0
Vddio1 (V)	5.0
Vddio2 (V)	5.0
Vddio3 (V)	5.0
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 62.6 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 67 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 67 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 8 lists the system clocks used in this design.

Table 8. System Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	0	35.5	±0	True	True
MASTER_CLK	DIGITAL	IMO	0	35.5	±0	True	True
Digital Signal	DIGITAL	CLK_In	35.5	35.5	±0	False	True
XTAL 32kHz	DIGITAL		0.0328	0	±0	False	False
XTAL	DIGITAL		10	0	±0	False	False
ILO	DIGITAL		0	0.001	-50,+100	True	True
PLL_OUT	DIGITAL	Digital Signal	10	0	±0	True	False
IMO	DIGITAL	Digital Signal	35.5	35.5	±0	True	True
USB_CLK	DIGITAL	IMO	48	0	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

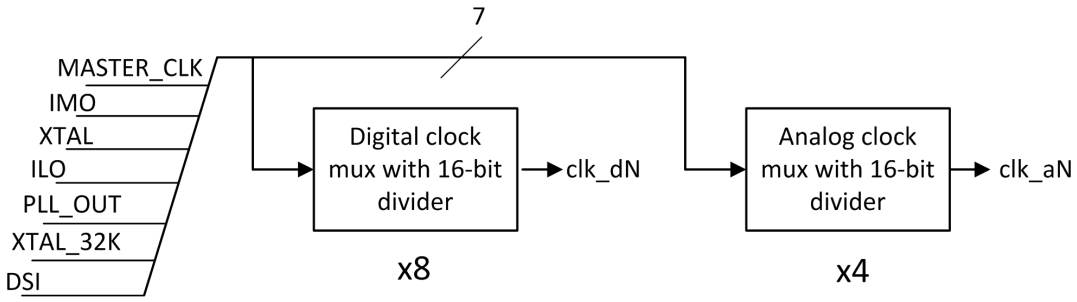


Table 9 lists the local clocks used in this design.

Table 9. Local Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
Clock_2	DIGITAL	MASTER_CLK	0	1.5435	±0	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 3 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - o CyPLL API routines
  - o CyIMO API routines
  - o CyILO API routines
  - o CyMaster API routines
  - o CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains no interrupt components.

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 3 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 10 lists the Flash protection settings for your design.

Table 10. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0xFFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - External read protect (Factory upgrade)
- R - External write protect (Field upgrade)
- W - Full Protection

For more information on Flash memory and protection, please refer to:

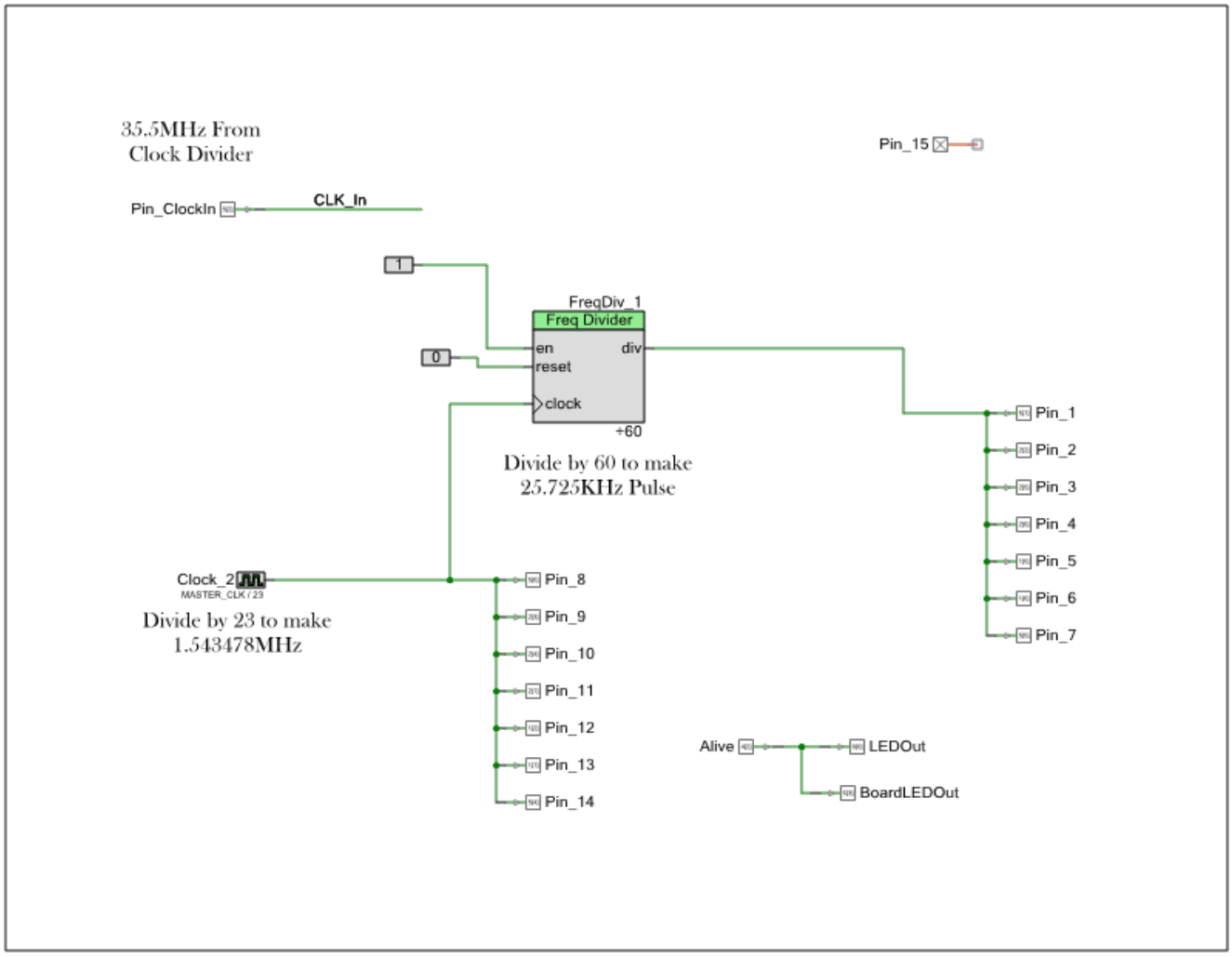
- Flash Protection chapter in the PSoC 3 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyFlash API routines
  - CyWrite API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance FreqDiv_1 (type: FreqDiv_v1_0)

8 Components

8.1 Component type: FreqDiv [v1.0]

8.1.1 Instance FreqDiv_1

Description: Frequency Divider
Instance type: FreqDiv [v1.0]
Datasheet: online component datasheet for FreqDiv

Table 11. Component Parameters for FreqDiv_1

Parameter Name	Value	Description
Divider	60	The divider used to generate the div output from the clock input.
HighPulseTime	59	Number of clock cycles each clock period that the div output is high. 0 indicates 50% duty cycle.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 3 register map is covered in the PSoC 3 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 3 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 3 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 3 Technical Reference Manual
  - Cache chapter in the System Reference Guide