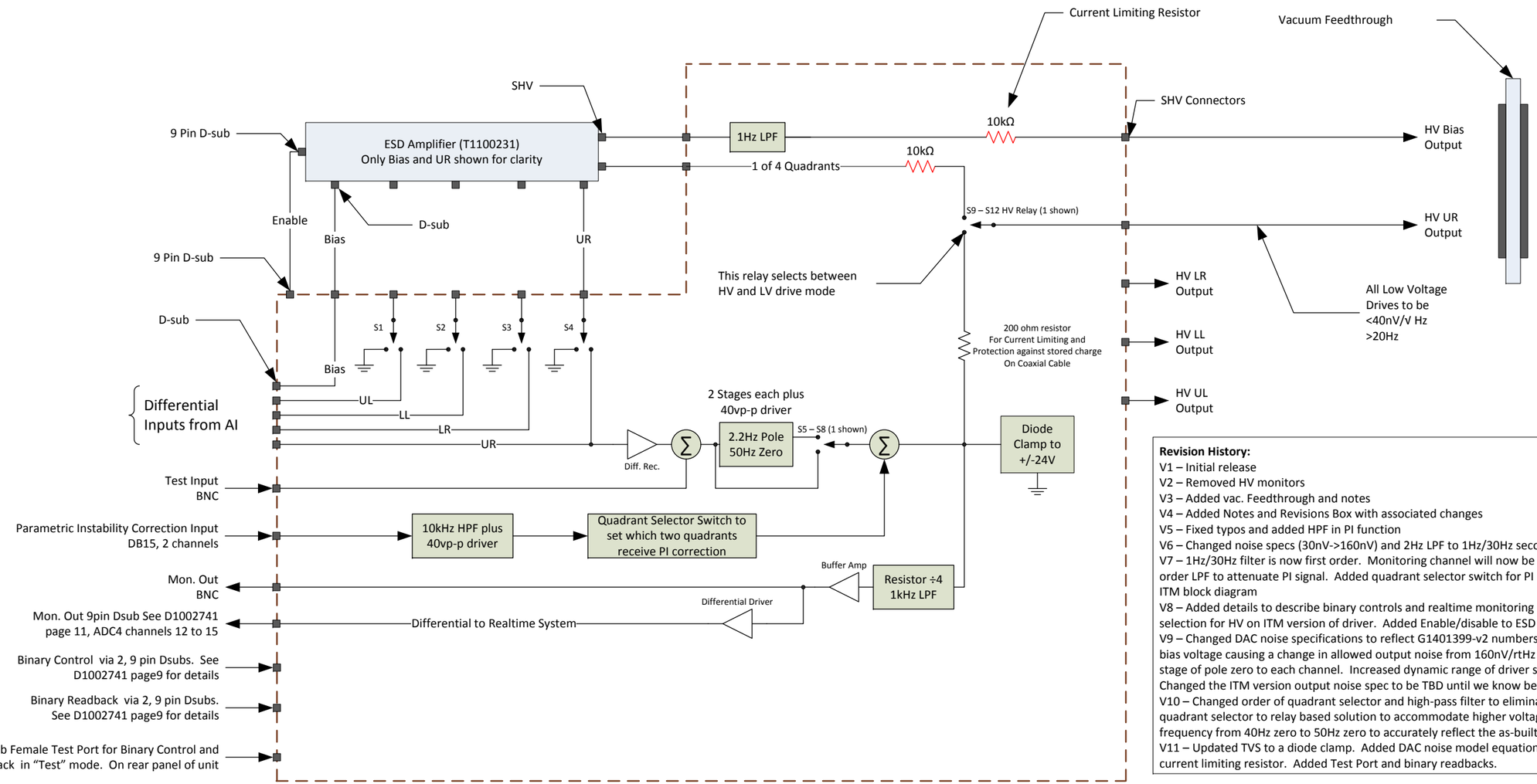
ETM ESD Low Voltage Driver and Monitor



Revision History:
V1 – Initial release
V2 – Removed HV monitors
V3 – Added vac. Feedthrough and notes
V4 – Added Notes and Revisions Box with associated changes
V5 – Fixed typos and added HPF in PI function
V6 – Changed noise specs (30nV->160nV) and 2Hz LPF to 1Hz/30Hz second order filters cascaded
V7 – 1Hz/30Hz filter is now first order. Monitoring channel will now be just a resistive divider and first order LPF to attenuate PI signal. Added quadrant selector switch for PI input. Added second sheet for ITM block diagram
V8 – Added details to describe binary controls and realtime monitoring channels. Added polarity selection for HV on ITM version of driver. Added Enable/disable to ESD HV Amp on ETM version
V9 – Changed DAC noise specifications to reflect G1401399-v2 numbers and updated the operational bias voltage causing a change in allowed output noise from 160nV/rtHz to 40nV/rtHz. Added another stage of pole zero to each channel. Increased dynamic range of driver stages to allow 40vp-p operation. Changed the ITM version output noise spec to be TBD until we know better.
V10 – Changed order of quadrant selector and high-pass filter to eliminate two stages. Changed quadrant selector to relay based solution to accommodate higher voltages. Updated pole-zero frequency from 40Hz zero to 50Hz zero to accurately reflect the as-built schematic.
V11 – Updated TVS to a diode clamp. Added DAC noise model equation. Updated 200 ohm series current limiting resistor. Added Test Port and binary readbacks.

Bit Level Binary Control List
1. 4 channels input switching for signals going to ESD HV amp
2. 2 channels PI Quadrant select
3. 4 channels of de-whitening bypass
4. 1 channel for ESD HV amp remote ON/OFF (the ESD HV amp needs +5V applied for less than 1 second will toggle the state)
5. 4 channels HV Relay control to switch from HV to LV mode

Total Count 15 channels. There are 8 channels per SUS binary output 9 pin D-sub. Per D1002741 page9, there are plenty of extra binary IO channels

$$v_n = \sqrt{300^2(50\,\mathrm{Hz}/f)^2 + 300^2}\ \frac{nV}{\sqrt{\mathrm{Hz}}}$$

DAC Noise Model from G1401399-v2

D1400301-v11
R. Abbott, P. Fritschel, C. Adams

Bit Level Binary Control List
1. 1 channel HV bias polarity Select
2. 2 channels PI Quadrant select
3. 4 channels of de-whitening bypass

Total Count 7 channels. There are 8 channels per SUS binary output 9 pin D-sub, per D1100022 page 12, 13, and 14, there are plenty of spare channels

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