Discussion Slides for Integrating O5 BHD SUS Electronics into Existing O4 SUS Electronics Layout

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PART I: Design Principles and Naming Conventions

The aspects of G2301306 have different audiences, and it covers a LOT. So I've split the document into 3 parts for easier human consumption and so you can have the design principles and naming choices open while you peruse the details

Here's the table of contents.

The part number will also be here throughout each .pdf

Design Motivation Highlights, Key Overall Decisions, and Driving Principles

- **Thinking about the *entire* integrated signal chains and future controls and automation for *all* SUS as a complete picture**
  >> Hardware - electronics - software - controls co-design
  >> there's no such thing as "optimize," but at least find a solution that "works."
  >> We're talking **from in-vac sensor/actuator arrangement to front-end computer core assignment with the eventual digital control and automation system in mind**.

- BSC123 System is *very* full. HAM34 IO chassis, and supporting SUS racks are pretty empty.
  >> Move BSC2 SUS to into HAM34 system to create B2H34 System Covered in Part II
  >> Do to error in DAC channel count and lack of IO chassis space, as of -v6, **Plan A is to use 16ch DACs to drive HRTS top masses, and down grade MC2/PR2/SR2 top masses to 16-bit such that BS M1, M2, and now M3 stages retain the best performance with 20-bit DACs (see Part II page 5).**
  >> Plan B is to incorporate the (hopefully) incoming 32-bit, 32 ch DAC
  >> 32-bit DAC is lower noise than 20-bit DACs.

- HAM56 System is *very* full, and is only going to get worse with all the incoming HAM6 SUS.
  >> Segregate H5 and H6 SUS, and move H6 SUS to a new H6 system Covered in Part III
  >> Confirmed we'll have 2 IO chassis per site available by O5
  >> Brand new drawing number for H6, and take SUS-M2 out of D2000202
  >> Need 2x new H6 chassis and and some new cards
  >> In O4, we sacrificed not reading out coil driver monitor channels because we didn't have the IO chassis space. Now's our chance to remedy this.
  >> H6 system will live in remote MER rack SUS-M2 and new SUS-R7 (next to ISC-R3 and ISC-R5 by HAM6)

- Try to move as few chassis as possible (only BS and H6 chassis will move), accept some cable re-wiring because we're up-cycling and space limited.
  >> There will need to be some new chassis and cards

- Preparing ahead of time for "Detector Improvements" that are under discussion
  >> Running under the assumption that at least BS will have M2 HoQIs or SmarActs, and with the move of BS from BSC123, that means there'll be room for QUADs to get them too.
  >> Running under the assumption that the existing OFI SUS will get scrapped, and replaced with OMCS (and renamed to be **OFDS** for Output Faraday Double Suspension)
  >> Leaving rack space for HoQI / SmarAct laser conditioning

- Attention paid to DuoTone / Timing signals — the last two channels on ADC0 and the last channel DAC0 must not be used
  >> in aLIGO SUS missed this requirement from CDS/Timing, and resulted in some post-install rearrangement of cables.

- Acquire DCOIL and PZT drive monitor signals for the first time
  >> These HXDS M2 actuators and their drivers came too late in the schedule to properly plan for ADC space to monitor these drive signals. We can fix that now in O5.

Issues with A+ O5 Final Design that this Review has Uncovered and Addressed

(1) **The channel count capability for a 20-bit DAC was over-estimated by a factor of two (a problem that was evident even in O4, and rectified using operational spares)**

:: The A+ electronics design was put together with a 18-bit DACs; they've been replaced with 20-bit DACs.
:: 18- and 20-bit DACs have 8 channels per card, and the A+ O4 and O5 design had assumed that they had 16 channels, and counted DAC cards and AI chassis accordingly.
:: Not only did has the number of DAC channels been underestimated, the space for DAC cards within IO chassis had not been considered.

>> **In order to rectify this, this review suggests we buy 16-bit DACs (and buy and/or convert associated AI chassis).**
. The associate financial cost impact for this is being evaluated in E2300309. The funding source to rectify the discrepancy is still to-be-determined.

>> **How will this "downgrade" impact the noise performance?**
. The vast majority of A+ O5 HAM6 SUS have examples in play in the IFO already, driven by 16-bit DACs — HXDS, HTTS, and BHSS — and the downgrade should be unimpactful.
. The BBSS, HRTS (LO1, LO2, LO3, OBS), and HATS (OM0) have the most stringent requirements.
. For the BBSS M3 stage, we can re-arrange existing channel assignments to ensure that all stages of the BBSS remain driven by 20-bit DACs.
. The actuation noise requirements and subsequent estimates of noise performance for HRTS and HATS — shown in Section 15.1 of T2000581 — were done using 10 and 30 Hz points of the 18-bit DAC noise model from E1800243.
. Both the noise model and real-world IFO experience show us that the DAC noise is not that different (at most a factor of 1.5) at those frequencies for 16- and 18-bit DACs.
. **"Figures" (which are really Tables) 33 and 34 in Section 15.1 of T2000581 conclude that there is an order-of-magnitude or more headroom between requirements and expected performance, so an extra 50% noise increase from the downgrade from 18- to 16-bit DAC will be unimpactful.**

(2) Coil driver monitor channels were over-looked in the ADC channel count (a problem that was evident in O4, and we simply sacrificed monitoring this channels.)

>> More ADC cards (and associated AA chassis) are required.
. The associate financial cost impact for this is being evaluated in E2300309. The funding source to rectify the discrepancy is still to-be-determined.
>> This review shows that there's enough IO chassis space available.

(3) Misunderstandings and miscommunications that had resulted in some panic during this review:

- For a while (up to G2301306-v6), Jeff had assumed that HRTS top masses were driven by TTOP drivers, and HATS bottom mass was driven by a TACQ driver.
This was incorrect, the original plan has been uncovered, and will work.
>> As per Section 15.1 of T2000581, all HRTS are driven by HAM-A drivers, and the one HATS, OM0, M3 stage will be driven by a modified HAM-A driver.

- For a while (up to -v6), Jeff had assumed that the HRTS (and HATS) were driven by TTOP drivers and thus needed remote low-pass switch-ability.
This was incorrect, the original plan has been uncovered, and will work.
>> Since the vast majority of A+ O5 SUS are driven with HAM-A drivers whose low-pass filters are permanently jumpered to "LP ON," we do not need the large quantity of binary IO chassis or cards that had been previously advertised.

- For a while (up to -v6), Jeff's mistake regarding TTOP drivers meant that "we needed" ADC coverage for 4x4 coil driver monitor channels, and the special D1000721 coil driver monitor AA chassis
This was incorrect, HAM-A drivers only need 4x1 V-MONs, which drastically reduces the ADC channel count need, and "simplifies" the AA chassis to a standard D0902783

- For a while (up to -v6), record was lost as to which suspension stages OSEM sensors were to be readout by "dual" 8ch sat amps vs. "single" 4ch sat amps, and it seemed up-for-debate as to which would be better to use given the apparent pros of the "dual" 8ch chassis.
This is incorrect, the original plan has been uncovered, and will work.
>> As of -v8 and re-inventory of what was bought and delivered to the sites (E2300309), we are no longer confused and have explicit assignment of 8ch vs 4ch sat amps to each A+ O5 suspension stage.

A Proposed Re-naming of Suspended Optics for Better Integration

- I suggest (and have completed this document with) the following renaming map from the names used in the UK design documentation :

BHDBS1 >> **LO1**,
BHDM1 >> **LO2**,
BHDL1 >> **LO3**
BHDBS2 >> **OBS** (for “output beam splitter”)
OM0 (stays OM0)
OMAS and OMBS >> **OMA1** and **OMB1**
OMA1 and OMB1 >> **OMA2** and **OMB2**
OMA2 and OMB2 >> **OMA3** and **OMB3**
45-TT1 and 45-TT2 >> **AM1** and **AM2**
BHSS >> **OMCAB**

(for optics along the **L**ocal **O**scillator path)

Note that “BBSS” suspension type will still suspend an optic name with the name “BS.” So we need the clear distinction between BS and OBS.

(for **A**nti-symmetric-port **M**irror”, like
- RMs are “Reflected-port Mirrors”
- IMs are “Input Mirrors” and
- OMs are “Output Mirrors”)

- **As of -v4** — Naming OM0 suspension type to be HAM **Alignment** Triple Suspension (HATS); it’s got DCOILs on the bottom stage. This will distinguish it from LO1, LO2, LO3, and LOBS which only have top mass control (and thus are “only” HAM Relay Triple Suspensions, HRTS)
(Previous -v1—v3 idea was HAM Dither Triple Suspension HDTS, but deemed to close to HAM Thermal Double Suspension HTDS.)

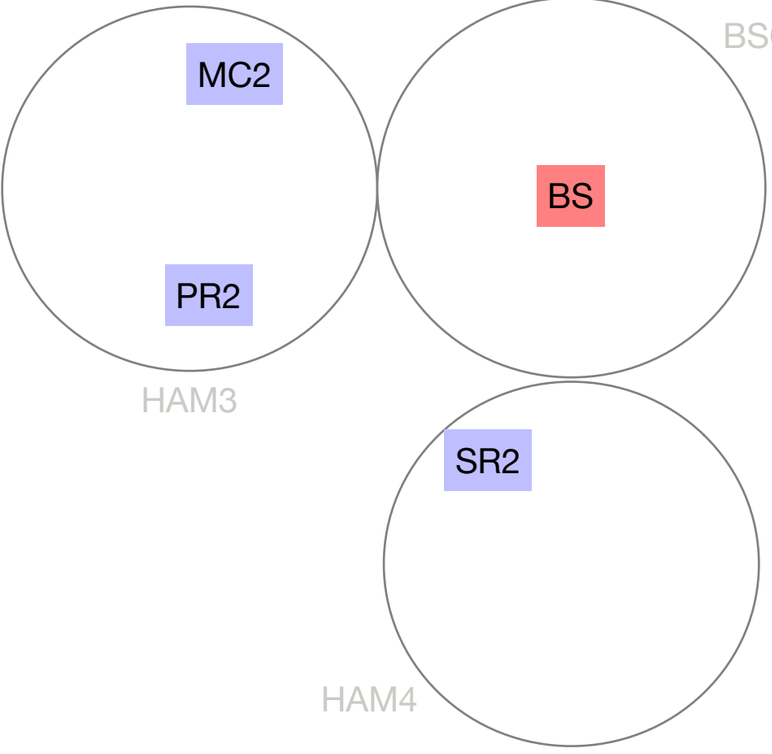
- **As of -v4** — Post-name change OM(A/B)3 have a combination of dither and mode matching control (PZT or Thermal). Had been called HAM Relay Double Suspension (**HRDS**) early on, but now more clear to call this HAM **Combined** Double Suspension (**HCDS**).

Design Doc Naming Convention Pros

- Clearly describes the optic type (BS, M, L)
  >> Good reminder when optical modeling where you need to know the optical function
  >> Helps during procurement of optics since each must be unique
- Differentiates new O5 A+ optics from old O4 and prior optics via “BHD” moniker
- Already have a lot of optical and mechanical systems tools products that use this convention (Zemax, Solidworks)

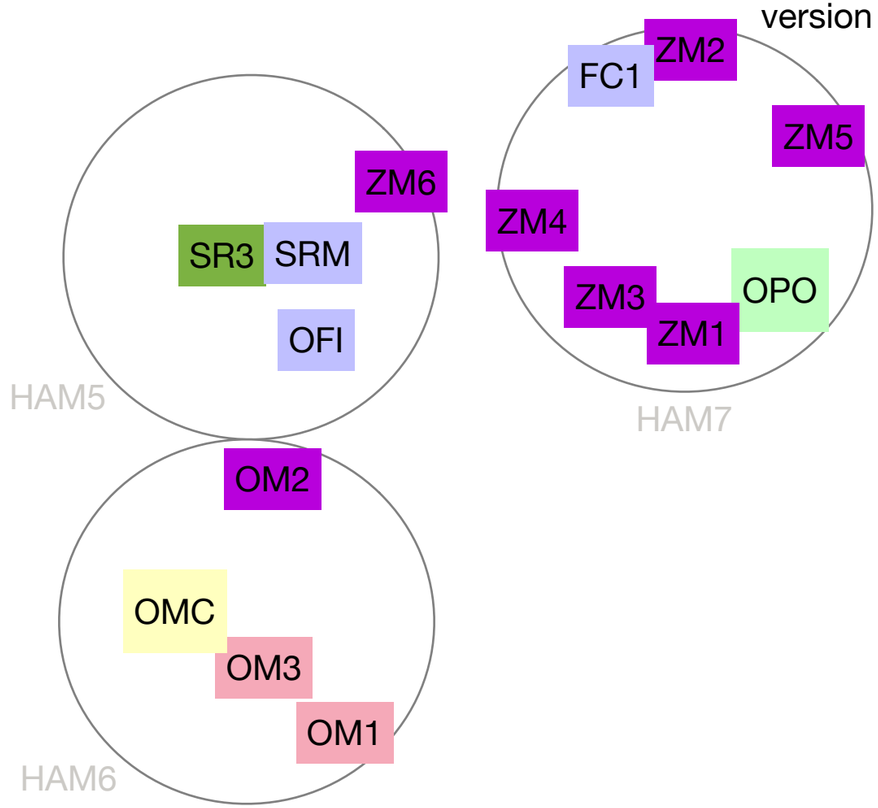
Proposed Integrated Naming Convention Pros

- (Where possible) named like existing suspensions, after optic *path*, not optic type
  >> Simple, memorable name
  >> In new HAM6, gives ties to equivalent optics’ historical name
- Named in numerical sequence by optical path
  >> gives immediate impression of “directional flow”
- A reduced number of characters (in all cases except for OMCAB)
  >> good for controls channel names, automation,
  >> easy “copy and paste” in large-scale documentation where there’s no functional difference *other* than optic type
- Lists of only 1 item (BHDL**1**, BHDM**1**, OM(A/B)**S**) don’t exist
  >> another character reduction, and leaving just “M” and “L” would be awkward
- Clear differentiation between “*instantiation* of suspension type” and “suspension type” (i.e. no BHSS named BHSS) as is true for all existing suspensions
  >> was an issue in the past when OMC was named OMC, and OPO was named OPO
  >> like other suspension types, allows for future extensible copies of the same suspensions type without confusing which instantiation is which

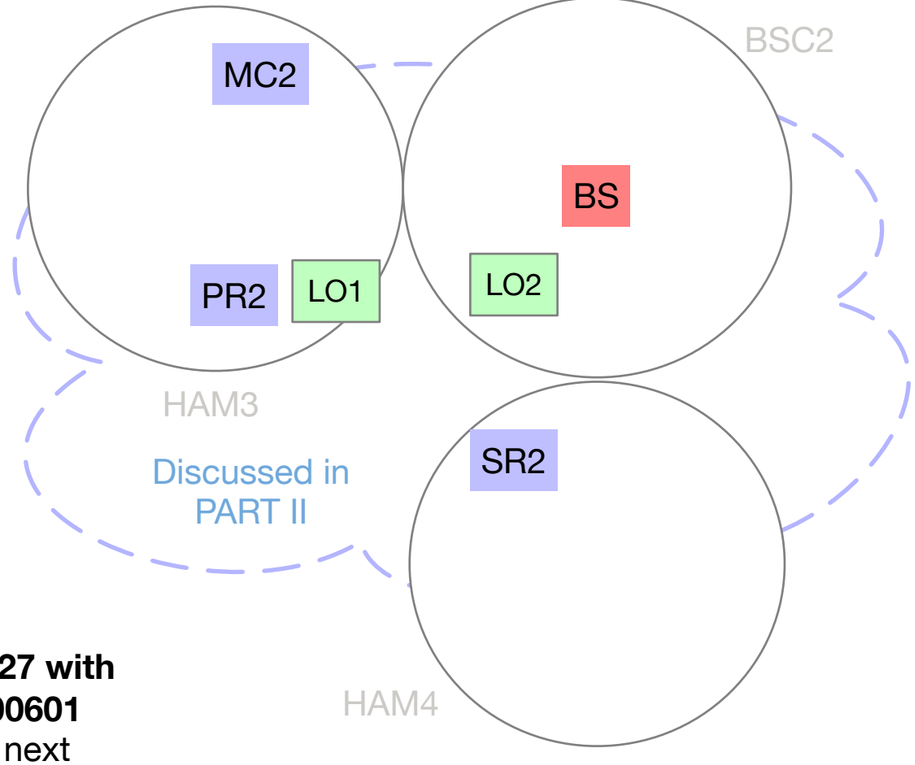


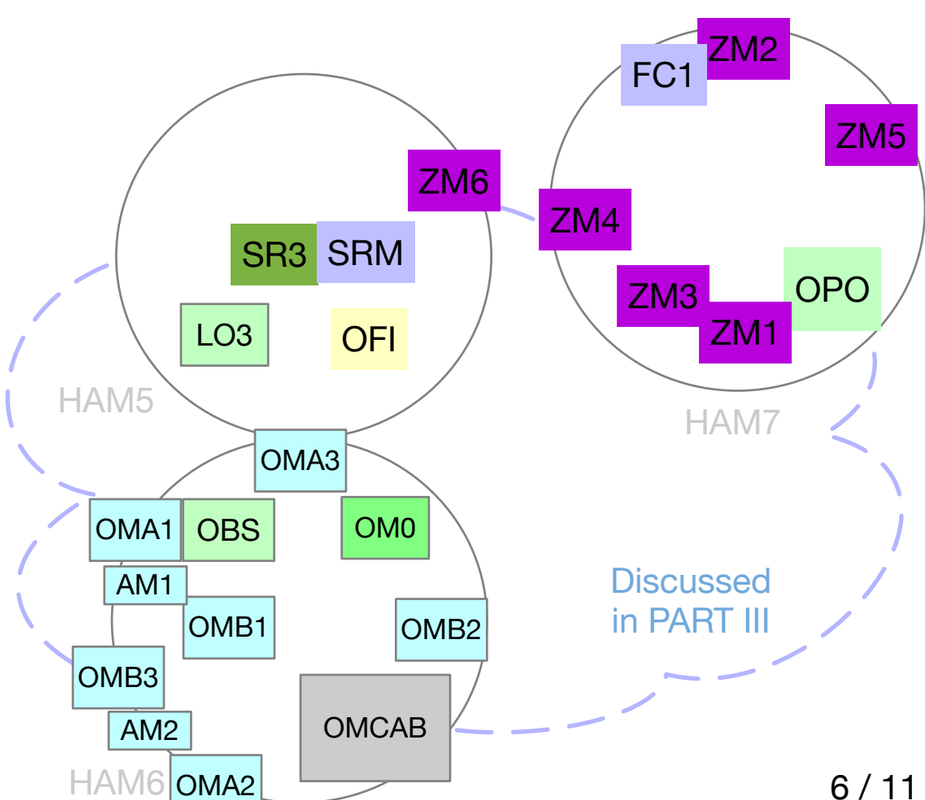
O4 SUS

Recap of D1800027-v27 with D2000405 and D2100601
(and the start of the next version of G1200071)

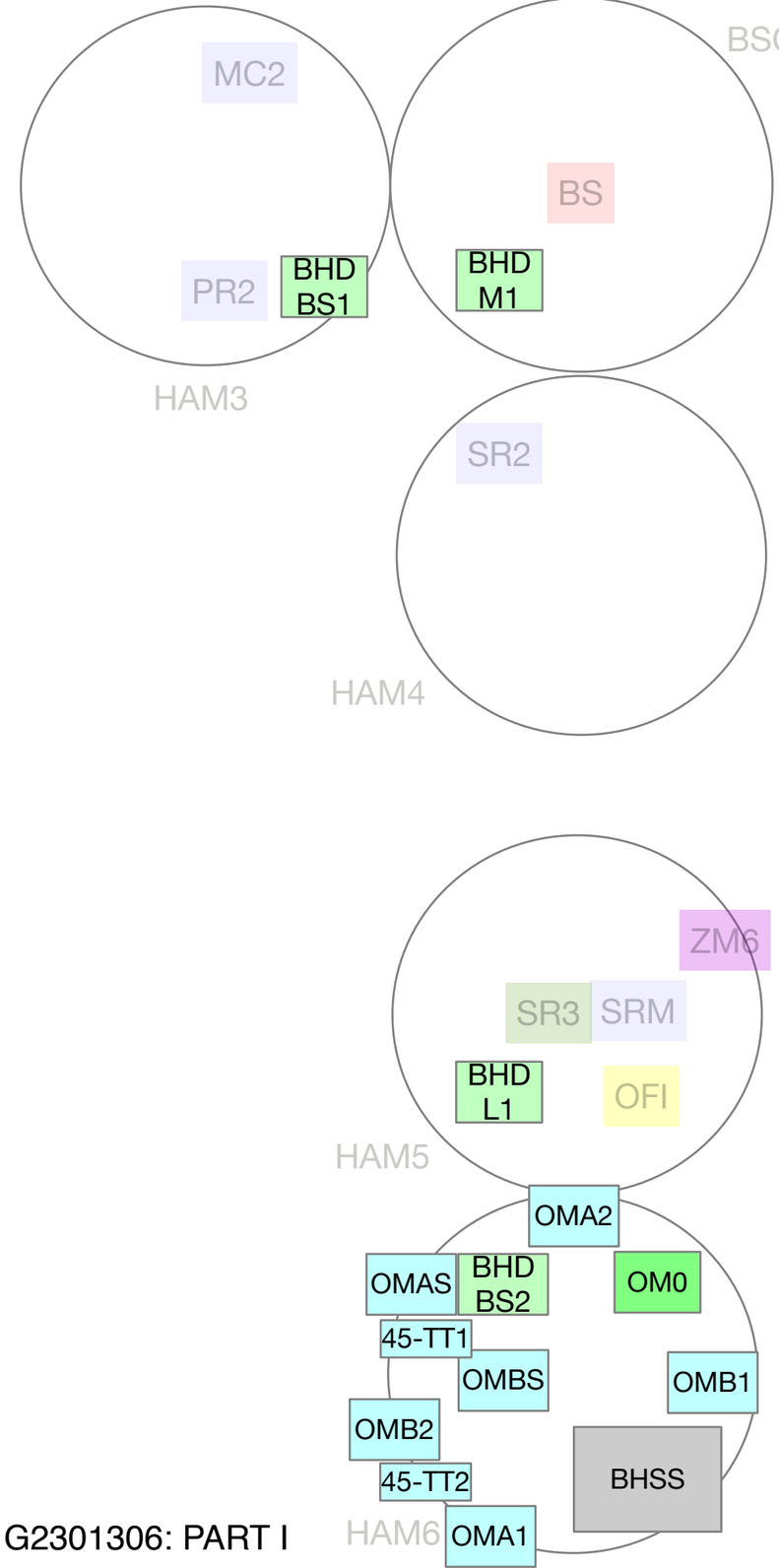


O5 SUS





O5 SUS

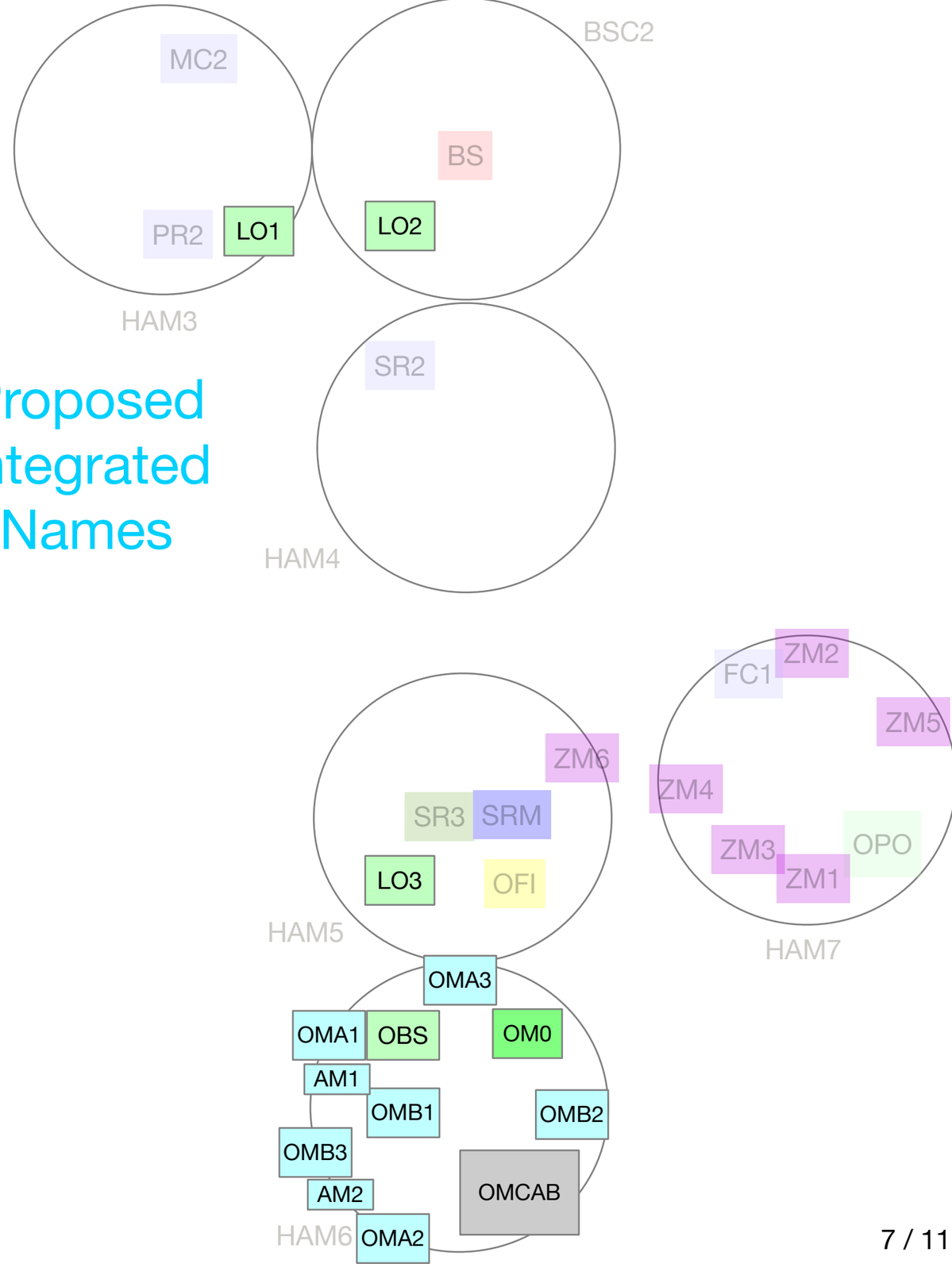


Design Doc Names

BHDBS1
BHDM1
BHDL1
BHDBS2
OM0
OMAS
OMA1
OMA2
OMBS
OMB1
OMB2
45-TT1
45-TT2
BHSS

Proposed Integrated Names

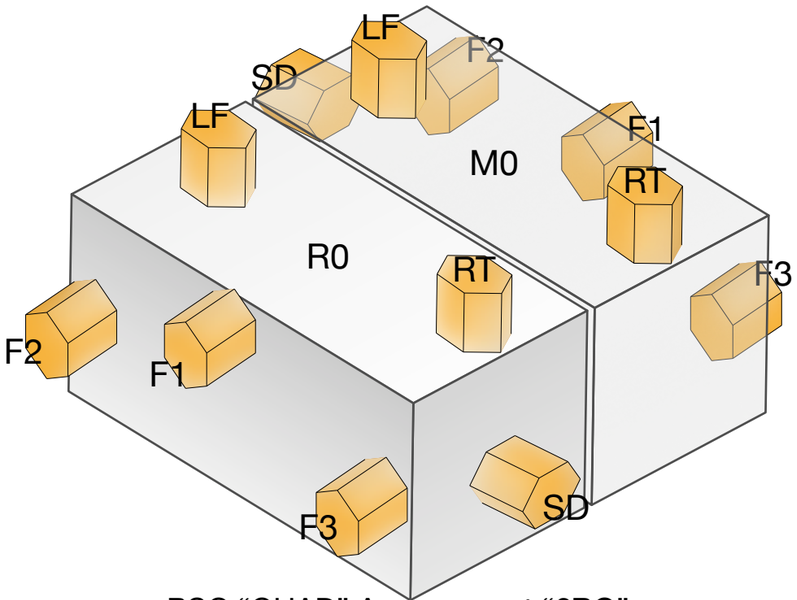
LO1
LO2
LO3
OBS
OM0
OMA1
OMA2
OMA3
OMB1
OMB2
OMB3
AM1
AM2
OMCAB



Controls Arrangement Recap

The diversity of 6-OSEM Arrangements, grouped into 4-OSEM signal chains in… so many ways. #facepalm

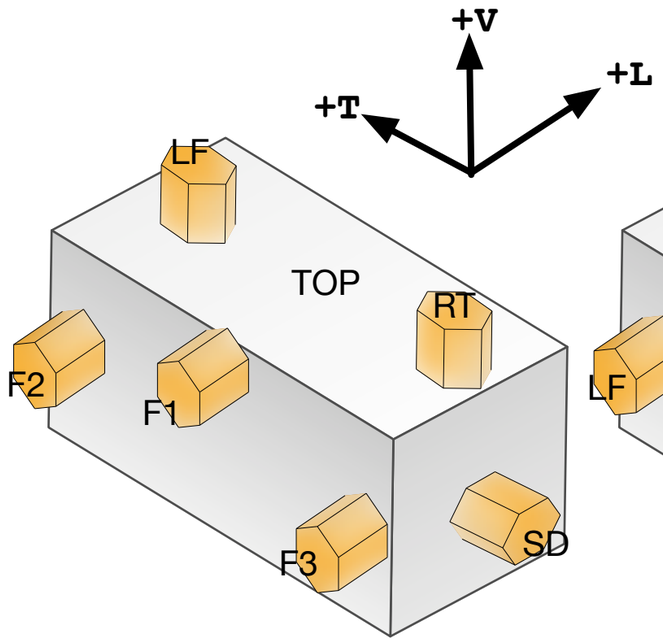
We all go insane if signals flow into digital system in any order *but* the canonical orders listed here.



BSC “QUAD” Arrangement “**6BQ**”

M0F1F2F3SD, M0LFRTR0LFRT, R0 F1F2F3SD

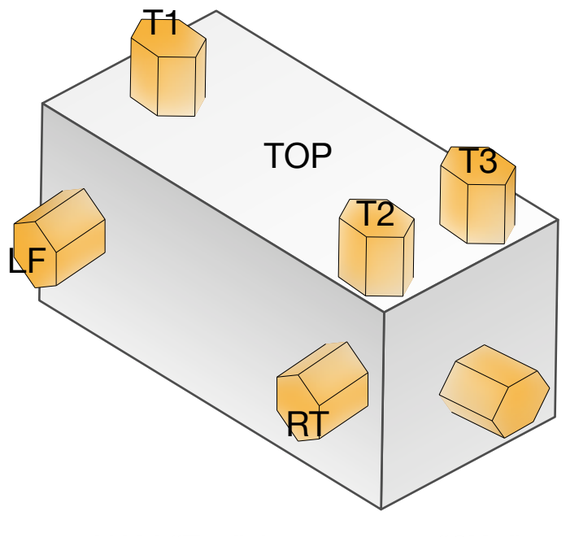
Quads



BSC “Face” Arrangement “6BF”

F1F2F3LF, RTSDxxxx

BSFM

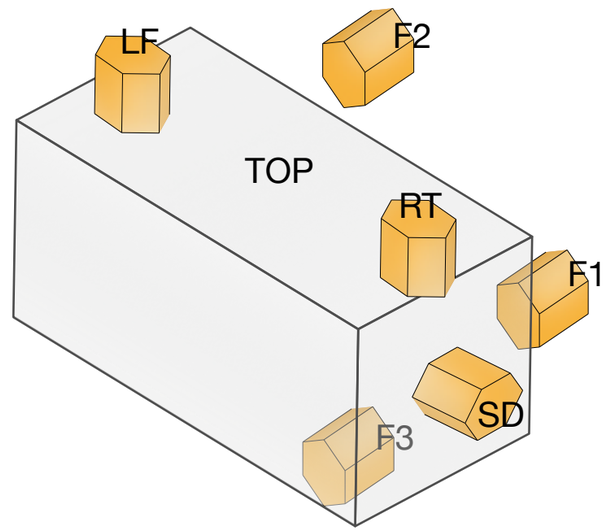


HAM “Top” Arrangement “**6HT**”

Solo: T1T2T3LF, RTSDxxx

Shared: T1T2T3LF, RTSDT1T2, T3LFRTSD

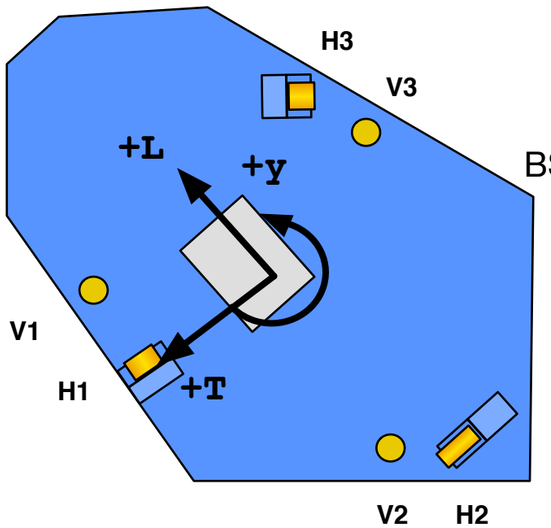
HLTS, HSTS, OMCS



HAM “Face” Arrangement “**6HF**”

F1F2F3SD, LFRTxxx

HRTS, HDTS



HAM “OPOS” Arrangement “**6HO**”

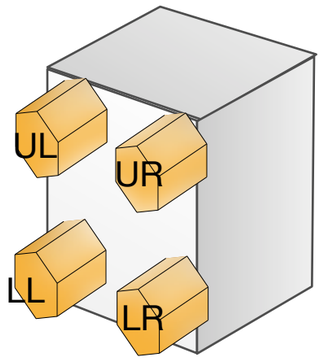
H1V1H2V2, H3V3xxxx

CHANGE BBSS FOR O5 to match QUADs and HRTS:

BSC “Face” Arrangement “**6BF**”

F1F2F3SD, LFRTxxxx

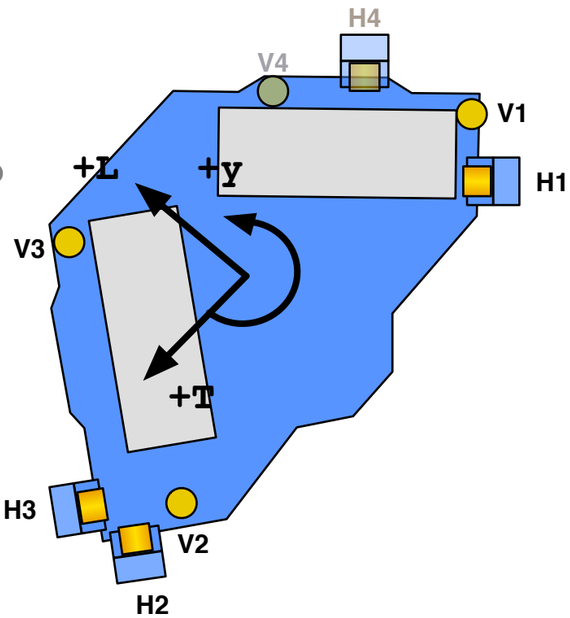
BBSS



4-OSEM stages are ALL UL LL UR LR

HoQIs are in “+” arrangement. Maybe UP, DN, LF, RT?

CHANGE if OMCS becomes OFDS FOR O5 to T1T2T3SD, LFRTxxxx



HAM “BHSS” Arrangement “**6HD**” (8HD)

H1V1H2V2, H3V3H4V4

New O5 Sensing / Actuation Controls Design Recap (H3, B2, H5)

Name	Chamber	Sus Type	Stage	Sensor/Actuator	Actuator Driver	N Sensor ADC Chans	N Driver DAC Chans	N CD Monitor Chans
BHDBS1 >> “**LO1**”	HAM3	HRTS	M1 “TOP”	6HF-BOSEM	HAM-A	6	6	6*1 (V)
			M2 “MID”	(none)	(n/a)	0	0	0
			M3 “BOT”	(none)	(n/a)	0	0	0
BS	BSC2	BBSS	M1	6BF-BOSEM	TTOP	6	6	6*4 (NSFV)
			M2	4-BOSEM 4-HoQI	TACQ (n/a)	4 4*3	6 (n/a)	4*4 (NSFV) (n/a)
			M3	4-AOSEM Oplev	TACQ (n/a)	4 4	4 0	4*4 (NSFV) 0
BHDM1 >> “**LO2**”	BSC2	HRTS	M1	6HF-BOSEM	HAM-A	6	6	6*1 (V)
			M2	(none)	(n/a)	0	0	0
			M3	(none)	(n/a)	0	0	0
BHDL1 >> “**LO3**”	HAM5	HRTS	M1	6HF-BOSEM	HAM-A	6	6	6*1 (V)
			M2	(none)	(n/a)	0	0	0
			M3	(none)	(n/a)	0	0	0
OFI	HAM5	OFDS	M1 “TOP”	6HT-BOSEM	OTOP	6	6	6*4 (NSFV)
			M2 “BOT”	(none)	(n/a)	0	0	0

New O5 Sensing / Actuation Controls Design Recap (H6)

Name	Chamber	Sus Type	Stage	Sensor/Actuator	Actuator Driver	N Sensor ADC Chans	N Driver DAC Chans	N CD Monitor Chans
OM0	HAM6	HATS	M1 “TOP”	6HF-BOSEM	HAM-A (-v1)	6	6	6*1 (V)
			M2 “MID”	(none)	(n/a)	0	0	0
			M3 “BOT”	4-AOSEM	HAM-A (-v2)	4	4	6*1 (V)
BHDBS2 >> “**OBS**”		HRTS	M1	6HF-BOSEM	HAM-A (-v1)	6	6	6*1 (V)
			M2	(none)	(n/a)	0	0	0
			M3	(none)	(n/a)	0	0	0
OMAS >> “**OMA1**”		HDDS	M1 “TOP”	4-BOSEM	HAM-A (-v2)	4	4	4*1 (V)
			M2 “BOT”	4-DCOIL	HAM-A (-v3)	0	4	4*1 (V)
OMA1 >> “**OMA2**”		H(P or T)DS	M1	4-BOSEM	HAM-A (-v2)	4	4	4*1 (V)
			M2	P or T SAMS	P or T Driver	0	1	2 (FS)
OMA2 >> “**OMA3**”		HCDS	M1	4-BOSEM	HAM-A (-v2)	4	4	4*1 (V)
			M2	4-DCOIL P or T SAMS	HAM-A (-v3) P or T Driver	0	4 1	4*1 (V) 2 (FS)
OMBS >> “**OMB1**”		HDDS	M1	4-BOSEM	HAM-A (-v2)	4	4	4*1 (V)
			M2	4-DCOIL	HAM-A (-v3)	0	4	4*1 (V)
OMB1 >> “**OMB2**”		H(P or T)DS	M1	4-BOSEM	HAM-A (-v2)	4	4	4*1 (V)
			M2	P or T SAMS	P or T Driver	0	1	2 (FS)
OMB2 >> “**OMB3**”		HCDS	M1	4-BOSEM	HAM-A (-v2)	4	4	4*1 (V)
			M2	4-DCOIL P or TSAMS	HAM-A (-v3) P or T Driver	0	4 1	4*1 (V) 2 (FS)
45-TT1 >> “**AM1**”		HTTS	M1	4-BOSEM	HAM-A (-v2)	4	4	4*1 (V)
45-TT2 >> “**AM2**”		HTTS	M1	4-BOSEM	HAM-A (-v2)	4	4	4*1 (V)
BHSS >> “**OMCAB**”		BHSS	M1	6HO-AOSEM 8-AOSEM	HAM-A (-v1) HAM-A	6 8	6 8	6*1 (V) 8*1 (V)

Notes on DC Power for a Rack

- Most standard SUS signal processing chassis require +/- 18 V, and draw current on the order of a few 100 milliamps in operation.

- IO Chassis require only +24 V, and a fully loaded IO chassis draws around 6 amps.

- Kepco's dual DC power supplies can supply either the +/- 18 V, +/- 24 V or two +24 V for IO chassis and are rated for 20 amps.

- Lessons learned best practices that have grown organically over the years:
:: Best to have 8 gauge wires for the cable run between Kepco DC power supplies and Rack Junction boxes (too much voltage drop on original 16 gauge wire design)
. H1 now almost entirely uses rack junction boxes***, L1 only recently (circa leading up to A+ O4) has started using them

:: OK to supply two IO chassis with a single Kepco power supply, but no more (even though 3 IO chassis ~ 18 amps < 20 amps, have seen issues)
. You'll often see single-IO chassis racks where +24 V goes from the junction box directly to the IO chassis rather than go "through" the +/-24 V power strip. OR you'll see a completely empty "standard" 24x +/- 24 V strip, and a "custom" 6x +24 V strip right next to it that distributes the single +24V from a single power supply to the two IO chassis in a two-IO-chassis rack.

- ***Rack junction boxes are custom built (no DCC drawing), so also organically grow and are different between sites.
:: They convert 3x 8 gauge wire incoming into 3x 16 gauge cables.
:: If the rack needs +/-18 V, +/-24 V, and +24 V, then three 3x 8 gauge cables are run from three separate power supplies
:: **This is a thing that could easily be standardized to be made generic between sites (think of LIGO India!).**

- Some racks, typically ISC racks, have chassis with "low-noise power regulators" that require a power sequencer, D1200757, in between the junction box and the power rails

- Some racks, including some SUS racks, need 200V high voltage for PZT drives. These racks need a High Voltage Distribution Box, D2000586
:: The distribute one 200V power supply (via 12-guage twisted pair cable) to a possible 5x PZT driver chassis (via similar 12-G twisted pair).

- IO Chassis are considered "noisy" digital systems and are powered separately from signal processing chassis that need +/-24 V.
- If there's only one IO chassis in the rack, then the +24 VDC gets it's

- The "standard" power strips, D1002189, have 24x distribution spigots and can be built to supply either +/- 24 VDC (Option 1) or +/- 18 VDC (Option 2)

- The "custom" power strips, D1100034, have 6x distribution spigots and can be built to supply either +/- 18 VDC (Option 1) or +/- 24 VDC (Option 2)
- (No typo there, which "option" is which voltage is obnoxiously opposite between the "standard" and "custom")