

# Simulink/Front Model & MEDM Screen Mods from ECR E1300578 (For SUS' in BSC Chambers)

J. Kissel for the SUS and ISC Team

**G1301192-v3**

# Added SVN \$Id\$ String to All Parts

```
Library: QUAD_MASTER
File Edit View Format Help

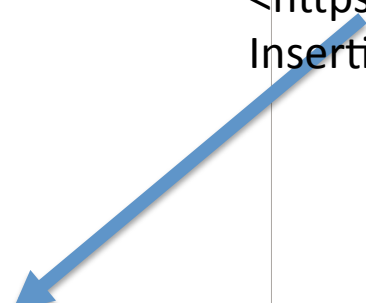
This is a standard
QUAD model

M0_COIL_F1_Out>
M0_COIL_F2_Out>
M0_COIL_F3_Out>
M0_COIL_LF_Out>
M0_COIL_RT_Out>
M0_COIL_SD_Out>
R0_COIL_F1_Out>
R0_COIL_F2_Out>
R0_COIL_F3_Out>
R0_COIL_LF_Out>
R0_COIL_RT_Out>
R0_COIL_SD_Out>
L1_COIL_UL_Out>
L1_COIL_LL_Out>
L1_COIL_LR_Out>
L2_COIL_UL_Out>
L2_COIL_LL_Out>
L2_COIL_LR_Out>
L3_ESD_DC_Out>
L3_ESD_UL_Out>
L3_ESD_LL_Out>
L3_ESD_LR_Out>
MOR0_WDSTAT_Out>
BIO_M0_CTRL_Out>
BIO_R0_CTRL_Out>
BIO_L1_CTRL_Out>
BIO_L2_CTRL_Out>
TEST1_Out>
TEST2_Out>
ODDCHAN>

QUAD
Quadruple Suspension

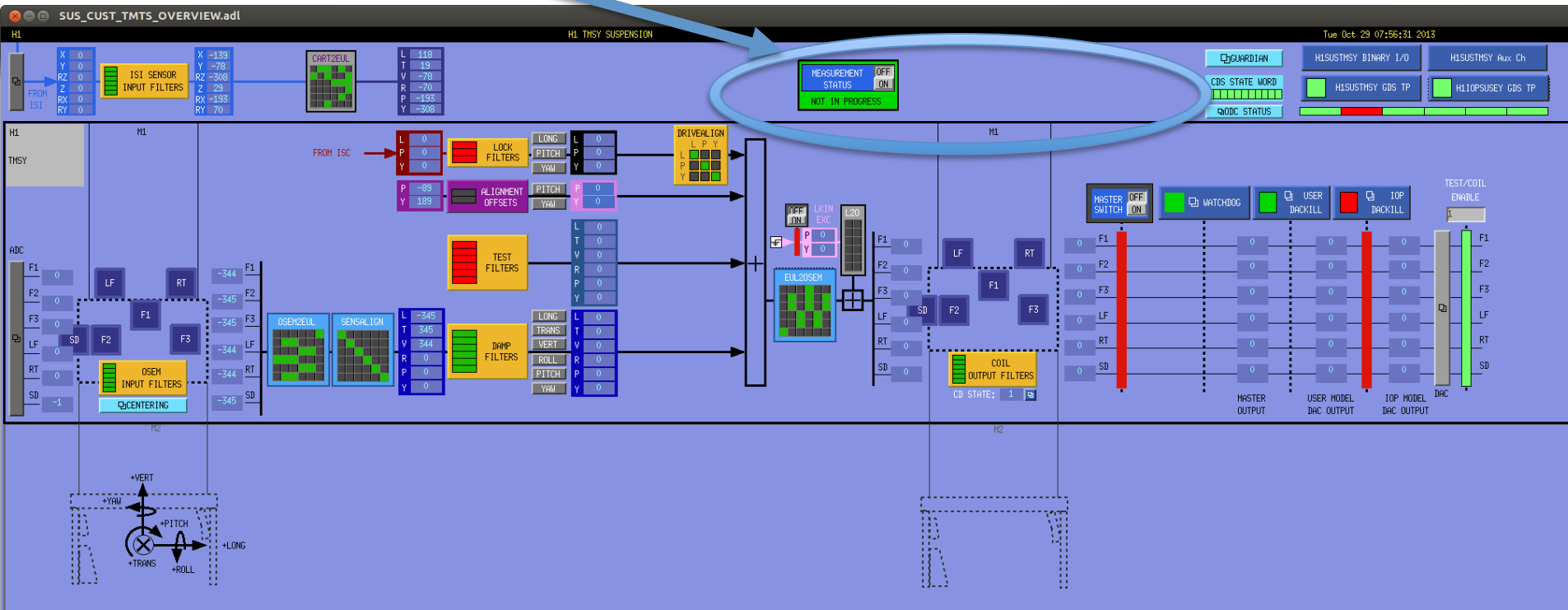
SVN $Id$: QUAD_MASTER.mdl 6115 2013-10-29 14:51:16Z jeffrey.kissel@LIGO.ORG $
```

- Added to all top level models and library parts
- Great for visual assessment of version control
- Must be added to each top-level model (but comes for free with library parts)
- See instructions / description here:  
<<https://awiki.ligo-wa.caltech.edu/aLIGO/InsertingSvnVersionStringIntoSimulinkModels>>

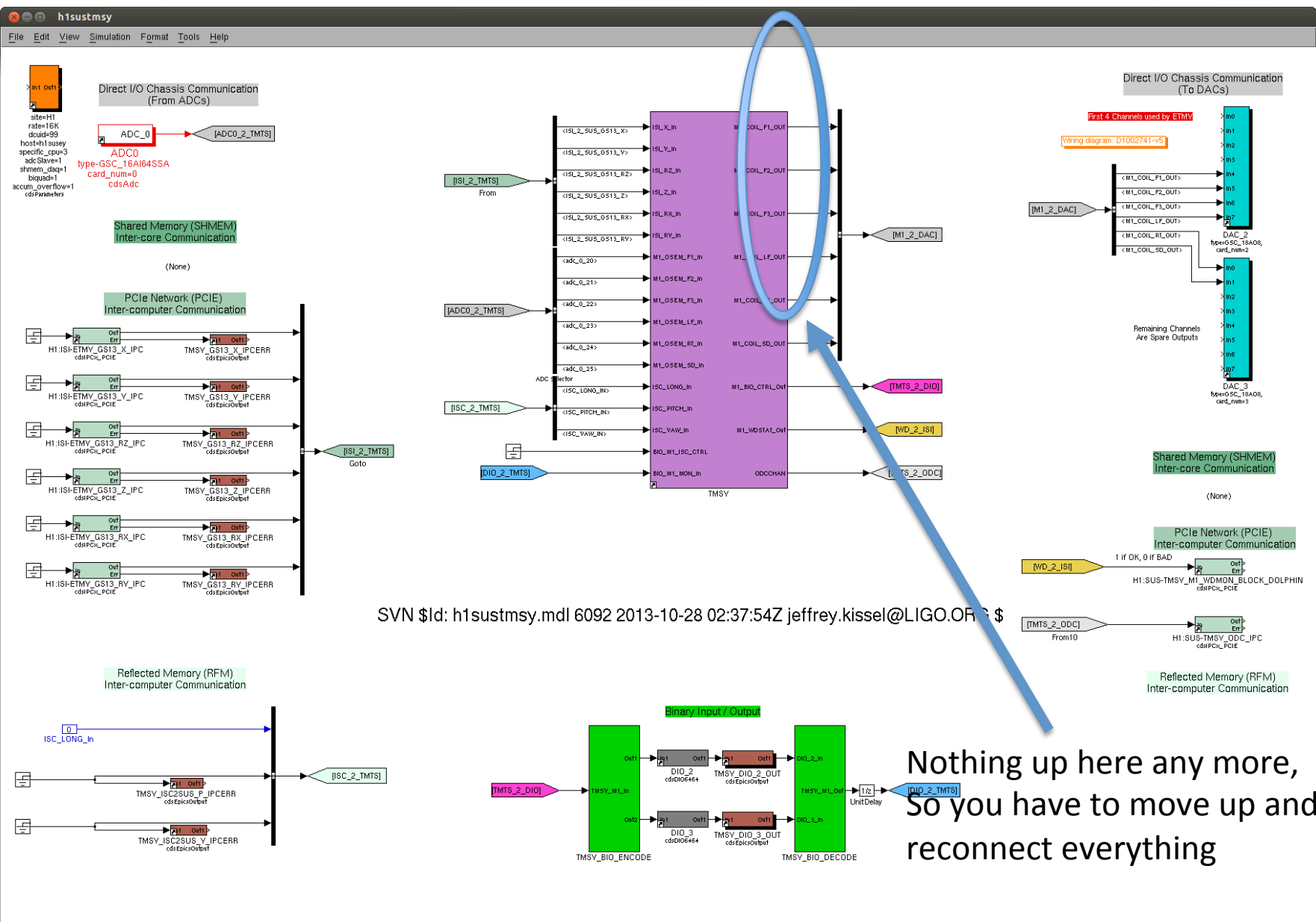


# Removal of ISI OFFLOAD

- A part of reducing wasted computation cycles
- Experience has shown that ISC offloading is only needed up to TOP mass of each suspension
- **Affects top-level of models**, so every model must be reconnected and IPCs senders removed
- **SEI needs to get rid of their IPC receivers**
- No longer anything here (for every suspension type)

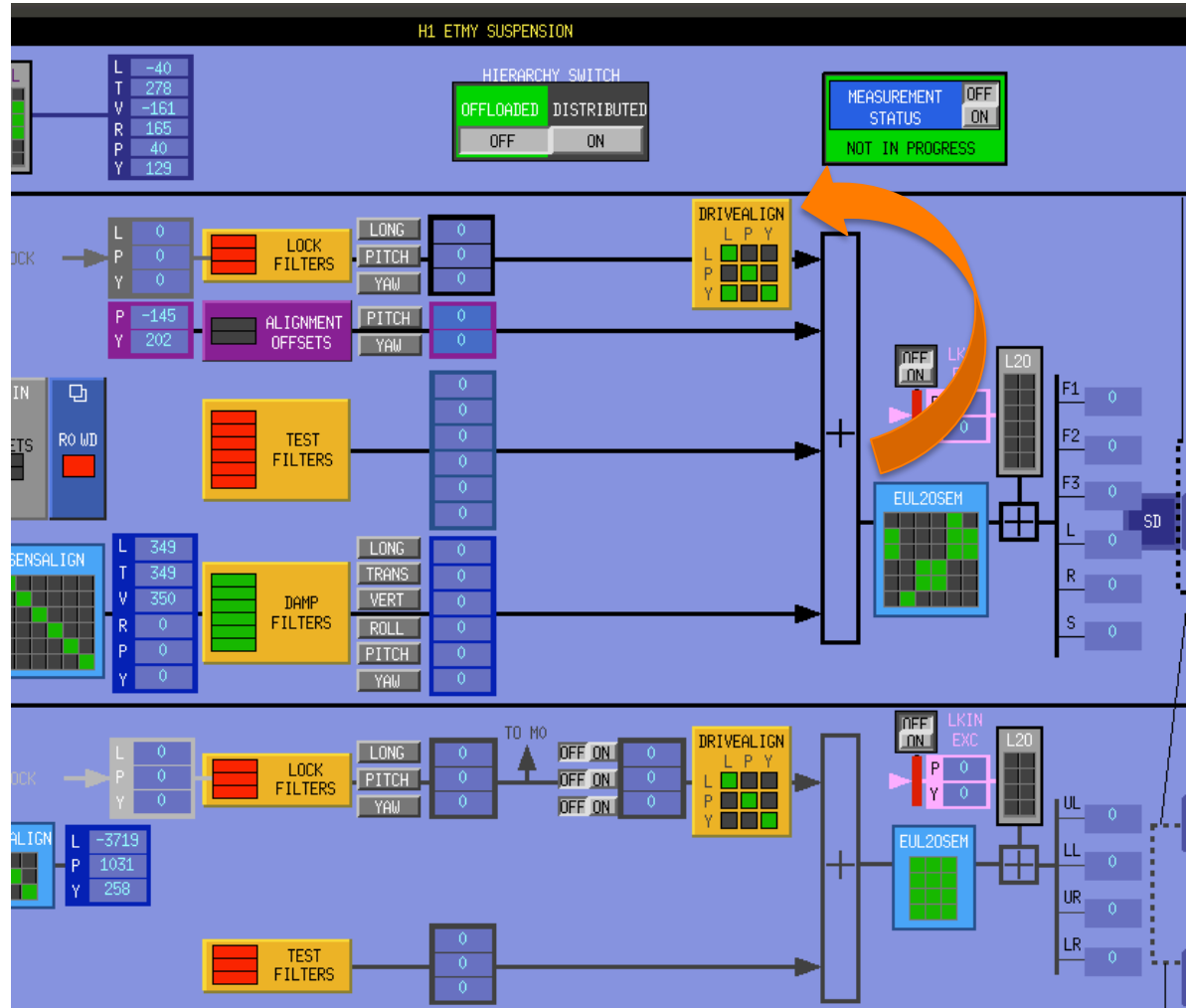


# Removal of ISI OFFLOAD



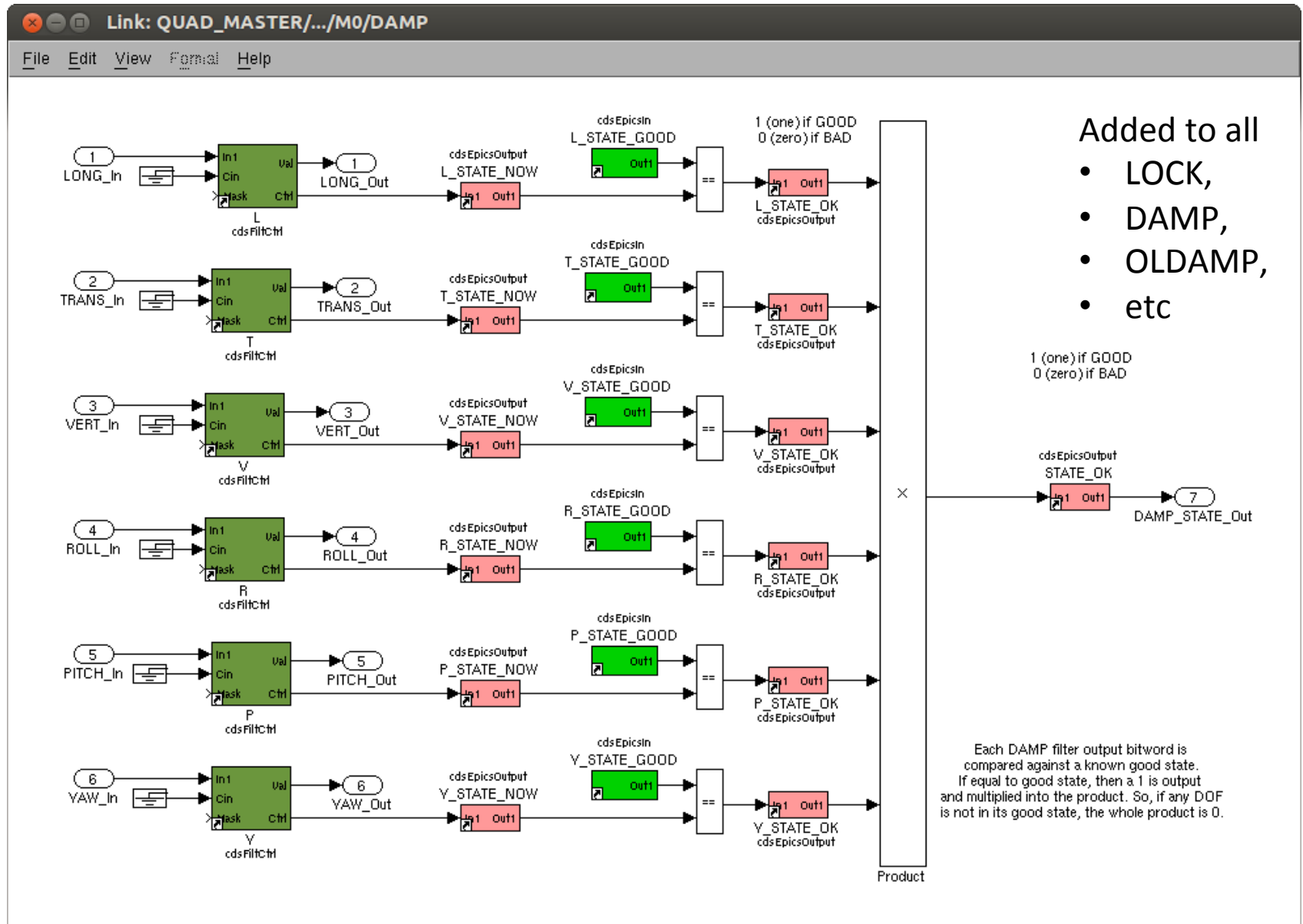
# DRIVEALIGN Mods

- Move drive align to only affect ISC / "LOCK" Filters
- DRIVEALIGN designed to decouple L, P, and Y force and torque at each stage from L of the optic (the main chain on the QUAD), so it doesn't make sense to include these filters in, say the damping path
- The means
  - Move it up to only affect LOCK path at every stage
  - Reduce the size of M0 M1 matrix from 6x6 to 3x3
  - Totally removed from R0
- Only involves library parts => Comes for free with update

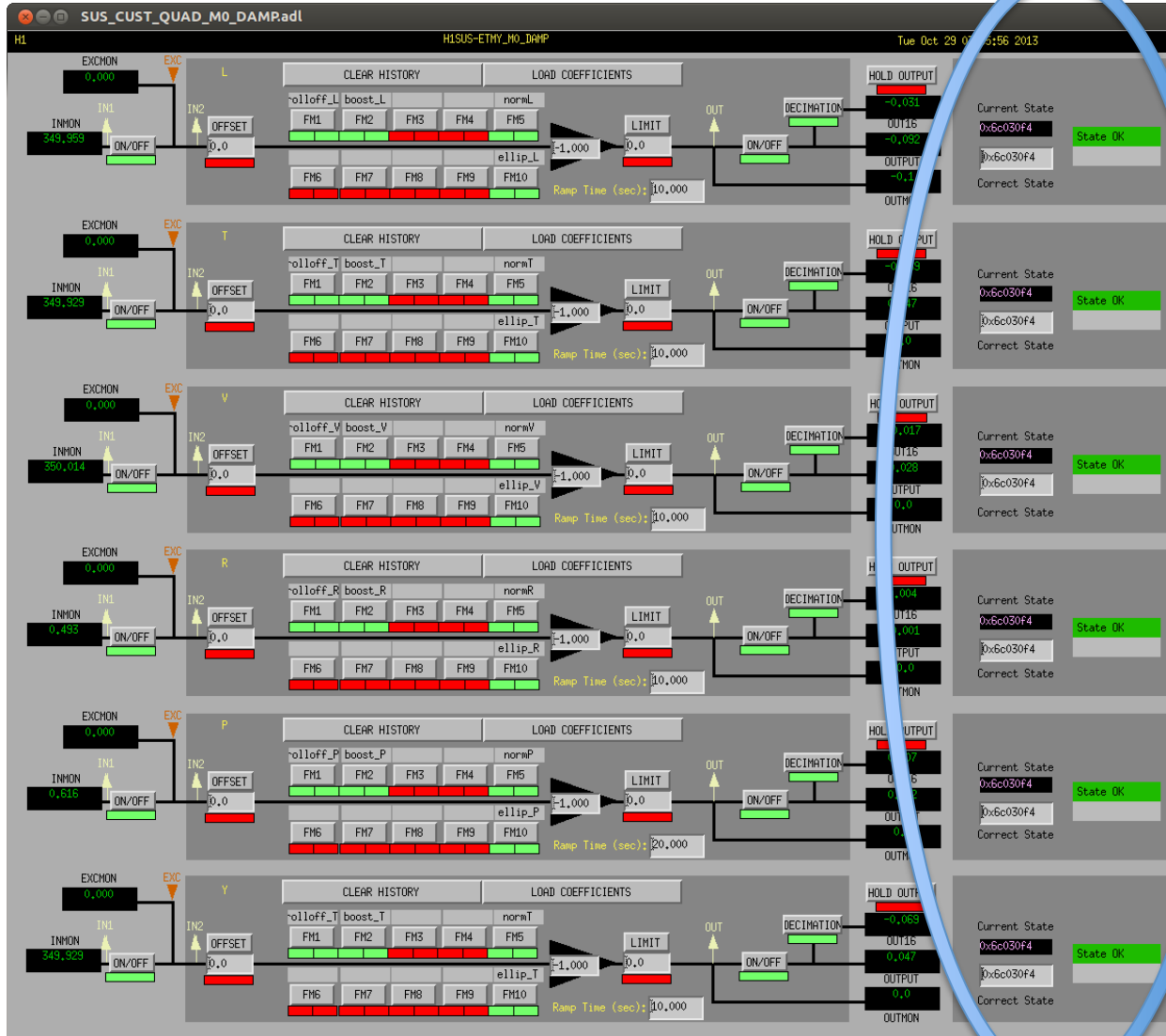


(Actually ECR E1300740)

# Added ODC Bits



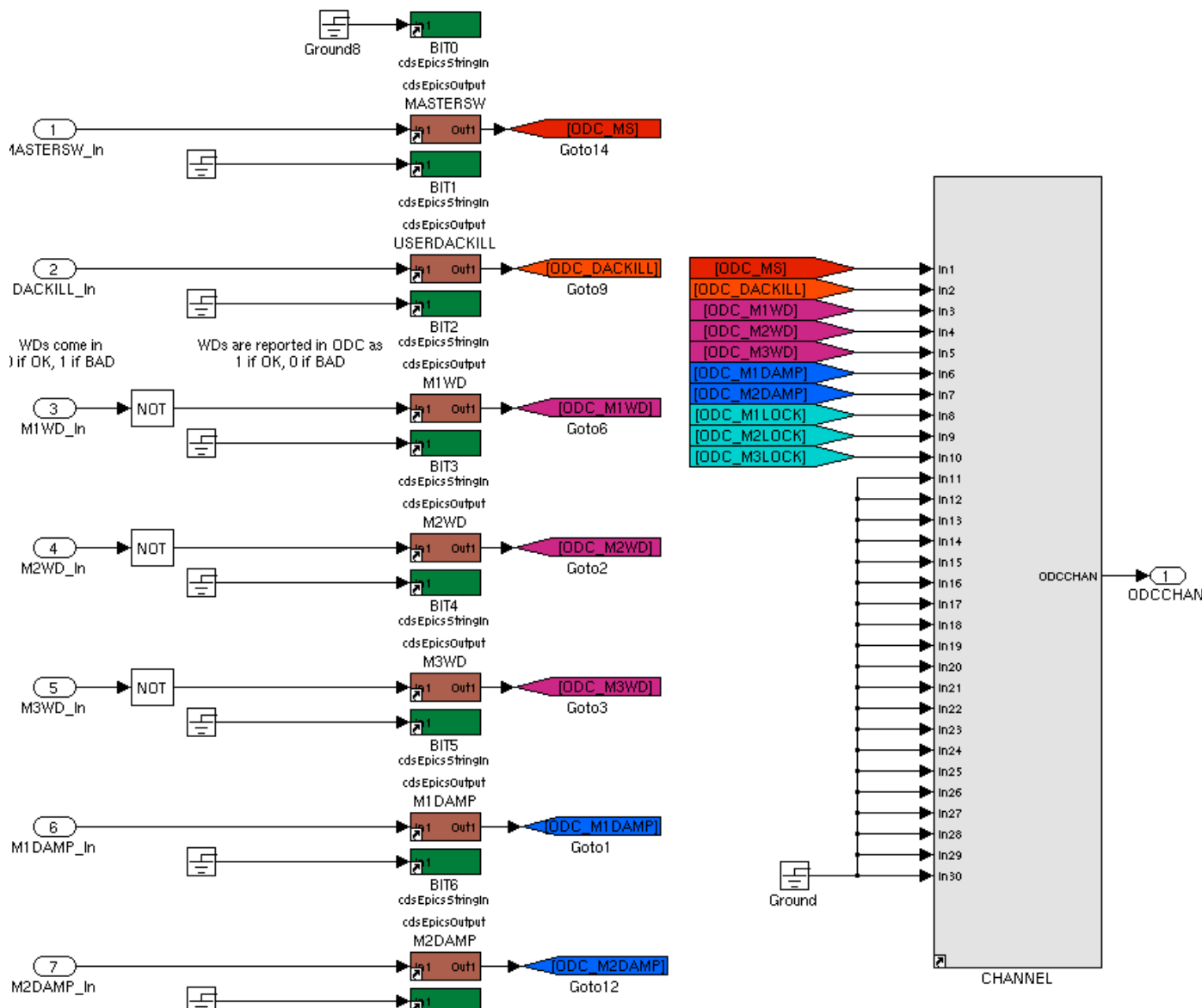
# Added ODC Bits



- State logic is now on every one of the DAMP, LOCK, OLDAMP filter screens
- Only includes filter modules in the state, no gains 😞
- Thought about doing this for OSEMINFs, but they need unique gain number for every OSEM, so not compatible with library parts

(Actually ECR E1300740)

# Added ODC Bits



All bits get piped into new ODC V2 Block which is much cleaner

QUADs have 13 bits, BSFMs have 10 bits, TMTs have 5 bits, Etc. depending on how many stages of LOCKing and DAMPing

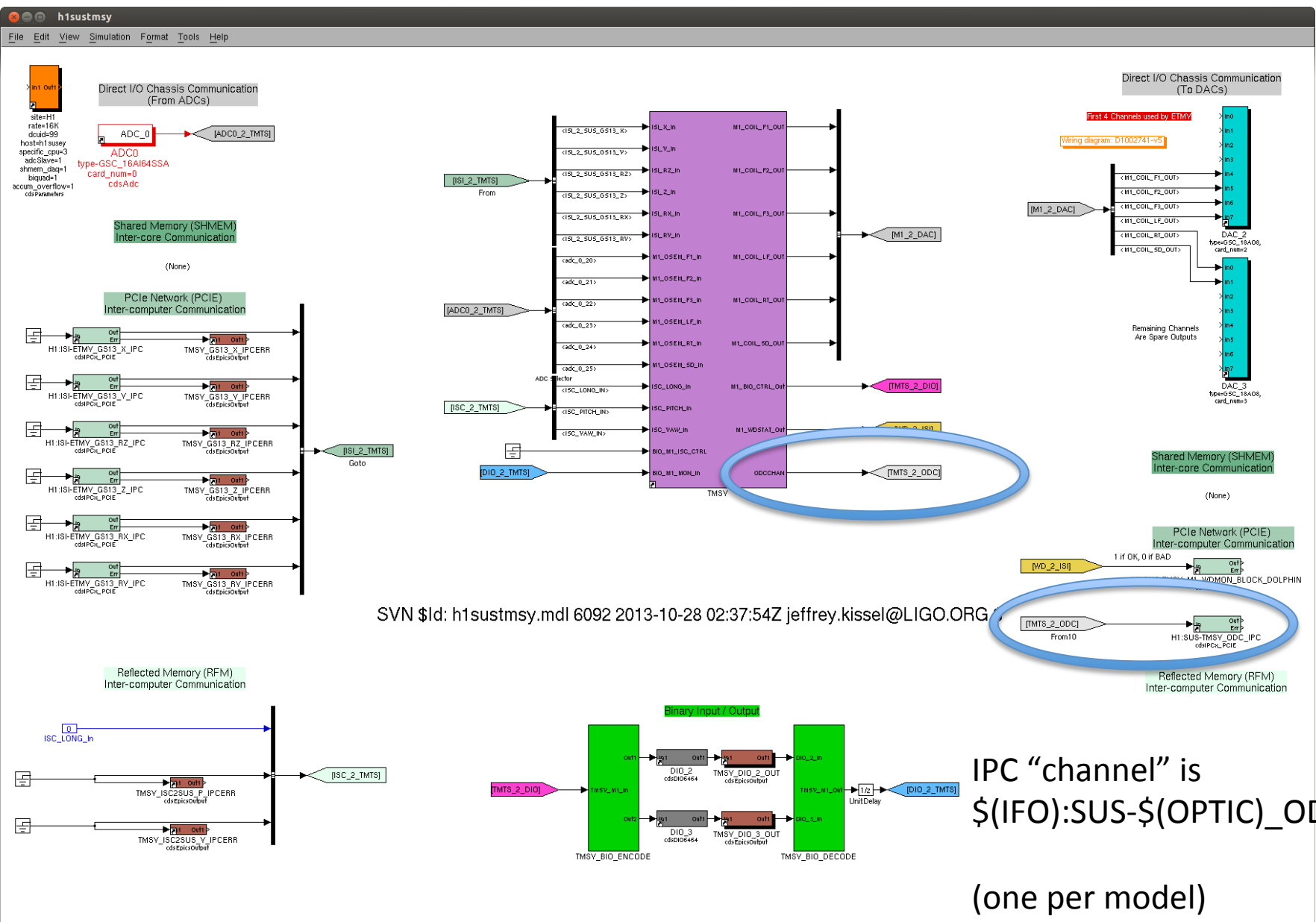
Channel is now spit out to the top level to be collected by ODC master



(Actually ECR E1300740)

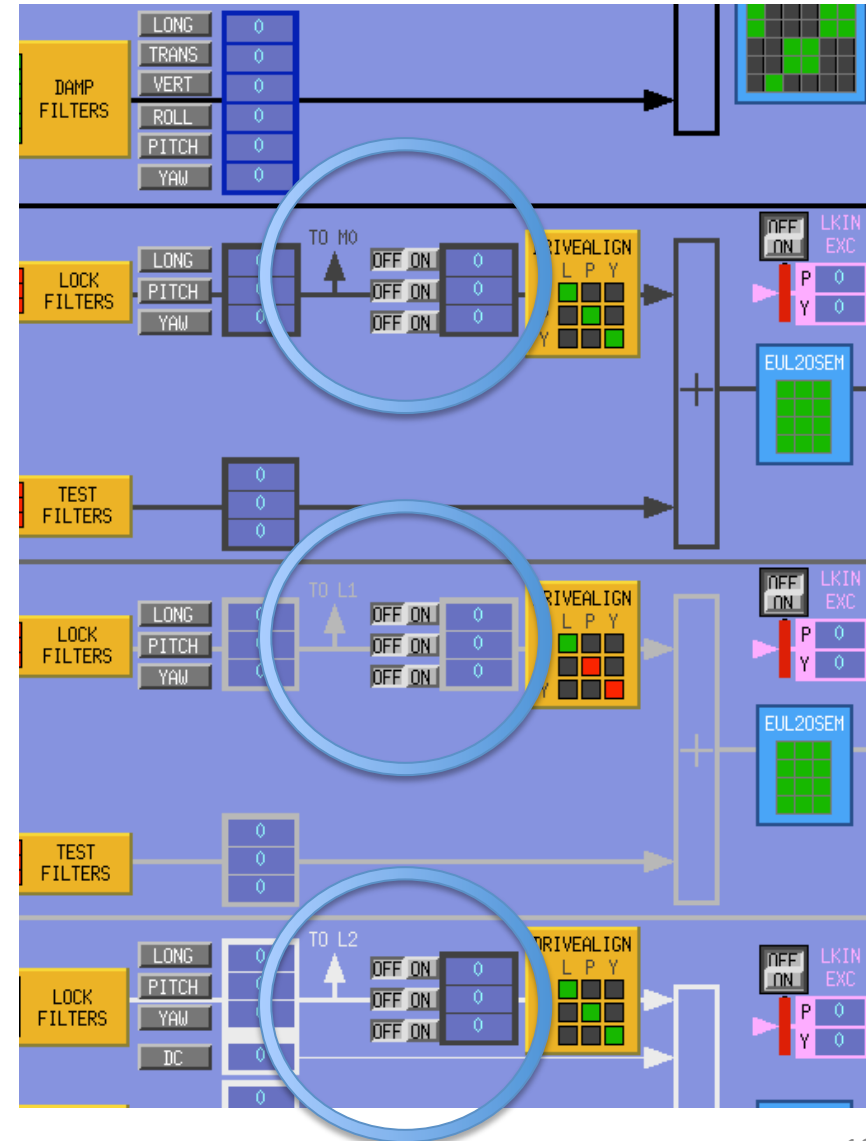
# Added ODC Bits

Affects top models!

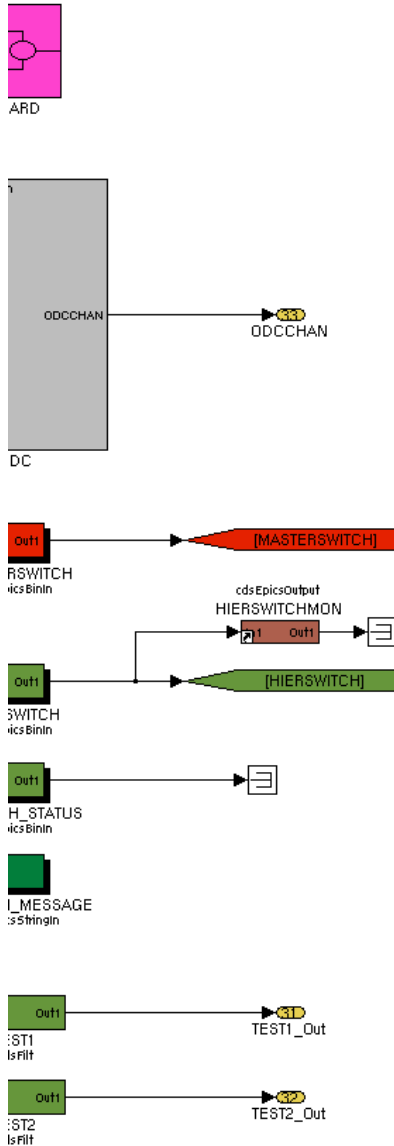


# Added switch after ISC (internal) OFFLOAD

- Added independent on/off switch between offload to upper stages and the DRIVEALIGN matrix
- This is so when we use “offloaded” (as opposed to “distributed”) hierarchy, we can pipe the ASC signals up to only the TOP mass, as opposed to LSC which needs to go to every stage



# Divided up Commissioning vs. Science Frames



```
#DAQ Channels
ODC_CHANNEL_OUT* uint32

M0_ISIINF_X_OUT* 1024
M0_ISIINF_Y_OUT* 1024
M0_ISIINF_RZ_OUT* 1024
M0_ISIINF_Z_OUT* 1024
M0_ISIINF_RX_OUT* 1024
M0_ISIINF_RY_OUT* 1024

M0_ISIWIT_L* 1024
M0_ISIWIT_T* 1024
M0_ISIWIT_V* 1024
M0_ISIWIT_R* 1024
M0_ISIWIT_P* 1024
M0_ISIWIT_Y* 1024

M0_TEST_L_OUT 256
M0_TEST_T_OUT 256
M0_TEST_V_OUT 256
M0_TEST_R_OUT 256
M0_TEST_P_OUT 256
M0_TEST_Y_OUT 256

M0_COILOUTF_F1_EXC 256
M0_COILOUTF_F2_EXC 256
M0_COILOUTF_F3_EXC 256
M0_COILOUTF_LF_EXC 256
M0_COILOUTF_RT_EXC 256
M0_COILOUTF_SD_EXC 256

M0_OSEMINF_F1_IN1 256
M0_OSEMINF_F2_IN1 256
M0_OSEMINF_F3_IN1 256
M0_OSEMINF_LF_IN1 256
M0_OSEMINF_RT_IN1 256
M0_OSEMINF_SD_IN1 256

M0_OSEMINF_F1_OUT 256
M0_OSEMINF_F2_OUT 256
M0_OSEMINF_F3_OUT 256
M0_OSEMINF_LF_OUT 256
M0_OSEMINF_RT_OUT 256
M0_OSEMINF_SD_OUT 256

M0_DAMP_L_IN1* 256
M0_DAMP_T_IN1* 256
M0_DAMP_V_IN1* 256
M0_DAMP_R_IN1* 256
M0_DAMP_P_IN1* 256
M0_DAMP_Y_IN1* 256

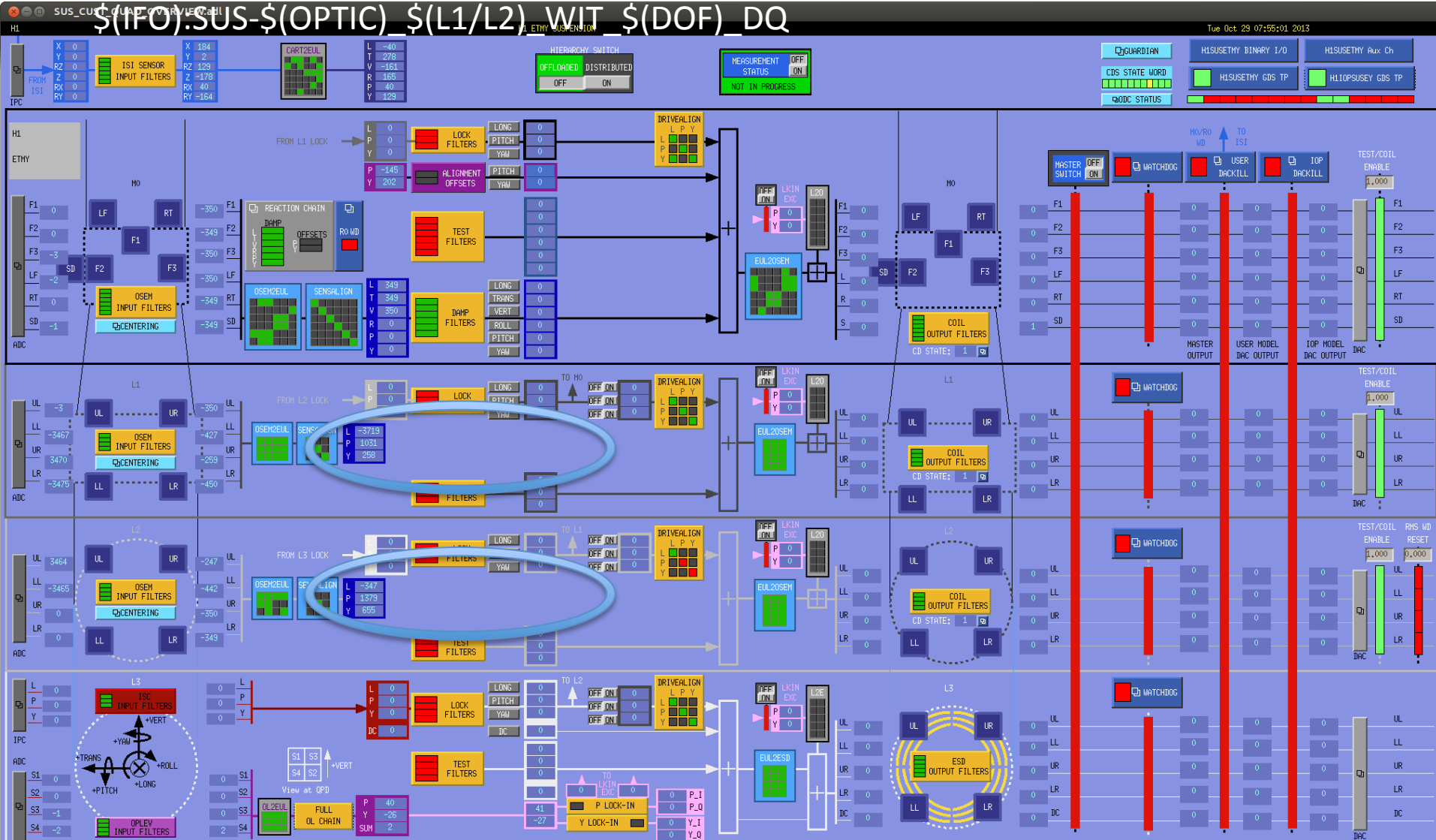
M0_DAMP_L_IN2 256
M0_DAMP_T_IN2 256
M0_DAMP_V_IN2 256
M0_DAMP_R_IN2 256
M0_DAMP_P_IN2 256
M0_DAMP_Y_IN2 256
```

Chose to store forever:

- One SUS/BSC-ISI's worth of Calibrated Cartesian Basis in [nm / nrad] ( $\$(IFO):SUS-\$(OPTIC)-\$(M0/M1)_ISIINF-\$(DOF)_OUT\_DQ$ ) i.e. the QUADs and the BSFMs are in charge of storing this
- Every SUS' Calibrated suspension point motion [nm / nrad]
- Only one version of OSEM / Oplev / ISC sensor signal at each stage – Euler basis, Calibrated into [ $\mu\text{m}$  /  $\mu\text{rad}$ ]
- Only one version of control signal at each stage – OSEM basis, (uncalibrated) DAC counts

# Removed QUAD lower stage damping

- No longer needed now that ISIs are commissioned
- Means \$(IFO):SUS-\$(OPTIC)\_\$(L1/L2)\_DAMP\_\$(DOF)\_IN1\_DQ becomes  
\$(IFO):SUS-\$(OPTIC)\_\$(L1/L2)\_WIT\_\$(DOF)\_DQ

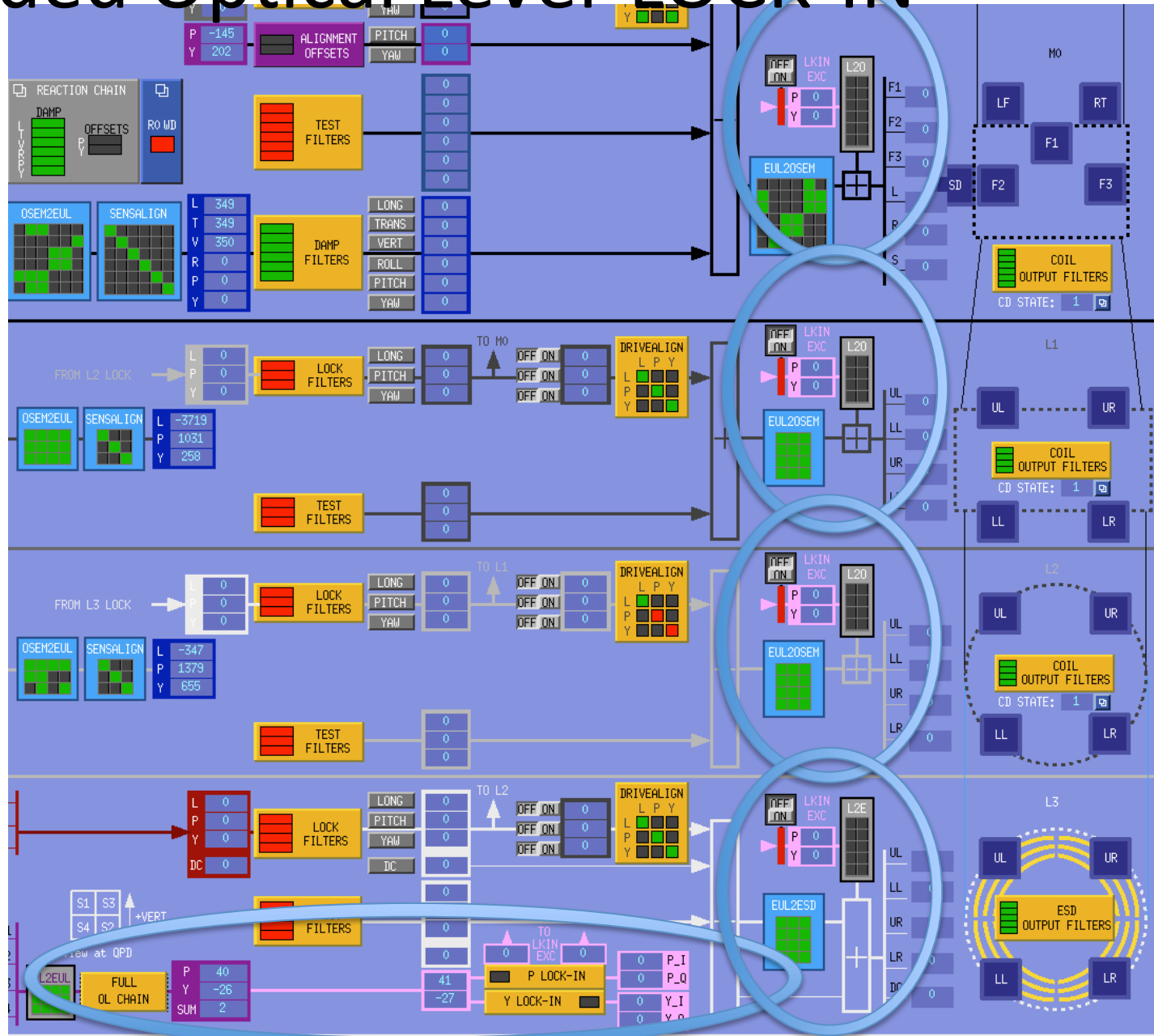


# Added Optical Lever LOCK-IN

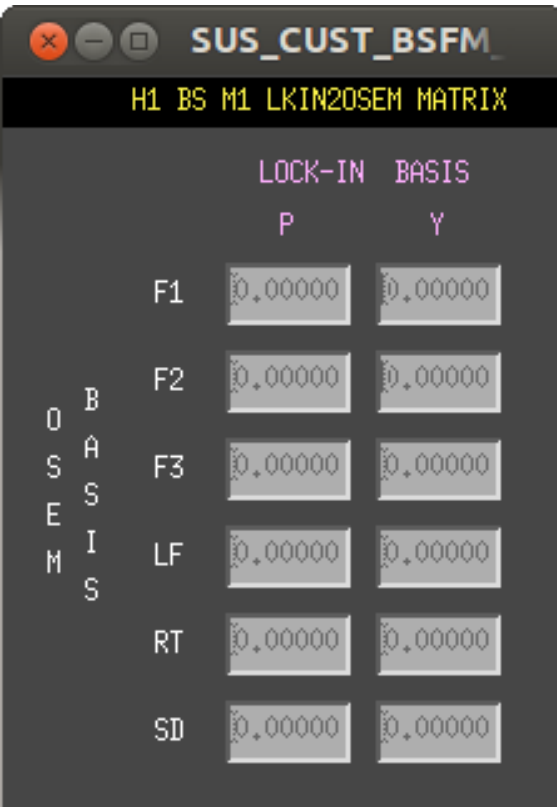
- 1) drive suspensions longitudinally and minimize the coupling to angle. Should we minimize coupling of M1\_L to M1\_A or M1\_L to M3\_A? The latter seems to make sense, but I haven't modeled what the effect will be for both cases.
- 2) balance the coil gains of all stages. here we want to use the logic of the old f2pRatio script written by Vuk/Matt which makes three measurements to find 3 of 4 coil gains (the remaining one is set to 1). The old way to do this was to use the OL for the readout. Naturally, we cannot do this for the M1/M2 stages anymore. And we can't use the OSEM readbacks at high frequency because of the pickup between the drive coil and the osem sensor.
- 3) Do a FD balance of P2Y and Y2P using something as the reference sensor. But what's the sensor?
- 4) Also, how do we do the A2L balancing for low frequencies (below the GW band)? For the GW band, we want to do this in the regular scalar way by just driving angle of each stage and minimizing the IFO readout. What's the harm in just punting on the  $f < 10$  Hz FD part?
- 5) In cases where we don't have OL on the mirror we can use the WFS DC. In case #4, we want to use the LSC signal. Both require some communication between SUS/ISC. I don't want to add a bunch of IPC to handle this. Perhaps for the cases where we use WFS\_DC to balance SUS we can utilize the ASC lockins. Not sure how to do #4.

# Added Optical Level LOCK-IN

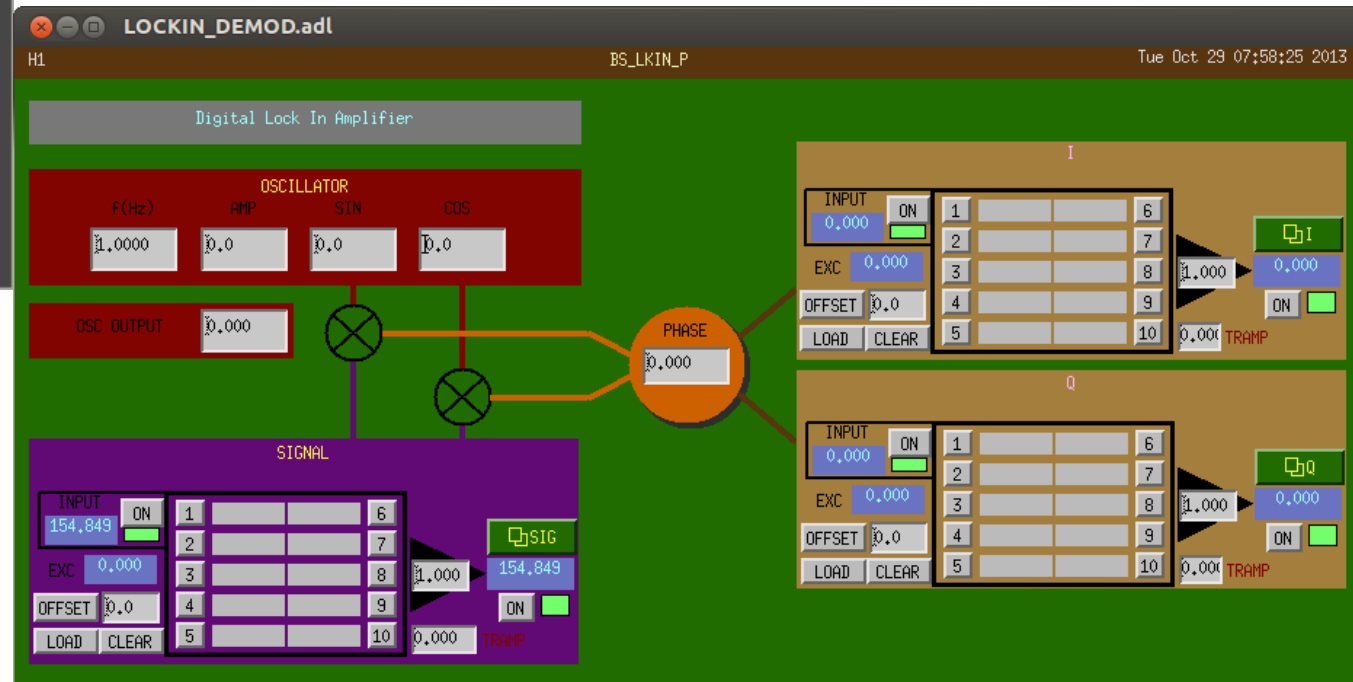
- Sent directly to coil basis, so we can do any configuration we want
- Sent to every stage
- One for PITCH, and one for YAW



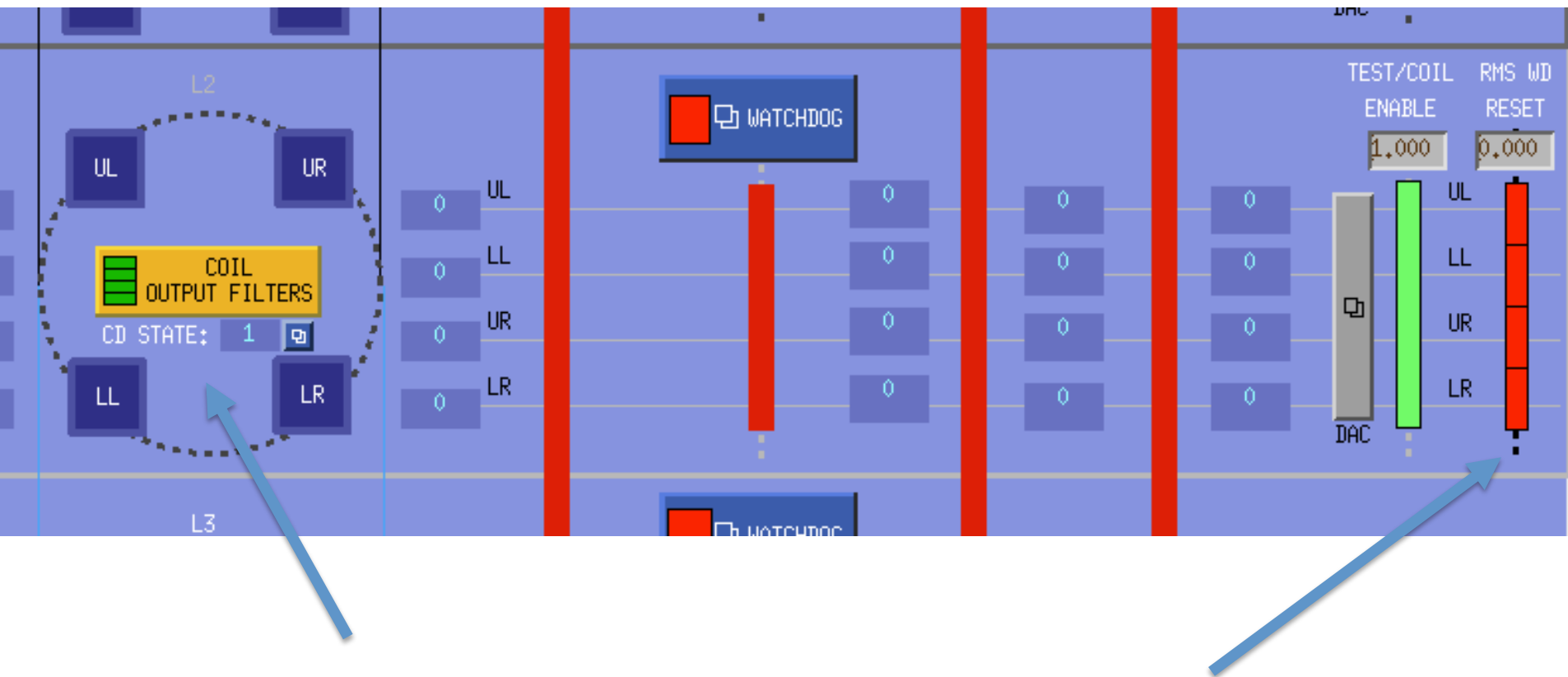
# Added Optical Lever LOCK-IN



- Sent directly to coil basis, so we can do any configuration we want
- Uses ISC library part
- **Needs new \$(SUBSYSTEM) and \$(INSTANCE) variables in macro files**



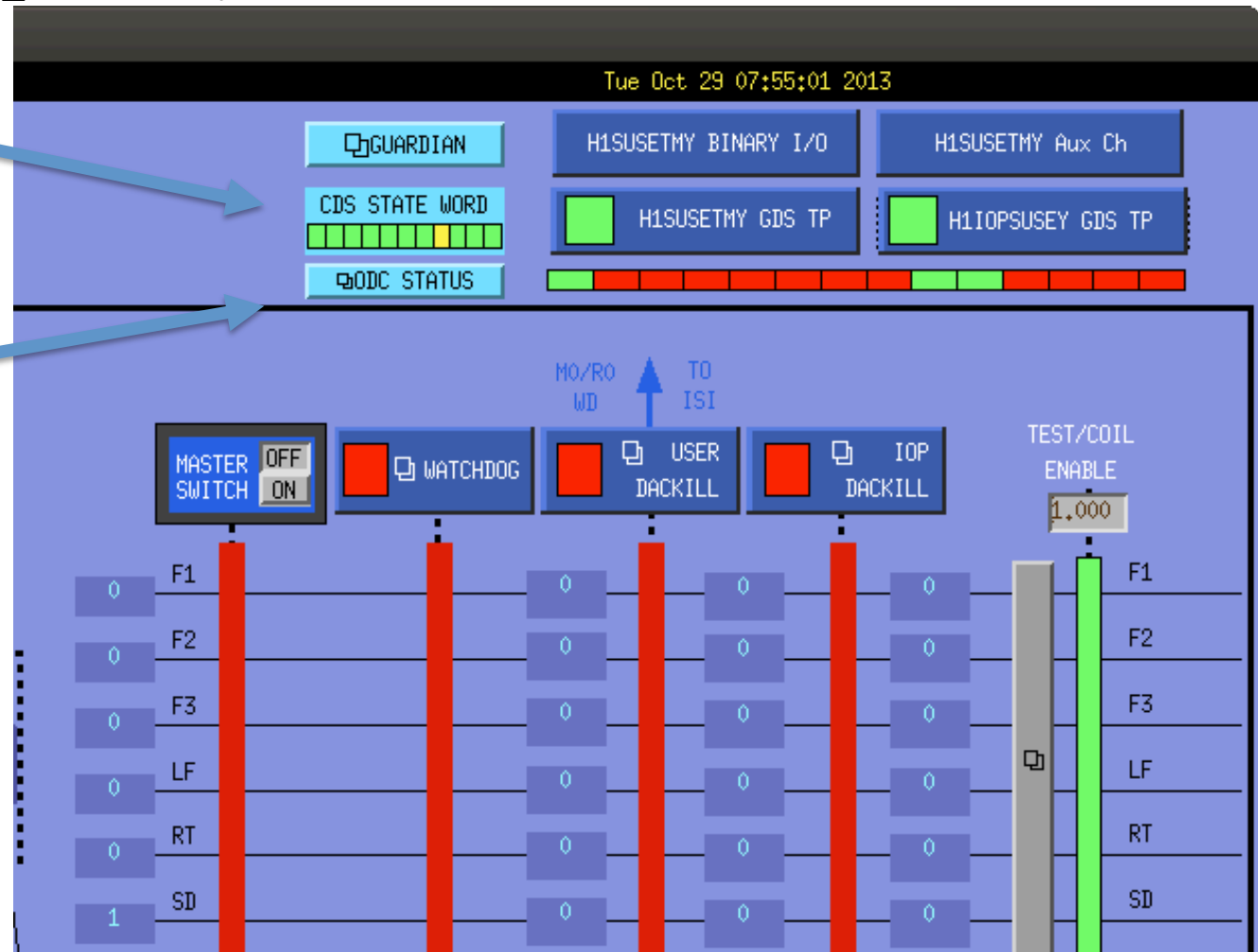
# Added CD State and PUM WD to OVERVIEW





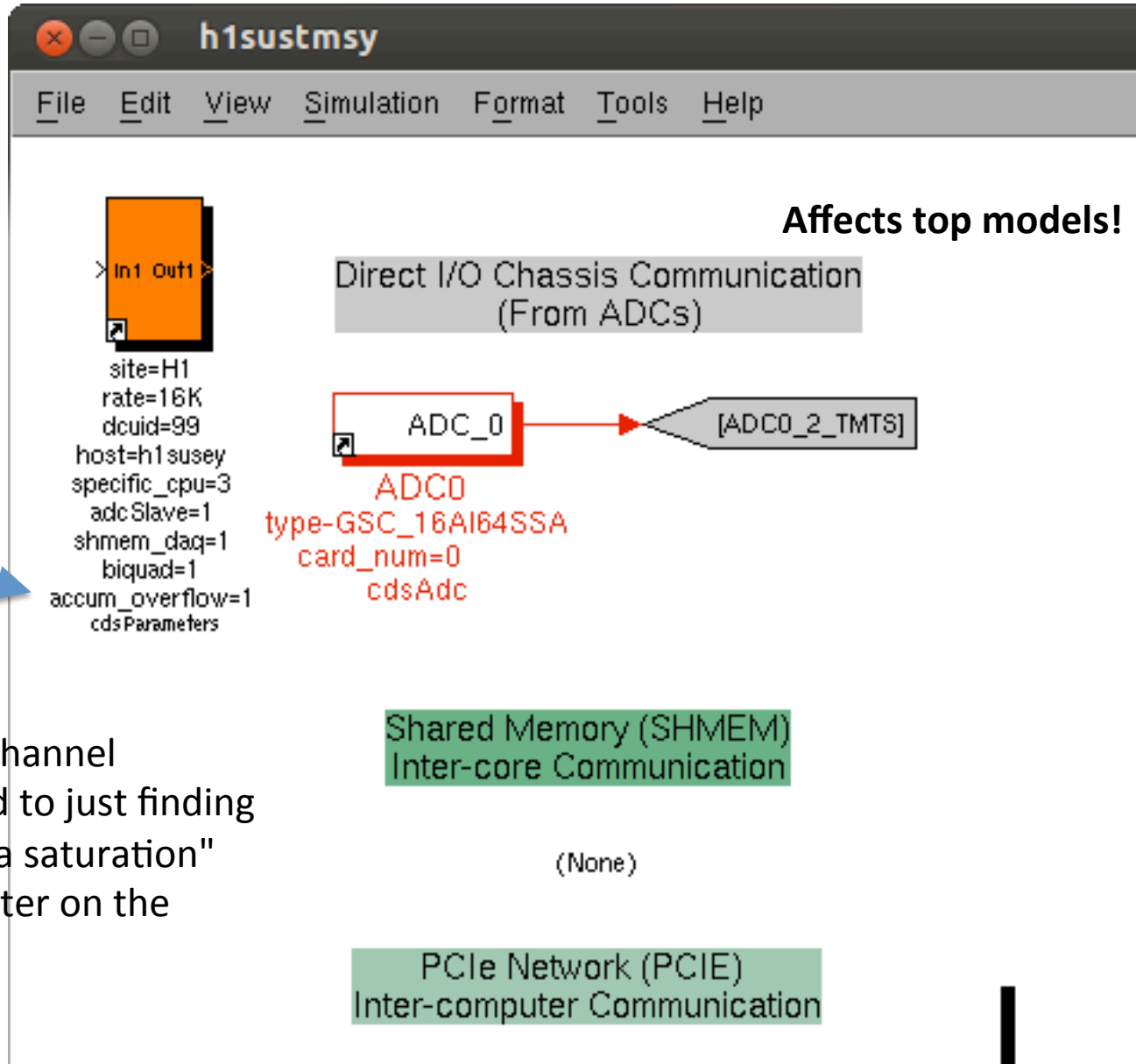
# Added CDS STATE Word and ODC Screen Link

Shows the health of the CDS system  
(which is \*not\* on the GDS\_TP screen!)



# Accumulate Individual Overflows

- changes the overflow counters for each DAC and ADC channel to accumulate until the reset button is hit (as opposed to clearing once a second)



- So can find \*which\* channel saturated, as opposed to just finding that "there has been a saturation" from the overall counter on the GDS\_TP screen.

# Left to do

- Fix filter files
- Take new safe.snaps
- The HAM SUS.