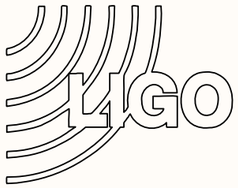


TP1 TP2
GND GND

VCC
GND

P3
1
2
VCC

PN3 connector
Newark

10B6044

P2

E17_P	1	2	E17_N
E18_P	3	4	E18_N
E19_P	5	6	E19_N
E0	7	8	E1
E2	9	10	E3
E4	11	12	E5
E6	13	14	E7
E8	15	16	E9
E10	17	18	E11
E12	19	20	E13
E14	21	22	E15
E16	23	24	OK2
GND	25	26	

female

P1

D17_P	1	2	D17_N
D18_P	3	4	D18_N
D19_P	5	6	D19_N
D0	7	8	D1
D2	9	10	D3
D4	11	12	D5
D6	13	14	D7
D8	15	16	D9
D10	17	18	D11
D12	19	20	D13
D14	21	22	D15
D16	23	24	OK1
GND	25	26	

male

H1 Handle, 3"
H2 Handle, 3"
Mouser
534-9109
H3 Ferrule
H4 Ferrule
H5 Ferrule
H6 Ferrule
Mouser
534-9121
M1 #6-32 3/8" flat
M2 #6-32 3/8" flat
M3 #6-32 3/8" flat
M4 #6-32 3/8" flat
McMaster-Carr
91099A215
H7 Standoff M-F
H8 Standoff M-F
H9 Standoff M-F
H10 Standoff M-F
H11 Standoff M-F
H12 Standoff M-F
Newark
56K3066

E1 BNC lock washer
E2 BNC lock washer
E3 BNC lock washer
E4 BNC lock washer
E5 BNC lock washer
E8 BNC lock washer
Newark
78M7215
H13 Standoff F-F
H14 Standoff F-F
H15 Standoff F-F
H16 Standoff F-F
H17 Standoff F-F
H18 Standoff F-F
Newark
56K3039

E9 BNC nut
E10 BNC nut
E11 BNC nut
E12 BNC nut
E13 BNC nut
E16 BNC nut
Newark
78M7214
M5 M4-8mm, flat
M6 M4-8mm, flat
M7 M4-8mm, flat
M8 M4-8mm, flat
M9 M4-8mm, flat
M10 M4-8mm, flat

PN4 Front Panel
LIGO
D1300798-v1
PN5 Rear Panel
LIGO
D1300799-v1
M11 M4-8mm, flat
M12 M4-8mm, flat
M13 M4-8mm, flat
M14 M4-8mm, flat
M15 M4-8mm, flat
M16 M4-8mm, flat
McMaster-Carr
91420A218

PN6 26 pin IDC
Newark
05M6783
PN7 DB25 male
Newark
95F9671
PN8 DB25 female
Newark
98F5808
PN9 Jack screw
PN10 Jack screw
Newark
80K5431

PN1 Banana jack
Newark
39F1574
PN2 Banana jack
Newark
39F1575

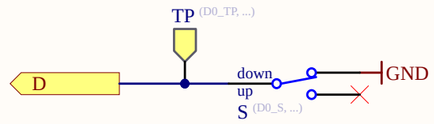
D0 PLLTestRig2.SchDoc
D1 PLLTestRig2.SchDoc
D2 PLLTestRig2.SchDoc
D3 PLLTestRig2.SchDoc
D4 PLLTestRig2.SchDoc
D5 PLLTestRig2.SchDoc
D6 PLLTestRig2.SchDoc
D7 PLLTestRig2.SchDoc
D8 PLLTestRig2.SchDoc
D9 PLLTestRig2.SchDoc
D10 PLLTestRig2.SchDoc
D11 PLLTestRig2.SchDoc
D12 PLLTestRig2.SchDoc
D13 PLLTestRig2.SchDoc
D14 PLLTestRig2.SchDoc
D15 PLLTestRig2.SchDoc
D16 PLLTestRig2.SchDoc
OK1 PLLTestRig3.SchDoc
D17 PLLTestRig4.SchDoc
D18 PLLTestRig4.SchDoc
D19 PLLTestRig4.SchDoc

E0 PLLTestRig5.SchDoc
E1 PLLTestRig5.SchDoc
E2 PLLTestRig5.SchDoc
E3 PLLTestRig5.SchDoc
E4 PLLTestRig5.SchDoc
E5 PLLTestRig5.SchDoc
E6 PLLTestRig5.SchDoc
E7 PLLTestRig5.SchDoc
E8 PLLTestRig5.SchDoc
E9 PLLTestRig5.SchDoc
E10 PLLTestRig5.SchDoc
E11 PLLTestRig5.SchDoc
E12 PLLTestRig5.SchDoc
E13 PLLTestRig5.SchDoc
E14 PLLTestRig5.SchDoc
E15 PLLTestRig5.SchDoc
E16 PLLTestRig5.SchDoc
OK2 PLLTestRig6.SchDoc
E17 PLLTestRig4.SchDoc
E18 PLLTestRig4.SchDoc
E19 PLLTestRig4.SchDoc

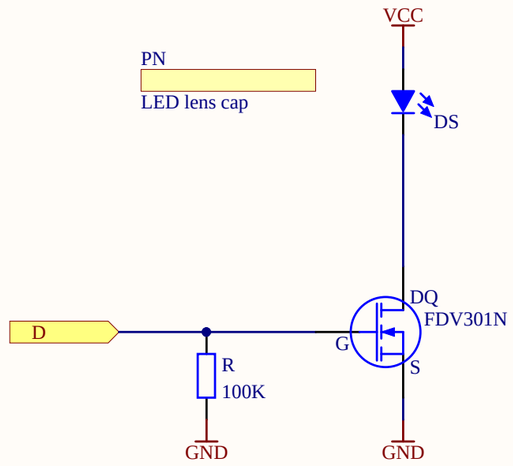
```
Digital Inputs:
D[0]     : Input 1 enable
D[1]     : Polarity input 1
D[2]     : Compensation 1 enable
D[3]     : Compensation 2 enable
D[ 9.. 4]: Gain slider input 1
D[10]:     Option enable
D[11]    : Output enable
D[12]    : Integrator enable
D[13]    : Filter enable
D[14]    : VCO compensation enable
D[15]    : Phase compensation enable
D[16]    : Excitation enable
```

```
Digital Outputs:
OK       : Voltages are within range

Analog Inputs:
D[19]    : Offset adjust

Analog Outputs:
D[17]    : Error signal monitor
D[18]    : Control signal monitor
```

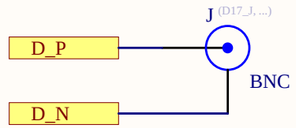
Title: **PLL Servo Tester**		
Size: B	Number: **D1300797**	Revision: **1**
Date: 10/3/2013		Sheet 1 of 6
File: D:\Users\..\PLLTestRig1.SchDoc		Drawn By: Daniel Sigg



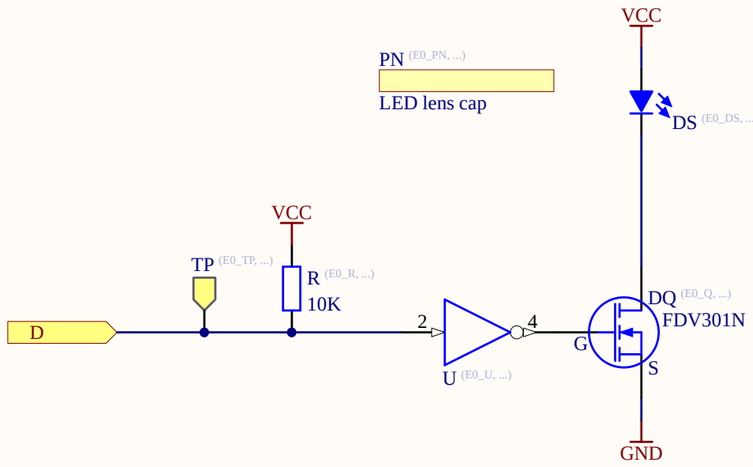
Title	**PLL Servo Tester**		
Size: A	Number: **D1300797**	Revision: **1**	
Date: 10/3/2013		Sheet 2 of 6	
File: D:\Users\..\PLLTestRig2.SchDoc		Drawn By: Daniel Sigg	



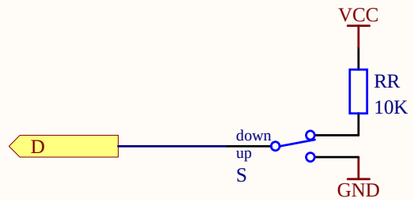
Title	**PLL Servo Tester**	
Size: A	Number: **D1300797**	Revision: **1**
Date: 10/3/2013		Sheet 3 of 6
File: D:\Users\..\PLLTestRig3.SchDoc		Drawn By: Daniel Sigg



Title	**PLL Servo Tester**	
Size: A	Number: **D1300797**	Revision: **1**
Date: 10/3/2013		Sheet 4 of 6
File: D:\Users\..\PLLTestRig4.SchDoc		Drawn By: Daniel Sigg



Title	**PLL Servo Tester**	
Size: A	Number: **D1300797**	Revision: **1**
Date: 10/3/2013		Sheet 5 of 6
File: D:\Users\..\PLLTestRig5.SchDoc		Drawn By: Daniel Sigg



Title	**PLL Servo Tester**	
Size: A	Number: **D1300797**	Revision: **1**
Date: 10/3/2013		Sheet 6 of 6
File: D:\Users\..\PLLTestRig6.SchDoc		Drawn By: Daniel Sigg