High/Low Voltage Piezo Driver Chassis Test Procedure
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The following checkout procedure pertains to the high/low voltage driver chassis used to drive the aLIGO OMC piezo transducers. The overview drawing number for the chassis is D1300485-v1. This overview document has links to schematic and panel files for all the components associated with the design.

This board uses lethal voltages. Do not attempt this procedure without training on safely working with exposed high voltages. Consult the LIGO Safety Officer for instructions on what constitutes sufficient training.

1. **General Setup:**
    a. With no external loads on the inputs or outputs to the board, apply the three DC power forms to the chassis at the appropriate connectors on the rear panel of the chassis.
        i. + low voltage = +18 volts
        ii. – low voltage = -18 volts
        iii. + high voltage = +200 volts
    b. Energize the chassis using the switch on the rear panel.
    c. Measure the quiescent operating voltages and currents associated with the full chassis and its internal regulator board. Visually check that the power LED indicators are lit. Record the results in F1300016-v1.

2. **High Voltage Section Tests:**
    a. **Output HV:** Measure the output high voltage of the HV driver board at the rear panel D-sub "To OMC HV/LV Piezos" Pins 1, 14. If needed, adjust potentiometer R42 until the output voltage at TP12 measures 100 volts +/- 1VDC. Record the measured value in F1300016-v1.
    b. **HVPS Current:** Record the HV power supply current in F1300016-v1
    c. **HV Output Monitor:** Measure and record the high voltage monitor at front panel D-sub **"Hi Voltage Mon.", pins 1 & 6**. Record the result in F1300016-v1.
    d. **Normal HV Signal Path DC Gain Check:** Apply 2 volt DC to front panel D-sub "Hi Voltage Drive", pins 1 & 6, positive and negative respectively. Measure the output voltage at TP12 and record the result in F1300016-v1. The output voltage should go down by 20 volts from the quiescent 100 volt operating point. The board is nominally set for a voltage gain of -20, but it is configurable for other gains.
    e. **Normal HV Signal Path AC Gain Check:** Using an SR-785 at 10mV drive level, measure the transfer function at 10, 100, and 1 kHz from J3, pins 1 & 2, positive and negative respectively, to J2, pins 2 & 7. Record the measured magnitude and phase in F1300016-v1.

f. **Alternate HV Signal Path AC Gain Check:** Using an SR-785, measure the transfer function at 100 Hz from front panel BNC "Alt. Drive", to J2, pins 2 & 7. Record the measured magnitude and phase in F1300016-v1.

g. **Output Current Limit Check:**
   i. With no drive voltages applied to the board, turn off the HV DC power supply used to power the HV driver board. After waiting for the output voltage to decay to less than 20-volts DC, use a clip-lead to short the high voltage at TP14 to ground through a 1k resistor.
   ii. Attach a voltmeter between TP14 and ground.
   iii. Briefly (<5 seconds) re-energize the 200-volt DC supply (so as not to thermally stress the output driver transistor), and measure the voltage from TP14 to ground as displayed on the voltmeter. Record the current limit (I_{Limit}) in Table 5 as calculated using Equation 1:

$$I_{Limit} = \frac{V_{TP14}}{1 \times 10^3} \qquad \text{(Equation 1)}$$

   iv. After recording the current limit, de-energize the HV DC power supply used to power the HV driver board and remove the clip lead from TP14. Disconnect the meter from TP14. Record the current in F1300016-v1.

h. **HV Path Output Referred Noise:** With no input to the HV driver board, and the input unterminated, use an SR785 to measure the differential output noise as observed on the AC monitor at J2, pins 2 & 7 at 100 and 1 kHz. Record the noise level in F1300016-v1

3. **Low Voltage Section Tests**
   a. **Internal 5VDC Regulator -** Measure the 5VDC regulator voltage at TP19. Record the result in F1300016-v1.
   b. **Trigger Logic -** Ensure the Logic Polarity Selector jumper (P3) is shorting pins 2 and 3 of the header. A trigger condition results if the front panel shutter trigger input is left unterminated. Verify that the red front panel fault light is lit while in this condition. Record the result in F1300016-v1
   c. **Trigger Clear -** Tie the "Shutter Trigger" input high by shorting TP19 to TP1 with a clip lead. Verify that the red front panel trigger LED is NOT lit in this condition. Record the result in F1300016-v1
   d. **LV Output Voltage -** Measure the output DC voltage of the LV driver board at the rear panel D-sub "To OMC HV/LV Piezos" Pins 2, 15. Record the measured value of the output voltages in F1300016-v1.
   e. **LV Output While Triggered -** While monitoring the voltage at TP29, disconnect the clip lead used to tie the shutter trigger input high. This simulates the condition wherein the OMC LV piezo has been clamped low

to act as a shutter. Measure the voltage at TP29 while in the triggered state, and record the result in F1300016-v1.

f. **LV Output Monitor:** Measure and record the low voltage monitor at front panel D-sub "Low Voltage Mon.", pins 1 & 6. Record the result in F1300016-v1.

g. **Normal Dither Path Transfer Function –** Using an SR785, measure the transfer function at 100 Hz and 5 kHz from the front panel "Low Voltage Drive" pins 1, 6, to the front panel "Low Voltage Mon." pins 2 and 7. Record the measured magnitude and phase in F1300016-v1.

h. **Alternate Dither Path Transfer Function –** Using an SR785, measure the transfer function at 100 Hz from the front panel "Alt Dither" BNC, to the front panel "Low Voltage Mon." pins 2 and 7. Record the measured magnitude and phase in F1300016-v1.

i. **LV Path Output Referred Noise:** With no input to the LV driver, and the drive input unterminated, use an SR785 to measure the differential output noise as observed on the front panel "Low Voltage Mon." at J2, pins 2 & 7 at 50Hz and 1kHz. Record the noise level in F1300016-v1