

**High/Low Voltage Piezo Driver Chassis Test Result Form**  
**R. Abbott**  
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Tested By:

Test Date:

Chassis Serial Number:

HV Board Serial Number:

LV Board Serial Number:

DC Regulator Serial Number:

**Table 1 HV Board (D060283-v1) Results**

Parameter	Required Value	Measured Value
DC Power LEDs	Illuminated while energized	
+ Regulated Voltage and total chassis current at feed to either board	+14.8 VDC +/- 0.5 VDC 182 mA +/- 10 mA	
- Regulated Voltage and total chassis current at feed to either board	-15.1 VDC +/- 0.5 VDC -130 mA +/- 10 mA	
HV output at TP12, and at rear panel D-sub "To OMC HV/LV Piezos" Pins 1, 14	100 VDC +/- 1 VDC	
+ High Voltage Supply Current	1.2 mA +/- 0.4 mA	
High voltage monitoring point at Front Panel "Hi Voltage Mon." pins 1&6	4 VDC +/-0.04 VDC	
Normal HV Path DC Gain Check	80 VDC +/- 1 VDC	
Normal HV Signal Path AC Gain Check at 10Hz (Magnitude)	-3.7 dB +/- 0.2dB	
Normal HV Signal Path AC Gain Check at 10Hz (Phase)	116 deg +/- 3 deg	
Normal HV Signal Path AC Gain Check at 100Hz (Magnitude)	-9.7dB +/- 0.2dB	
Normal HV Signal Path AC Gain Check at 100Hz (Phase)	162 deg +/- 3 deg	
Normal HV Signal Path AC Gain Check at 1kHz (Magnitude)	-14.7 dB +/- 0.2 dB	
Normal HV Signal Path AC Gain Check at 1kHz (Phase)	122 deg +/- 3 deg	
Alternate HV Signal Path AC Gain Check at 100Hz (Magnitude)	-9.7 dB +/- 0.2 dB	
Alternate HV Signal Path AC Gain Check at 100Hz (Phase)	162 deg +/- 3 deg	
Output Current Limit	3.9 mA, +/- 0.5 mA	

HV Path Output Referred Noise (measured at differential monitor) at 100Hz	Less than $1.9 \mu\text{V}/\sqrt{\text{Hz}}$	
HV Path Output Referred Noise (measured at differential monitor) at 1kHz	Less than $2.2 \mu\text{V}/\sqrt{\text{Hz}}$	

**Table 2 LV Board (D1300024-v1) Results**

<b>Parameter</b>	<b>Required Value</b>	<b>Measured Value</b>
5VDC regulator voltage at TP19	4.9 VDC +/- 0.1 VDC	
Front Panel "Trigger" LED lit during trigger condition	LED On (Red)	
Front Panel "Trigger" LED <i>NOT</i> lit when trigger input is tied high	LED Off	
Output DC voltage of the LV driver board at the rear panel D-sub "To OMC HV/LV Piezos" Pins 2, 15	9.8 VDC +/-0.05 VDC	
TP29 voltage during triggered condition	$\leq 1 \text{ mVDC}$	
Front Panel "Low Voltage Mon." pins 1 & 6	-19.6 VDC +/-0.1 VDC	
Normal Dither Path AC Gain Check at 100Hz (Magnitude)	-50.8 dB +/- 0.2 dB	
Normal Dither Path AC Gain Check at 100Hz (Phase)	80 deg +/- 3 deg	
Normal Dither Path AC Gain Check at 5 kHz (Magnitude)	27.6 dB +/- 0.2dB	
Normal Dither Path AC Gain Check at 5 kHz (Phase)	-97 deg +/- 3 deg	
Alternate Dither Path AC Gain Check at 100Hz (Magnitude)	-50.8 dB +/- 0.2 dB	
Alternate Dither Path AC Gain Check at 100Hz (Phase)	80 deg +/- 3 deg	
HV Path Output Referred Noise at 50 Hz	Less than $1 \mu\text{V}/\sqrt{\text{Hz}}$	
HV Path Output Referred Noise at 1 kHz	Less than $2.2 \mu\text{V}/\sqrt{\text{Hz}}$	