



LIGO Laboratory / LIGO Scientific Collaboration

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Advanced LIGO

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aLIGO 4 Ch. WFS RFPD Interface Chassis Test Procedure

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1 Overview

This procedure documents the testing of D1101906-v1, the aLIGO WFS Interface Chassis. This chassis supports up to 4 aLIGO WFS heads. The chassis houses 2 PD Interface boards (D1101865-v1), 1 Power Protection board (D1101816-v2), and an internal voltage regulator board

2 Testing

Each production chassis must be functionally tested and the results recorded in Section 4. It is assumed that the person using this procedure is familiar with Dynamic Signal Analyzers, and rudimentary test equipment including oscilloscopes and multimeters.

Serial Number Data

- Record all serial number data in Table 1

DC Tests

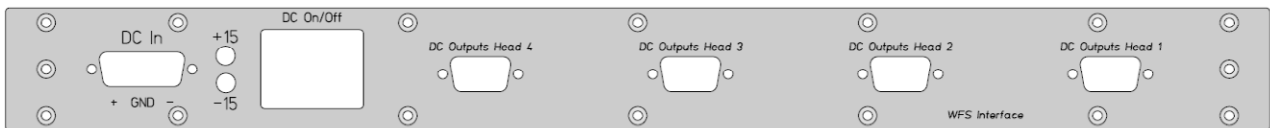
- Apply +/- 18, +/-200 mV Volts DC to the chassis under test and record front panel LED operation, total positive and negative power supply current, internal regulator output voltage and individual circuit board power supply currents as required in Table 2.

3 Reference for chassis front and rear panel layout

Figure 1: ISC WFS Interface Chassis Front Panel



Figure 2: ISC WFS Interface Chassis Rear Panel



4 Test Data Tables

4.1 General Information

Table 1 Serial Number Data

Chassis Serial Number	DC PWR Board PCB Serial #	Head 1-2 PCB Serial #	Head 3-4 PCB Serial #	Power Protection Board Serial #

4.2 DC Power Supply Data

Total chassis and individual circuit board quiescent current draw is recorded in Table 2. Use caution in believing the digital readouts of laboratory triple output power supplies. Their meters are not highly accurate. When in doubt, use a multimeter on the appropriate scale in series with the supply to be measured.

Table 2, Record of DC Test Data

Parameter	Typical Value	Allowable Tolerance	Measured Value
Front Panel +/- 15VDC Power LEDs	All Lit	N/A	
Front Panel +/- 18VDC Power LEDs	All Lit	N/A	
Rear Panel +/- 15VDC Power LEDs	All Lit	N/A	
+18VDC, +/-0.2VDC TOTAL supply current	400 mA	+/- 20mA	
-18VDC, +/-0.2VDC TOTAL supply current	380 mA	+/- 20mA	
Regulated Internal DC Voltage under full load (both boards)	15 VDC	+/- 0.25VDC	

4.3 DC Offsets on Each Rear-panel 9-pin D-sub Output

As a general measure of the health, the DC offset at the differential outputs for each channel must be measured. Using a multimeter, measure the DC offset at each of the 4 9-pin D-sub outputs on the rear panel. Each respective front panel input is to be left open during this measurement. Set the front panel gain switch to “HI”. Record the results in Table 3.

Table 3, Differential Output DC Offset

<i>Differential DC Measurement Point</i>	<i>Typical DC Offset</i>	<i>Allowable Range</i>	<i>Measured Value</i>	<i>Pass/Fail</i>
Head 1, pin 1-6	0VDC	+/- 15mV		
Head 1, pin 2-7	0VDC	+/- 15mV		
Head 1, pin 3-8	0VDC	+/- 15mV		
Head 1, pin 4-9	0VDC	+/- 15mV		
Head 2, pin 1-6	0VDC	+/- 15mV		
Head 2, pin 2-7	0VDC	+/- 15mV		
Head 2, pin 3-8	0VDC	+/- 15mV		
Head 2, pin 4-9	0VDC	+/- 15mV		
Head 3, pin 1-6	0VDC	+/- 15mV		
Head 3, pin 2-7	0VDC	+/- 15mV		
Head 3, pin 3-8	0VDC	+/- 15mV		
Head 3, pin 4-9	0VDC	+/- 15mV		
Head 4, pin 1-6	0VDC	+/- 15mV		
Head 4, pin 2-7	0VDC	+/- 15mV		
Head 4, pin 3-8	0VDC	+/- 15mV		
Head 4, pin 4-9	0VDC	+/- 15mV		

4.4 DC Transfer Function

The DC transfer function of each channel of the amplifier should be measured by injecting a 1 volt; +/-0.002V DC input into each the front panel D-sub. While each channel is under test, the from panel gain switch can be switched to verify the correct gain in each channel. Record all results in Table 4

Table 4 DC Transfer Function

DC Input Point on Front Panel	Measurement Point on Rear Panel	Magnitude (VDC)	Allowable Range	Measured Values	Pass/Fail
Head 1, pin 4-12	Head 1, pin 1-6 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 1, pin 3-11	Head 1, pin 2-7 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 1, pin 2-10	Head 1, pin 3-8 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 1, pin 1-9	Head 1, pin 4-9 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 2, pin 4-12	Head 2, pin 1-6 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 2, pin 3-11	Head 2, pin 2-7 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 2, pin 2-10	Head 2, pin 3-8 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 2, pin 1-9	Head 2, pin 4-9 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 3, pin 4-12	Head 3, pin 1-6 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 3, pin 3-11	Head 3, pin 2-7 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 3, pin 2-10	Head 3, pin 3-8 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 3, pin 1-9	Head 3, pin 4-9 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 4, pin 4-12	Head 4, pin 1-6 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 4, pin 3-11	Head 4, pin 2-7 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 4, pin 2-10	Head 4, pin 3-8 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	
Head 4, pin 1-9	Head 4, pin 4-9 (LOW/HI GAIN)	1V/10.09V	+/- (4mV/10mV)	/	