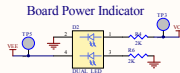
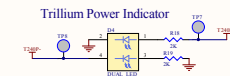
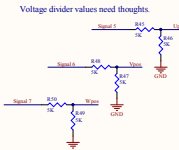
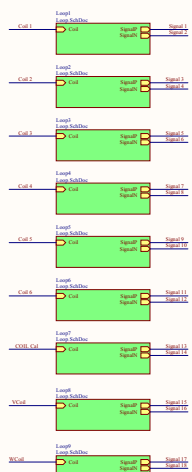


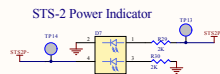
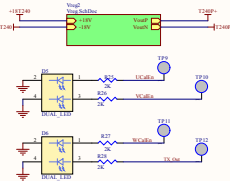
Input Power select



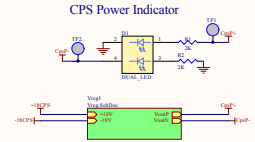
Board Power Indicator



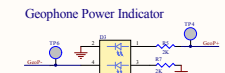
Trillium Power Indicator



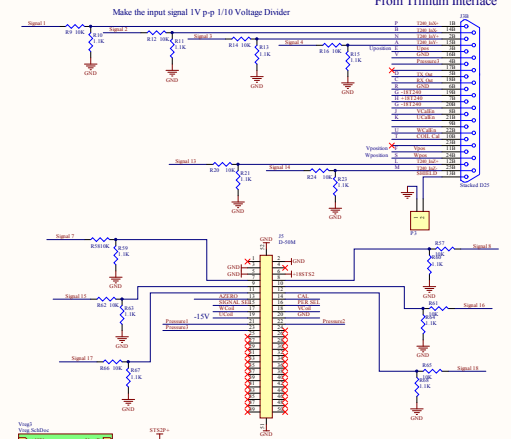
STS-2 Power Indicator



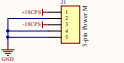
CPS Power Indicator



Geophone Power Indicator

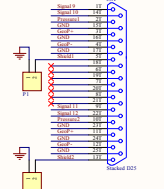


Uses a temporary 50-pin to 50-pin cable to test this.  
Getting -15V from U Coil front panel.  
Input analog sine wave into V & W Coil

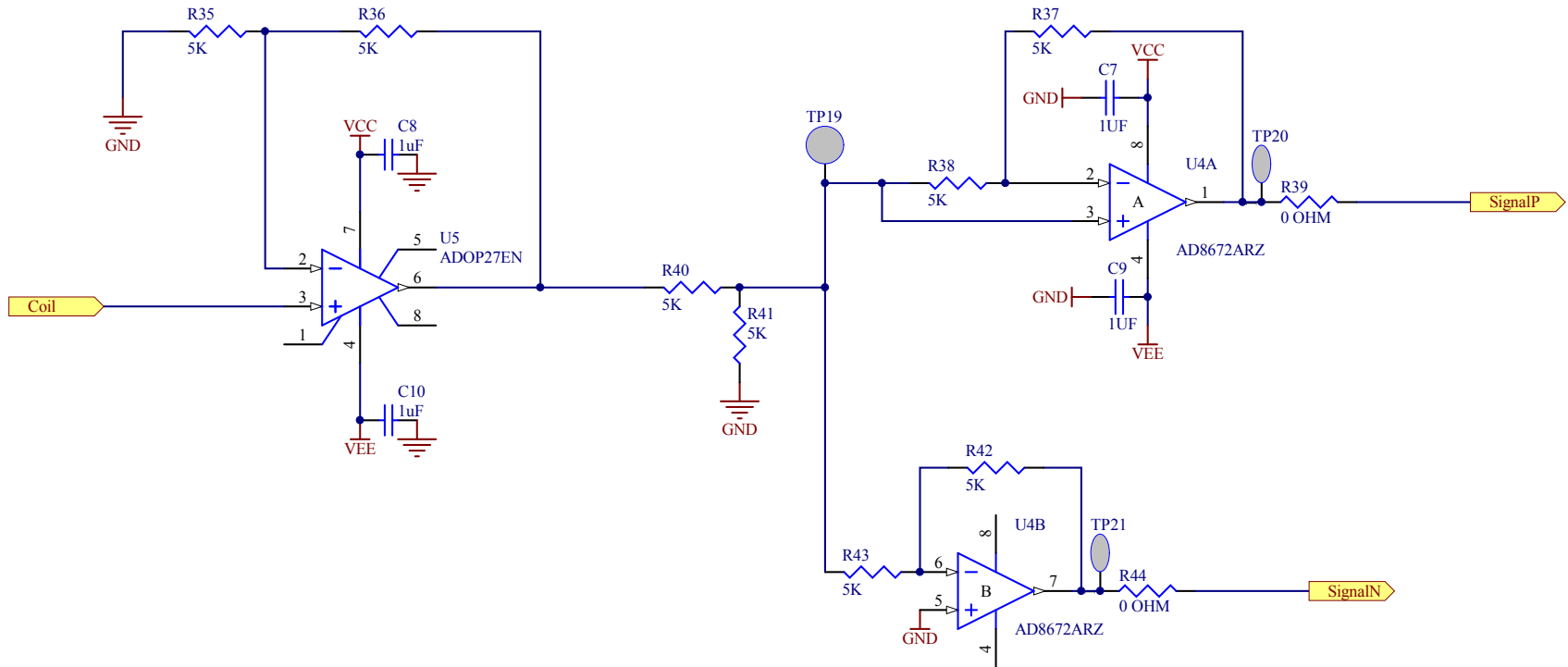


To CPS Interface

To GS-13s or L4C Interface



From Trillium Interface



Title **ISI Seismic Emulator Board Loopback**

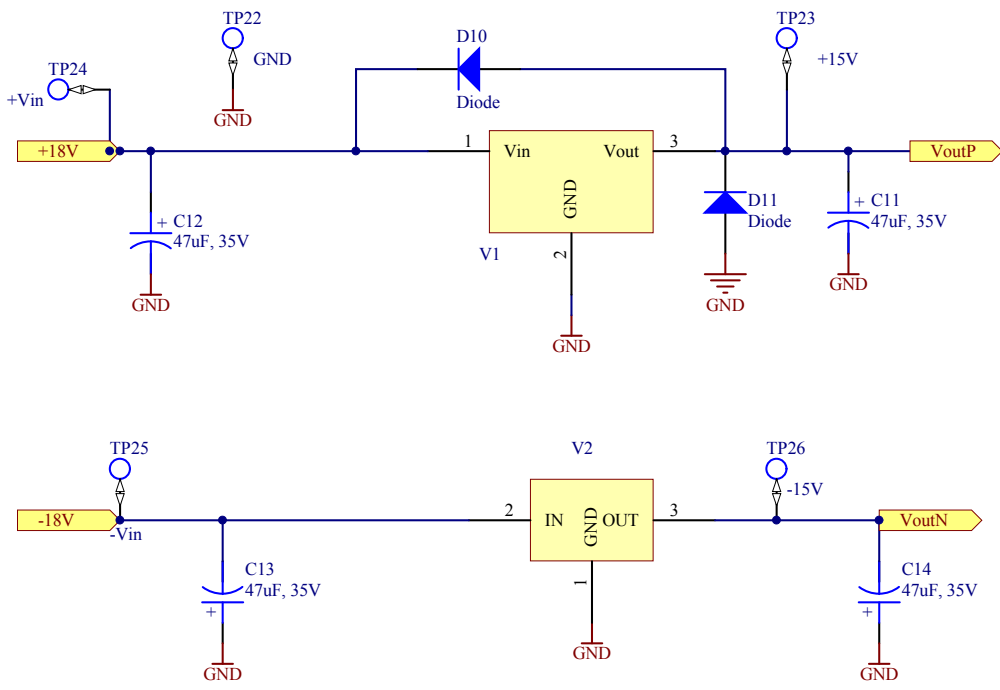
Size: **A**      DCC Number: **D1102340**

*Ligo Project*  
*California Institute of Technology*  
*Massachusetts Institute of Technology*



Drawn by: **Ben Abbott**      Date: **2/22/2012**      Revision: **v1**

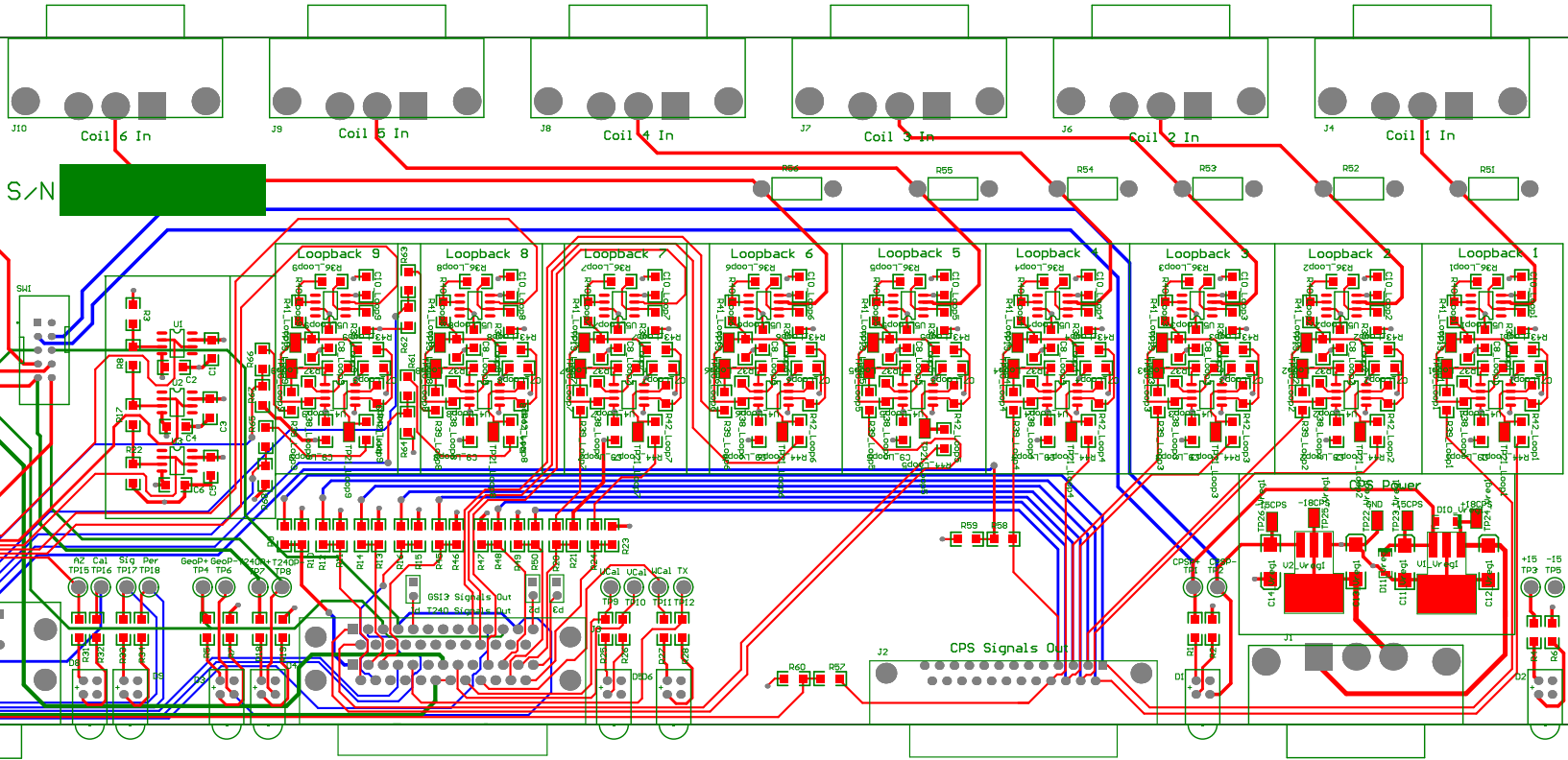
## Voltage Regulation



Title <b><i>ISI Seismic Emulator Vreg.</i></b>			
Size: <b>A</b>	DCC Number: <b>D1102340</b>		<i>Ligo Project</i> <i>California Institute of Technology</i> <i>Massachusetts Institute of Technology</i> 
Drawn by: <b>Ben Abbott</b>	Date: <b>2/22/2012</b>	Revision: <b>v1</b>	
File: C:\restored\Ben\Seismic\ISI\Tester Modules\Vreg.SchDoc			Time: 5:08:56 PM Sheet 3 of 3

ISI Seismic Emulator  
LIGO-D1102340

S/N



J10 Coil 6 In

J9 Coil 5 In

J8 Coil 4 In

J7 Coil 3 In

J6 Coil 2 In

J4 Coil 1 In

Loopback 9

Loopback 8

Loopback 7

Loopback 6

Loopback 5

Loopback 4

Loopback 3

Loopback 2

Loopback 1

ST2 Power

T24 Power

ST2 Signals Out

CPS Signals Out

Power

J1

J2

J3

J4

J5

J6

J7

J8

J9

J10

J11

J12

J13

J14

J15

J16

J17

J18

J19

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