LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

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aLIGO AA/AI Chassis Level Test Procedure		
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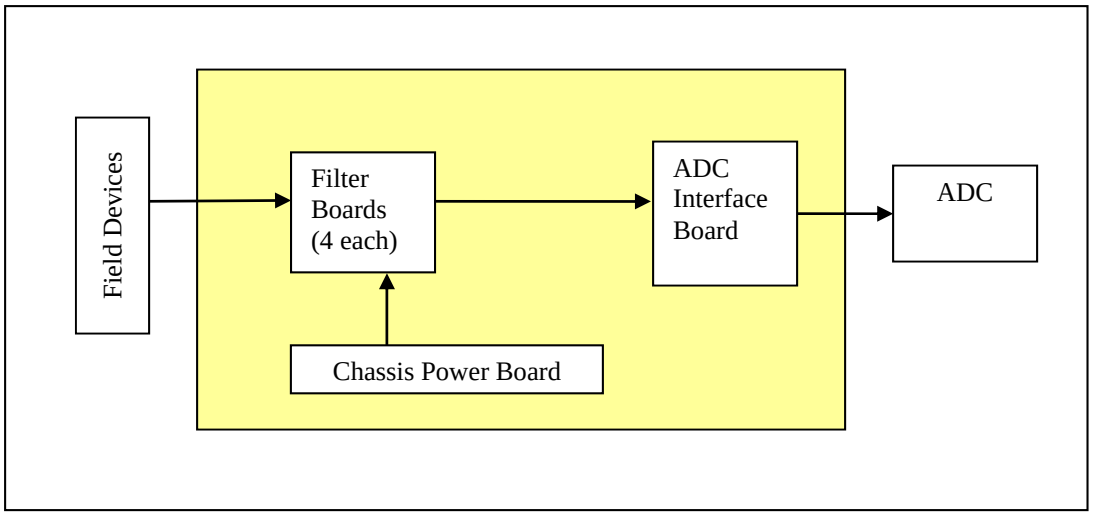
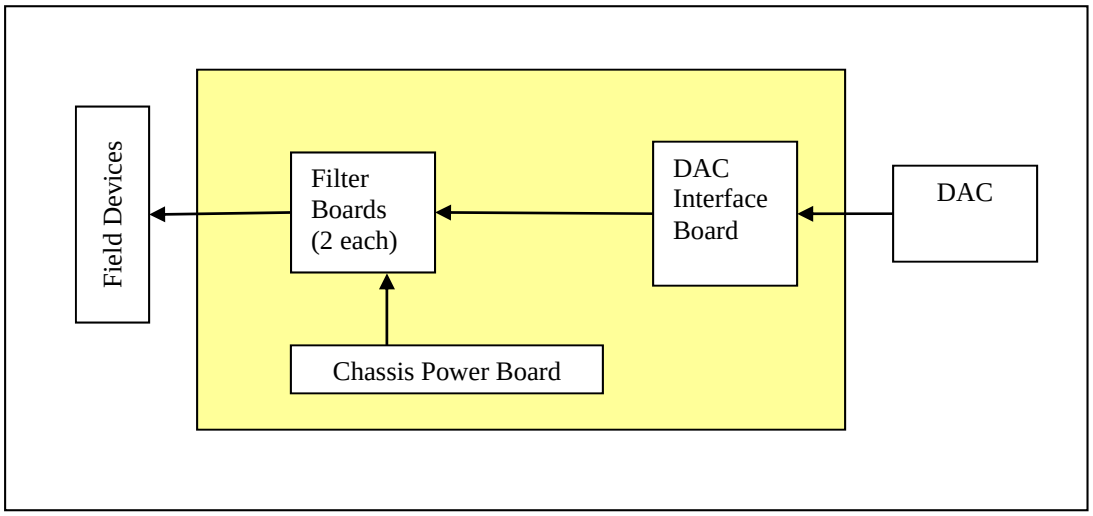
1 Introduction

The tests described below are required to verify the correct operation of the AdL AA Filter Boards when 4 boards are installed in an Anti-Alias chassis (D070081, all revisions, not for 18 bit AI chassis), or 2 boards installed in an Anti-Image chassis. This test plan assumes that the internal circuit boards have been fully tested and assembled into a chassis for final test. For simplicity, one document has been written to test both the AA and AI chassis. Since they are slightly different (the AI Chassis has half as many boards per chassis, and the signals go the opposite way), the tests specific to testing the AI chassis will be in **bold.** When testing an AI chassis, only the bold tests should be performed. When testing an AA chassis, both the bold and normal font tests should be performed. Similarly, any expected test results specific to the AI chassis will be in bold, with the AA chassis results in the normal font.

A block diagram of the AA chassis and connections to the field devices and ADC is shown below.



A block diagram of the AI chassis and connections to the field devices and DAC is shown below.



2 Test Equipment (for both)

Signal Generator
Oscilloscope
Power supplies

3 Serial Number Data

Chassis Serial Number	**Filter Board 1 S-Number**	**Filter Board 2 S-Number**	Filter Board 3 S-Number	Filter Board 4 S-Number

4 Tests

4.1 DC Power Supply Parameters

Record the input voltage and current in the table below. Values should be +/-50mA of the nominal values.

Table 1, Power Supply Data

Supply	**Nominal Current**	**Actual**	**Pass/Fail**
+15 V	610mA, +/-50mA, **290mA +/- 25mA**		
-15 V	590mA, +/-50mA, **300mA +/- 25mA**		

4.2 Filter Response

Using a function generator input a 5 Vpk-pk, 1 kHz sine wave into each channel under test per

Table 2. Note that due to the board connections, the nominal response is non-inverting, so trigger the scope from the function generator sync output and check for proper polarity (make sure they are in-phase). In

Table 2, connector J1A and J1B refer to the first filter board, J2A and J2B refer to the second board, J3A and J3B refer to the third and J4A and J4B refer to the fourth board. For the AI chassis, this mapping is not as literal, but the connector order is maintained.

Table 2

Chan	Input **Output (Front Panel of Chassis)**	Output **Input (ADC Interface Board)**	**Nominal Output on Scope (Vpk-pk) +/-10mV**	**Pass/ Fail**
1	**J1A- 1,6**	**P8- 1,35**	**5 Vpk-pk**	
2	J1A- 2,7	P8- 2,36	5 Vpk-pk	
3	**J1A- 3,8**	**P8- 3,37**	**5 Vpk-pk**	
4	J1A- 4,9	P8- 4,38	5 Vpk-pk	

5	**J1B- 1,6**	**P8- 5,39**	**5 Vpk-pk**	
6	J1B- 2,7	P8- 6,40	5 Vpk-pk	
7	**J1B- 3,8**	**P8- 7,41**	**5 Vpk-pk**	
8	J1B- 4,9	P8- 8,42	5 Vpk-pk	
9	**J2A- 1,6**	**P8- 9,43**	**5 Vpk-pk**	
10	J2A- 2,7	P8- 10,44	5 Vpk-pk	
11	**J2A- 3,8**	**P8- 11,45**	**5 Vpk-pk**	
12	J2A- 4,9	P8- 12,46	5 Vpk-pk	
13	**J2B- 1,6**	**P8- 13,47**	**5 Vpk-pk**	
14	J2B- 2,7	P8- 14,48	5 Vpk-pk	
15	**J2B- 3,8**	**P8- 15,49**	**5 Vpk-pk**	
16	J2B- 4,9	P8- 16,50	5 Vpk-pk	
17	**J3A- 1,6**	**P8- 17,51**	**5 Vpk-pk**	
18	J3A- 2,7	P8- 18,52	5 Vpk-pk	
19	**J3A- 3,8**	**P8- 19,53**	**5 Vpk-pk**	
20	J3A- 4,9	P8- 20,54	5 Vpk-pk	
21	**J3B- 1,6**	**P8- 21,55**	**5 Vpk-pk**	
22	J3B- 2,7	P8- 22,56	5 Vpk-pk	
23	**J3B- 3,8**	**P8- 23,57**	**5 Vpk-pk**	
24	J3B- 4,9	P8- 24,58	5 Vpk-pk	
25	**J4A- 1,6**	**P8- 25,59**	**5 Vpk-pk**	
26	J4A- 2,7	P8- 26,60	5 Vpk-pk	
27	**J4A- 3,8**	**P8- 27,61**	**5 Vpk-pk**	
28	J4A- 4,9	P8- 28,62	5 Vpk-pk	
29	**J4B- 1,6**	**P8- 29,63**	**5 Vpk-pk**	
30	J4B- 2,7	P8- 30,64	5 Vpk-pk	
31	**J4B- 3,8**	**P8- 31,65**	**5 Vpk-pk**	
32	J4B- 4,9	P8- 32,66	5 Vpk-pk	