LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

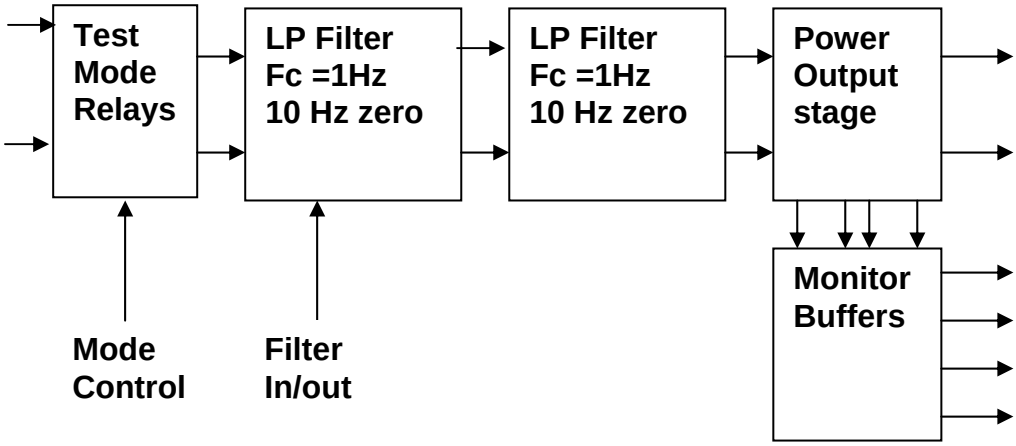
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP68P……Serial No ……
Test Engineer ….Xen……..……
Date ……10/3/10……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal gen	Agilent	33250A	

Unit……T_TOP68P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Also replaced U3, U1 and C12 on CH3.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

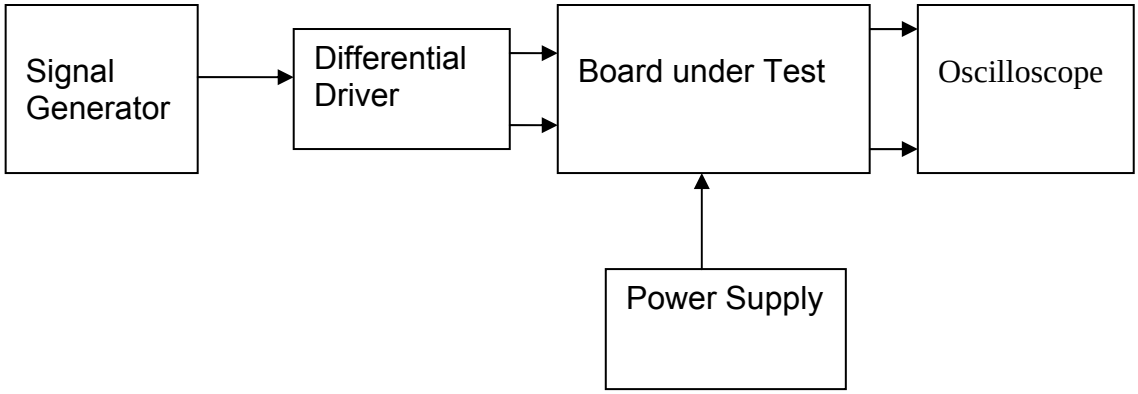
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP68P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.03	1mV	√
+15v TP4	14.95	1mV	√
-15v TP6	-15.03	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP68P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.45	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.68	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.68	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.25	3v to 3.4v	√
Ch2	3.25	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.25	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.202	Pin 1 to Pin 2	1.202	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.202	√
3	1.15-1.25v	1.202	Pin 9 to Pin 10	1.202	√
4	1.15-1.25v	1.202	Pin 13 to Pin 14	1.202	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.479	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.482	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.482	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.4	√	-24.5	√	-24.4	√	-24.5	√
-7v	-17.0	√	-17.2	√	-17.1	√	-17.2	√
-5v	-12.2	√	-12.3	√	-12.2	√	-12.4	√
-1v	-2.41	√	-2.41	√	-2.4	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.1	√	17.0	√	17.1	√
10v	24.3	√	24.4	√	24.3	√	24.3	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.43	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

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http://www.ligo.caltech.edu/

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

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TEST PLAN

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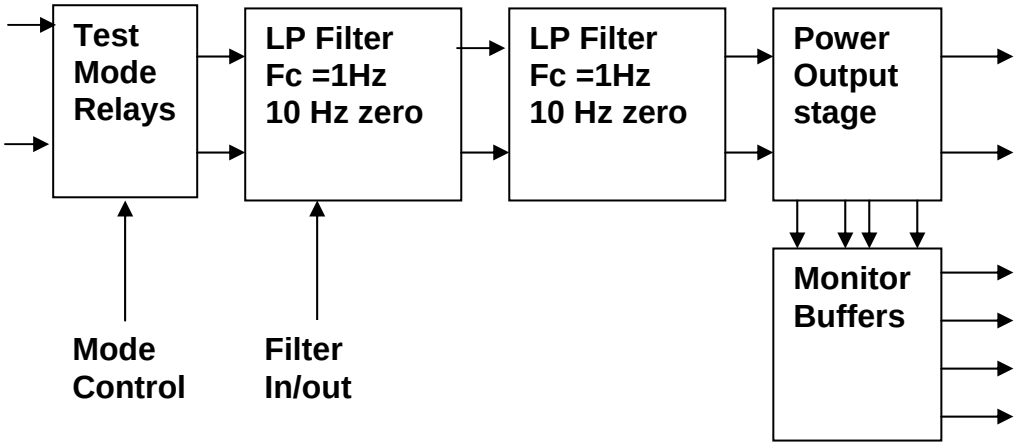

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Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

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Links:

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J2

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2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

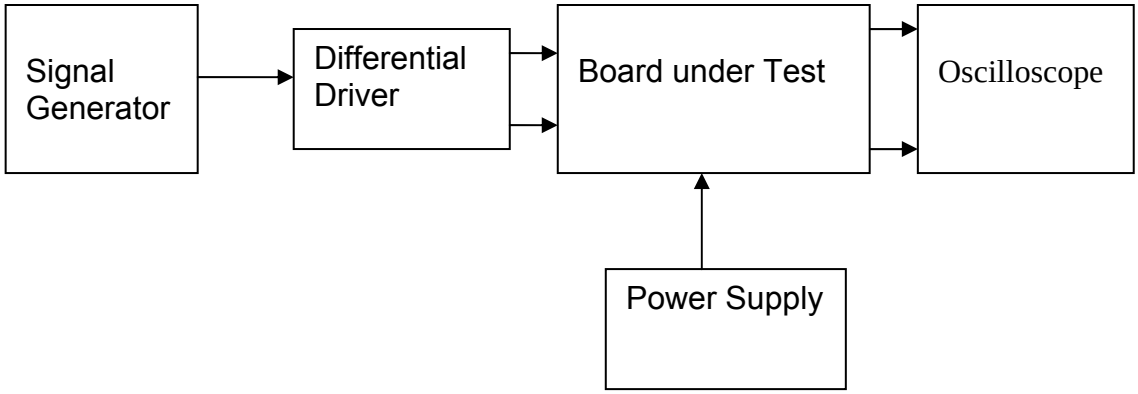
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.13	1mV	√
+15v TP4	14.95	1mV	√
-15v TP6	-15.07	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP_1P……Serial No ……
Test Engineer ….Xen…….
Date ……19/10/09…….

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP1P……Serial No ……
Test Engineer ….Xen……..
Date ……19/10/09……...

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.85	4.85	**4.7v to 5v**	√
Ch2	4.75	4.85	4.85	**4.7v to 5v**	√
Ch3	4.75	4.85	4.85	**4.7v to 5v**	√
Ch4	4.75	4.85	4.85	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.45	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.45	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP1P……Serial No ……
Test Engineer ….Xen…….
Date ……19/10/09…….

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.1	3v to 3.4v	√
Ch2	3.1	3v to 3.4v	√
Ch3	3.1	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.45	0.4v to 0.5v	√
Ch2	0.45	0.4v to 0.5v	√
Ch3	0.45	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.15	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP1P……Serial No ……
Test Engineer ….Xen……
Date ……19/10/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**1.15-1.25v**	1.22	Pin 1 to Pin 2	1.22	√
2	**1.15-1.25v**	1.22	Pin 5 to Pin 6	1.22	√
3	**1.15-1.25v**	1.22	Pin 9 to Pin 10	1.22	√
4	**1.15-1.25v**	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**0.47-0.49v**	0.486	Pin 3 to Pin 4	0.487	√
2	**0.47-0.49v**	0.488	Pin 7 to Pin 8	0.489	√
3	**0.47-0.49v**	0.484	Pin 11 to Pin 12	0.486	√
4	**0.47-0.49v**	0.485	Pin 15 to Pin 16	0.487	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP1P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.0	√	-24.2	√	-24.0	√	-24.2	√
-7v	-16.9	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	16.9	√	16.9	√
10v	24.0	√	24.0	√	24.0	√	24.0	√

Unit……T_TOP1P……Serial No ……
Test Engineer ….Xen…….
Date …….19/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the outputs in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-148dB	-111dB	457Hz
Channel 2	Channel 1	-143dB	-111dB	457Hz
Channel 2	Channel 3	-136dB	-112dB	912Hz
Channel 3	Channel 2	-137dB	-108dB	209Hz
Channel 3	Channel 4	-142dB	-111dB	457Hz
Channel 4	Channel 3	-142dB	-108dB	457Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP_1P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5 v**	3.44	√
Ch2	**3.3-3.5 v**	3.46	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

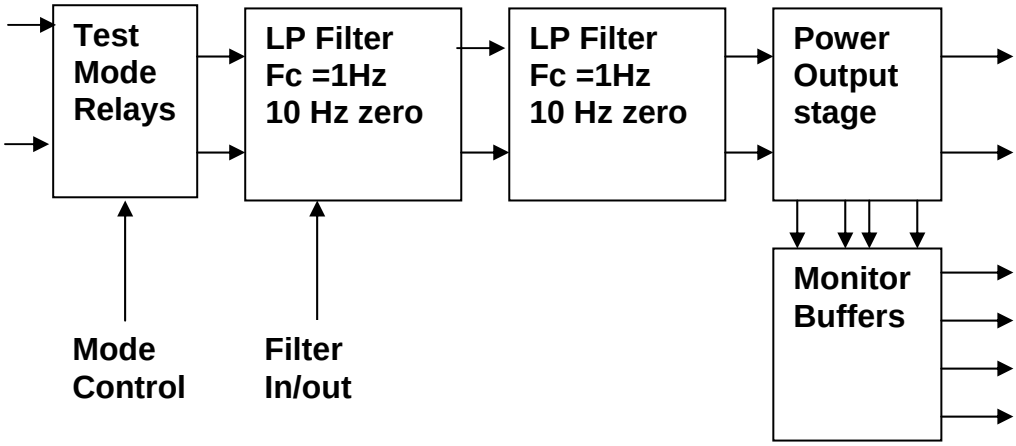
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP2P……Serial No ……
Test Engineer ….Xen……
Date …….20/10/09…..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP2P……Serial No ……
Test Engineer ….Xen……..
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP2P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP2P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

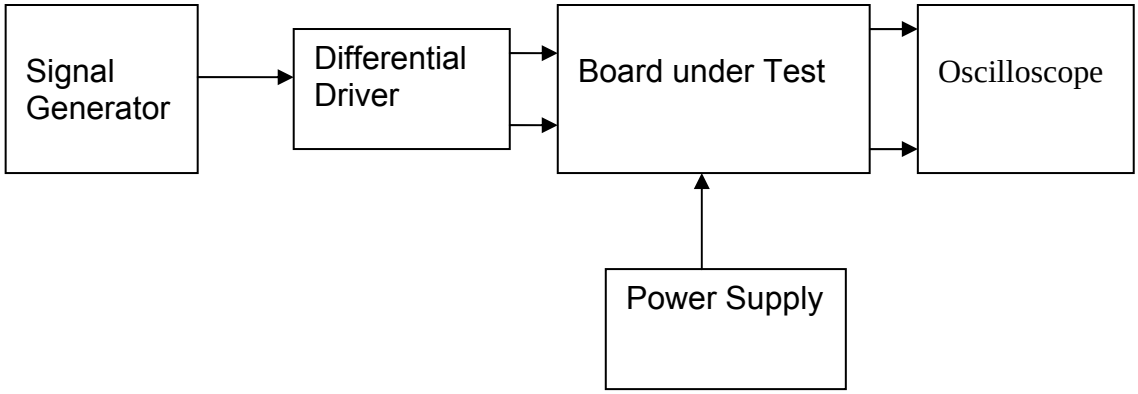
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP2P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.08	1mV	√
+15v TP4	14.85	1mV	√
-15v TP6	-15.08	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP2P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP2P……Serial No ……
Test Engineer ….Xen……..
Date ……19/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.85	4.85	**4.7v to 5v**	√
Ch2	4.75	4.85	4.85	**4.7v to 5v**	√
Ch3	4.75	4.85	4.85	**4.7v to 5v**	√
Ch4	4.75	4.85	4.85	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.65	**0.48 to 0.75v**	√
Ch3	0.60	**0.48 to 0.75v**	√
Ch4	0.60	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP2P……Serial No ……
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Date ……19/10/09……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP2P……Serial No ……
Test Engineer ….Xen……
Date ……19/10/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.486	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.486	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.487	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP2P……Serial No ……
Test Engineer ….Xen…….
Date …….20/10/09……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.1	√	-24.0	√	-24.1	√
-7v	-17.0	√	-16.9	√	-16.9	√	-16.9	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	17.0	√	16.9	√	17.0	√	17.0	√
10v	24.0	√	24.0	√	24.1	√	24.1	√

Unit……T_TOP2P……Serial No ……
Test Engineer ….Xen…….
Date …….20/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	**Channel 2**	-133dB	-112dB	827Hz
Channel 2	**Channel 1**	-141dB	-117dB	495Hz
Channel 2	**Channel 3**	-137dB	-113dB	832Hz
Channel 3	**Channel 2**	-139dB	-111dB	457Hz
Channel 3	**Channel 4**	-137dB	-115dB	478Hz
Channel 4	**Channel 3**	-141dB	-114dB	473Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	**Channel 2**		
Channel 2	**Channel 1**		
Channel 2	**Channel 3**		
Channel 3	**Channel 2**		
Channel 3	**Channel 4**		
Channel 4	**Channel 3**		

Unit……T_TOP2P……Serial No ……
Test Engineer ….Xen……..
Date …….20/10/09……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5 v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace link W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

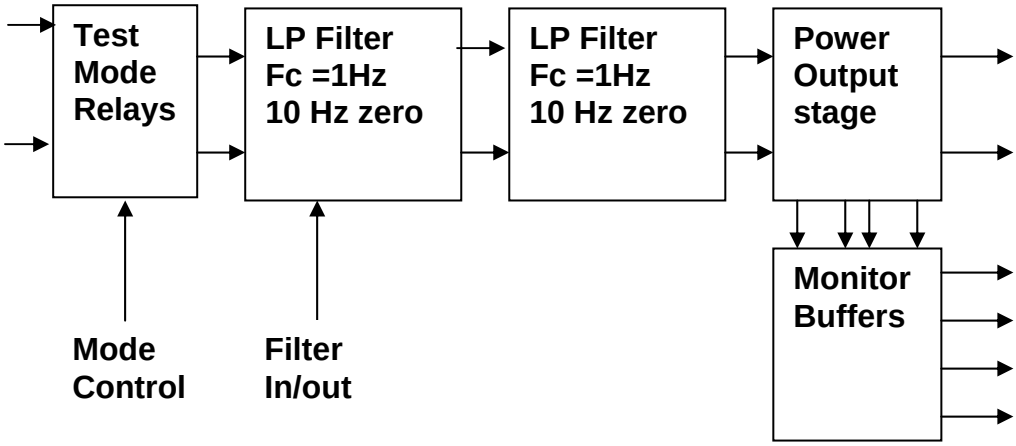
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP3P……Serial No ……
Test Engineer …..Xen……
Date ……..20/10/09……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP3P……Serial No ……
Test Engineer ….Xen……..
Date …….20/10/09……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
DVM	Fluke	77III	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP3P……Serial No ……
Test Engineer ….Xen…….
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP3P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

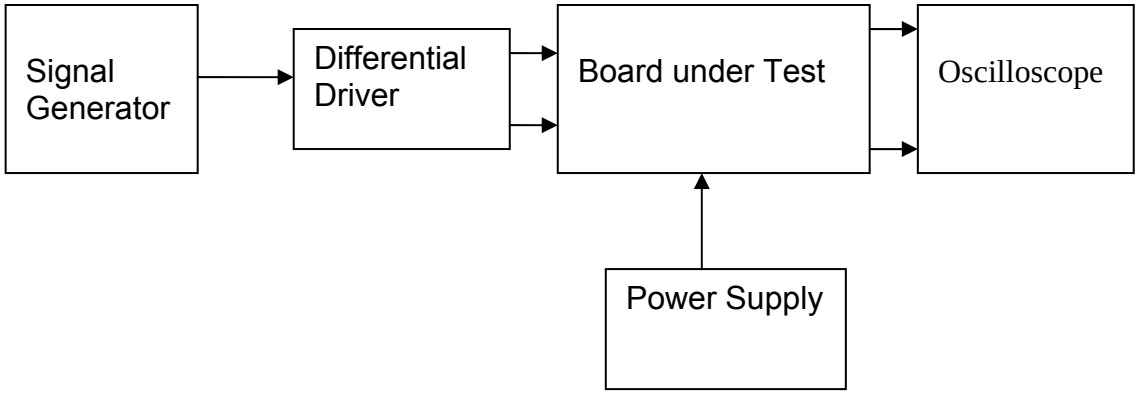
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP3P……Serial No ……
Test Engineer ….Xen……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.98	1mV	√
+15v TP4	14.95	1mV	√
-15v TP6	-14.99	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP3P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP3P……Serial No ……
Test Engineer ….Xen……..
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.65	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP3P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.1	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.45	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.44	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP3P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**1.15-1.25v**	1.22	Pin 1 to Pin 2	1.22	√
2	**1.15-1.25v**	1.22	Pin 5 to Pin 6	1.22	√
3	**1.15-1.25v**	1.22	Pin 9 to Pin 10	1.22	√
4	**1.15-1.25v**	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**0.47-0.49v**	0.485	Pin 3 to Pin 4	0.487	√
2	**0.47-0.49v**	0.485	Pin 7 to Pin 8	0.486	√
3	**0.47-0.49v**	0.485	Pin 11 to Pin 12	0.487	√
4	**0.47-0.49v**	0.485	Pin 15 to Pin 16	0.489	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP3P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.1	√	-24.0	√	-24.2	√
-7v	-17.0	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.1	√	12.0	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.1	√	24.0	√	24.1	√	24.1	√

Unit……T_TOP3P……Serial No ……
Test Engineer ….Xen…….
Date …….20/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-136dB	-113dB	417Hz
Channel 2	Channel 1	-154dB	-115dB	363Hz
Channel 2	Channel 3	-144dB	-115dB	525Hz
Channel 3	Channel 2	-148dB	-114dB	462Hz
Channel 3	Channel 4	-151dB	-115dB	363Hz
Channel 4	Channel 3	-141dB	-110dB	692Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP3P……Serial No ……
Test Engineer ……..Xen……..
Date ……..21/10/09……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5 v**	3.43	√
Ch3	**3.3-3.5 v**	3.43	√
Ch4	**3.3-3.5 v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

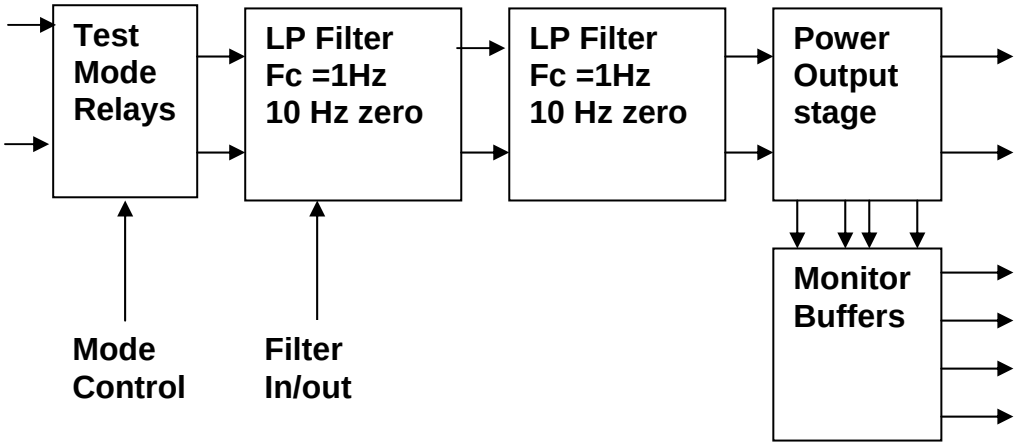
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP4P……Serial No ……
Test Engineer …..Xen……
Date ……..21/10/09……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP4P……Serial No ……
Test Engineer ….Xen……..
Date …….21/10/09……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP4P……Serial No ……
Test Engineer .Xen…….
Date ……..21/10/09…….

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP4P……Serial No ……
Test Engineer ….Xen……
Date …….21/10/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

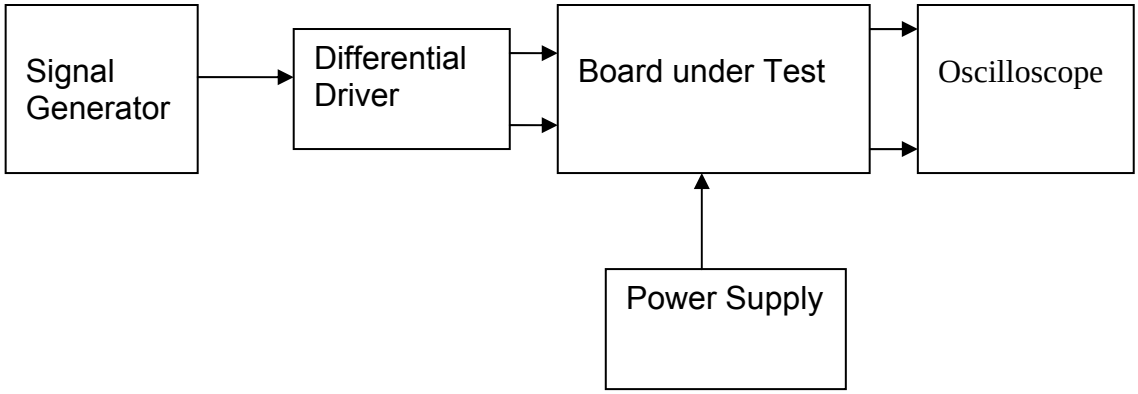
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP4P……Serial No ……
Test Engineer ….Xen……
Date …….21/10/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.97	1mV	√
+15v TP4	14.88	1mV	√
-15v TP6	-15.06	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP4P……Serial No ……
Test Engineer ….Xen…….
Date …….21/10/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP4P……Serial No ……
Test Engineer ….Xen……..
Date …….21/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.85	4.85	**4.7v to 5v**	√
Ch2	4.75	4.85	4.85	**4.7v to 5v**	√
Ch3	4.75	4.85	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.64	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.65	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP4P……Serial No ……
Test Engineer ….Xen……..
Date …….21/10/09……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.0	3v to 3.4v	√
Ch2	3.1	3v to 3.4v	√
Ch3	3.1	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.44	0.4v to 0.5v	√
Ch2	0.44	0.4v to 0.5v	√
Ch3	0.44	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP4P……Serial No ……
Test Engineer ….Xen……
Date …….21/10/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP4P……Serial No ……
Test Engineer ….Xen…….
Date …….21/10/09……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.2	√	-24.1	√	-24.1	√
-7v	-17.0	√	-17.0	√	-16.9	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	17.0	√	17.0	√	17.0	√	16.9	√
10v	24.2	√	24.2	√	24.1	√	24.1	√

Unit……T_TOP4P……Serial No ……
Test Engineer ….Xen…….
Date …….21/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-134dB	-112dB	457Hz
Channel 2	Channel 1	-137dB	-114dB	347Hz
Channel 2	Channel 3	-136dB	-112dB	251Hz
Channel 3	Channel 2	-134dB	-112dB	1kHz
Channel 3	Channel 4	-134dB	-112dB	1kHz
Channel 4	Channel 3	-137dB	-110dB	229Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP4P……Serial No ……
Test Engineer ….Xen……..
Date …….21/10/09……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

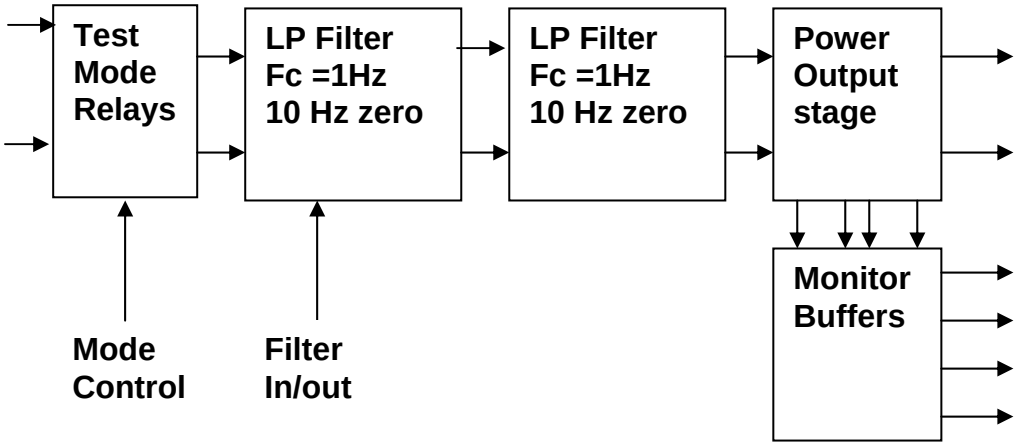
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP5P……Serial No ……
Test Engineer ….Xen……
Date …….21/10/09……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP5P……Serial No ……
Test Engineer ….Xen……..
Date …….21/10/09……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP5P……Serial No ……
Test Engineer ….Xen…….
Date …….21/10/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP5P……Serial No ……
Test Engineer ….Xen……
Date …….21/10/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

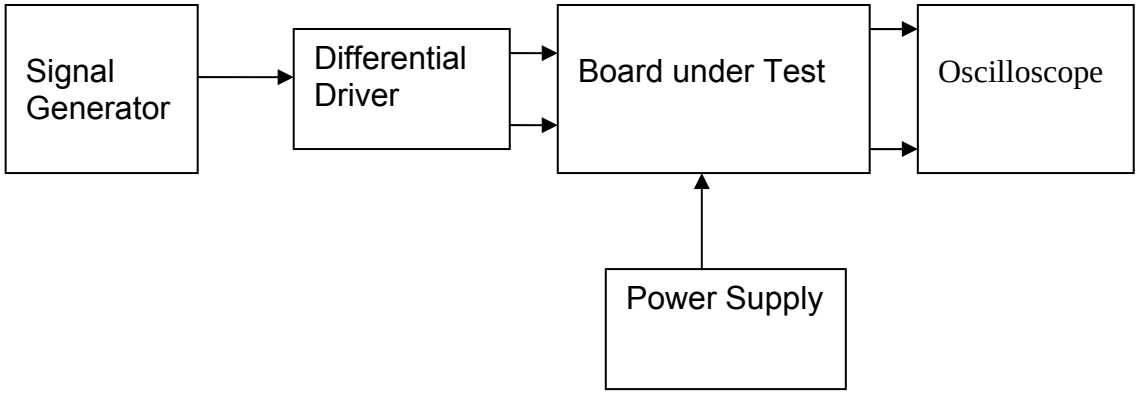
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP5P……Serial No ……
Test Engineer ….Xen……
Date …….21/10/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.98	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-14.92	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP5P……Serial No ……
Test Engineer ….Xen…….
Date …….21/10/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP5P……Serial No ……
Test Engineer ….Xen……..
Date …….23/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP5P……Serial No ……
Test Engineer ….Xen……..
Date …….21/10/09……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.1	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.1	3v to 3.4v	√
Ch4	3.1	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.44	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.45	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP5P……Serial No ……
Test Engineer ….Xen……
Date …….21/10/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.486	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.487	Pin 7 to Pin 8	0.488	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.1	√	-24.0	√	-24.0	√
-7v	-17.0	√	-17.0	√	-17.0	√	-16.9	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	17.0	√	16.9	√	16.8	√	16.9	√
10v	24.1	√	24.0	√	24.0	√	24.0	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-137dB	-112dB	794Hz
Channel 2	Channel 1	-135dB	-113dB	831Hz
Channel 2	Channel 3	-128dB	-112dB	240Hz
Channel 3	Channel 2	-136dB	-110dB	316Hz
Channel 3	Channel 4	-140dB	-112dB	316Hz
Channel 4	Channel 3	-140dB	-106dB	209Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP5P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.42	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

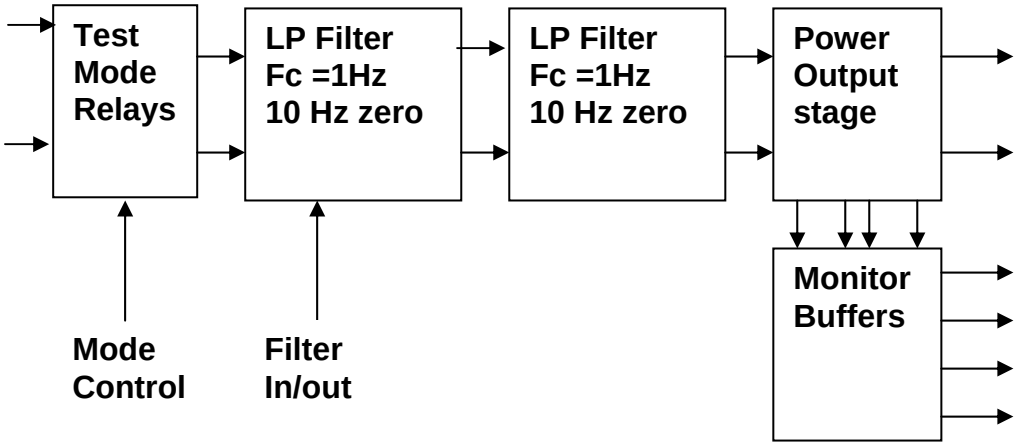
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP6P……Serial No ……
Test Engineer …..Xen……
Date ……..22/10/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP6P……Serial No ……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

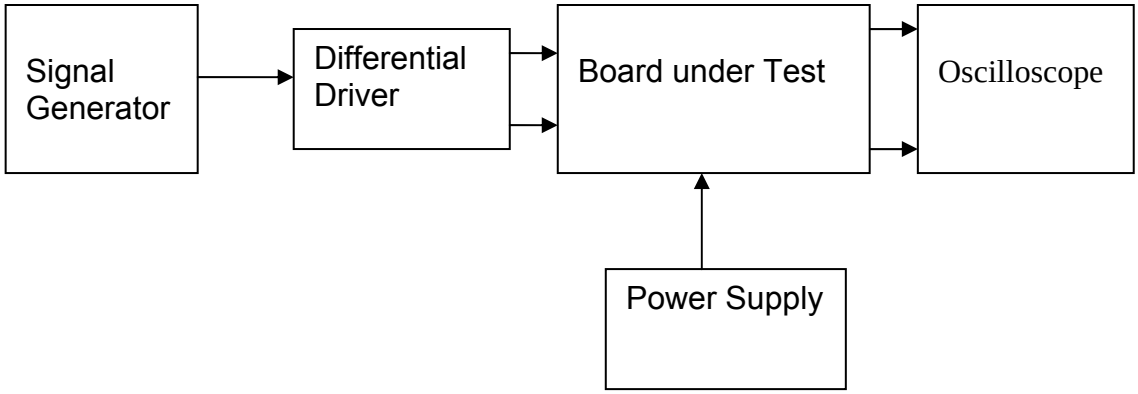
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.06	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-15.00	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP6P……Serial No ……
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Date ……..22/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP6P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.1	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.45	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP6P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP6P……Serial No ……
Test Engineer …..Xen…….
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.0	√	-24.0	√	-24.1	√
-7v	-17.0	√	-16.9	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	16.9	√	16.9	√
10v	24.0	√	24.0	√	24.0	√	24.0	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-135dB	-111dB	724Hz
Channel 2	Channel 1	-135dB	-108dB	417Hz
Channel 2	Channel 3	-133dB	-111dB	692Hz
Channel 3	Channel 2	-140dB	-111dB	437Hz
Channel 3	Channel 4	-136dB	-115dB	955Hz
Channel 4	Channel 3	-132dB	-111dB	229Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP6P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.32	√
Ch2	**3.3-3.5v**	3.33	√
Ch3	**3.3-3.5v**	3.32	√
Ch4	**3.3-3.5v**	3.32	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

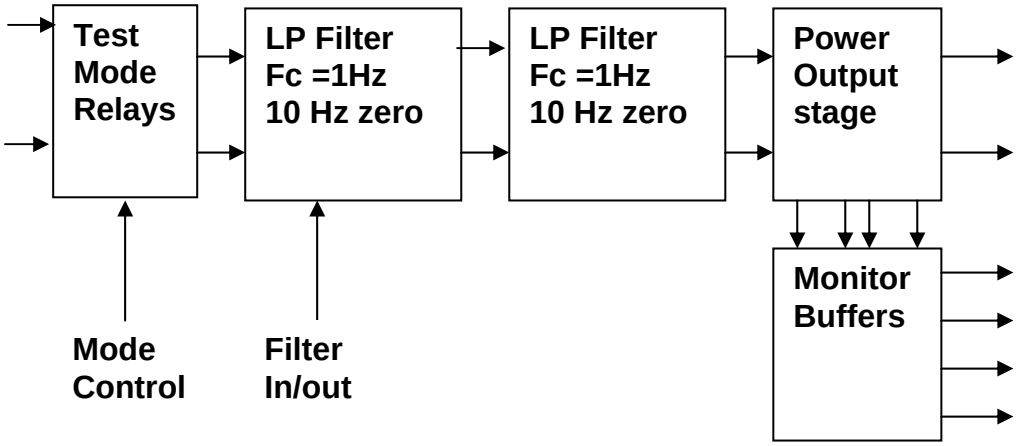
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP7P……Serial No ……
Test Engineer ……..…Xen……
Date ……..23/10/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP7P……Serial No ……
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Date …….22/10/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP7P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

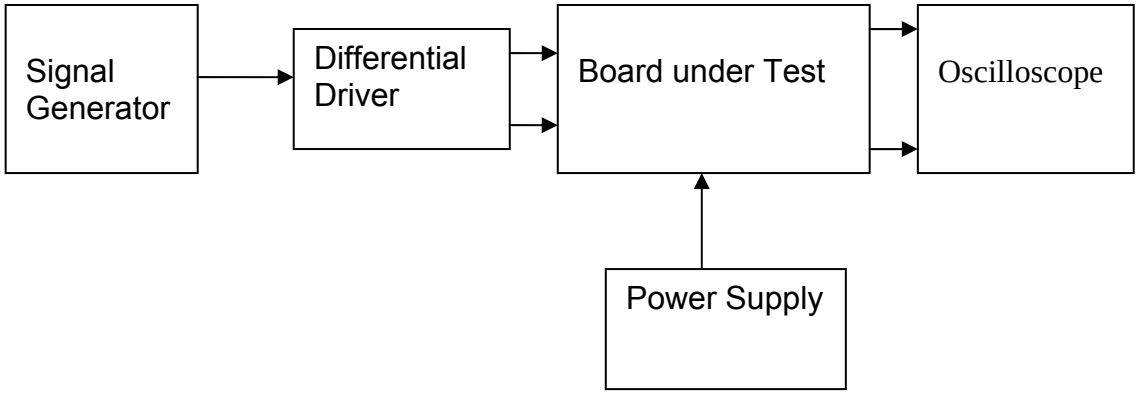
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP7P……Serial No ……
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Date …….22/10/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.03	1mV	√
+15v TP4	14.91	1mV	√
-15v TP6	-15.14	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP7P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP7P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.65	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP7P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.1	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.15	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.44	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**1.15-1.25v**	1.22	Pin 1 to Pin 2	1.22	√
2	**1.15-1.25v**	1.22	Pin 5 to Pin 6	1.22	√
3	**1.15-1.25v**	1.22	Pin 9 to Pin 10	1.22	√
4	**1.15-1.25v**	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**0.47-0.49v**	0.485	Pin 3 to Pin 4	0.487	√
2	**0.47-0.49v**	0.485	Pin 7 to Pin 8	0.486	√
3	**0.47-0.49v**	0.486	Pin 11 to Pin 12	0.488	√
4	**0.47-0.49v**	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.0	√	-24.0	√	-24.2	√	-24.0	√
-7v	-17.0	√	-16.9	√	-17.0	√	-16.9	√
-5v	-12.0	√	-12.0	√	-12.1	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.8	√	17.0	√	16.9	√
10v	24.0	√	24.0	√	24.1	√	24.0	√

Unit……T_TOP7P……Serial No ……
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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-133dB	-113dB	260Hz
Channel 2	Channel 1	-129dB	-110dB	759Hz
Channel 2	Channel 3	-127dB	-115dB	331Hz
Channel 3	Channel 2	-138dB	-112dB	1kHz
Channel 3	Channel 4	-130dB	-114dB	871Hz
Channel 4	Channel 3	-136dB	-109dB	417Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP7P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

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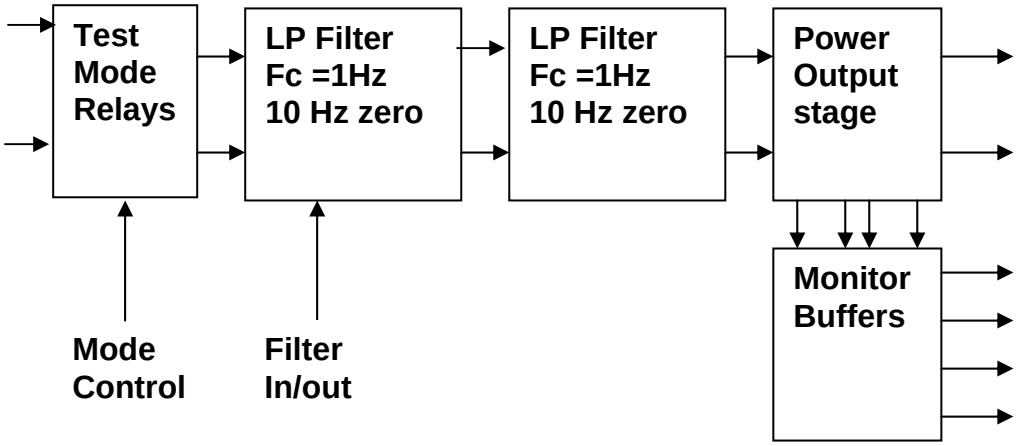

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2. Test equipment

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Workmanship

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J2

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2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

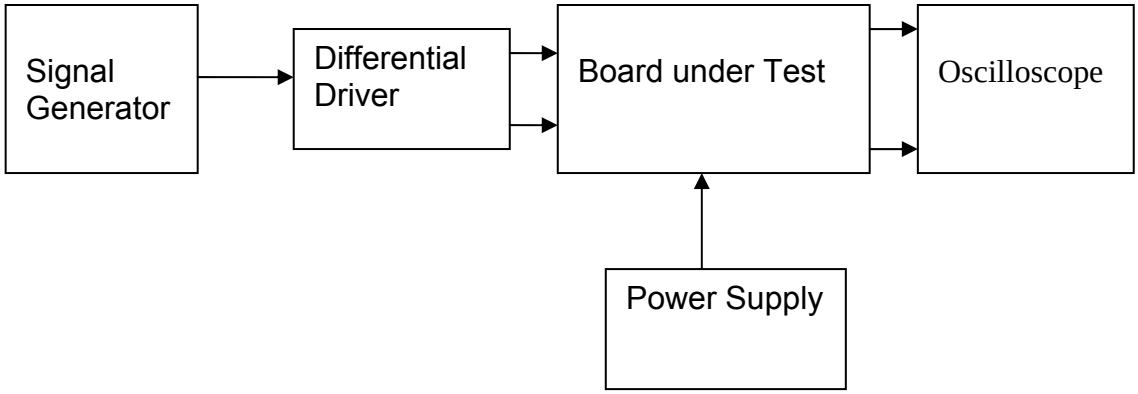
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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J3 pins 6, 7, 8, 9 = negative input
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Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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Test Engineer ….Xen……
Date …….23/10/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.08	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-14.96	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP8P……Serial No ……
Test Engineer ….Xen…….
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP8P……Serial No ……
Test Engineer ….Xen……..
Date …….23/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.64	**0.48 to 0.75v**	√
Ch2	0.65	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP8P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP8P……Serial No ……
Test Engineer ….Xen……
Date …….23/10/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.487	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.489	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP8P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.1	√	-24.1	√	-24.1	√
-7v	-17.0	√	-16.9	√	-17.0	√	-16.9	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	17.0	√	16.9	√	16.9	√
10v	24.0	√	24.1	√	24.1	√	24.1	√

Unit……T_TOP8P……Serial No ……
Test Engineer ….Xen…….
Date …….28/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-132dB	-113dB	1kHz
Channel 2	Channel 1	-130dB	-112dB	275Hz
Channel 2	Channel 3	-129dB	-112dB	724Hz
Channel 3	Channel 2	-135dB	-109dB	229Hz
Channel 3	Channel 4	-137dB	-111dB	575Hz
Channel 4	Channel 3	-143dB	-107dB	219Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

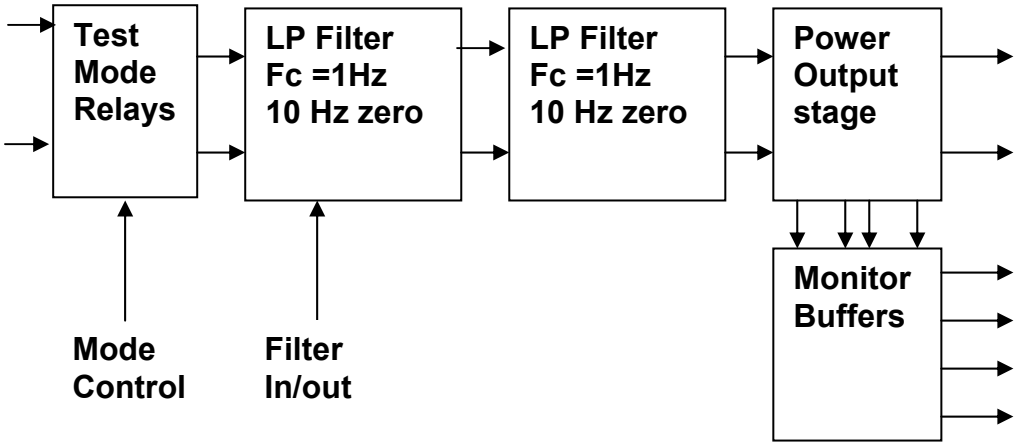
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP9P……Serial No ……
Test Engineer ….Xen……
Date …….23/10/09…..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP9P……Serial No ……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP9P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

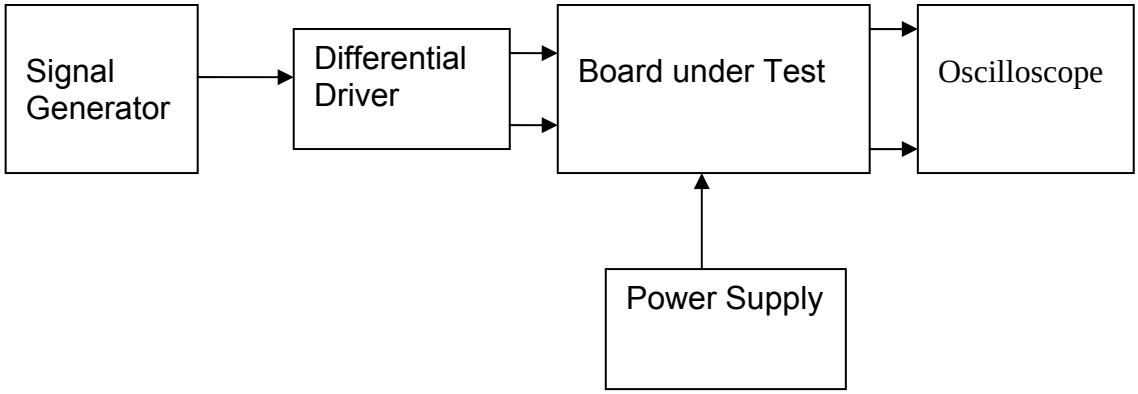
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP9P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.98	1mV	√
+15v TP4	14.99	1mV	√
-15v TP6	-15.04	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP9P……Serial No ……
Test Engineer ……Xen…….
Date ……..23/10/09…….

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP9P……Serial No ……
Test Engineer ….Xen……..
Date …….23/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.65	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.65	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP9P……Serial No ……
Test Engineer ….Xen……..
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.1	3v to 3.4v	√
Ch2	3.1	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.1	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.44	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP9P……Serial No ……
Test Engineer ….Xen……
Date …….23/10/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP9P……Serial No ……
Test Engineer ….Xen…….
Date …….23/10/09……..

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.1	√	-24.0	√	-24.1	√
-7v	-17.0	√	-17.0	√	-17.0	√	-16.9	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	16.9	√	16.9	√
10v	24.0	√	24.0	√	24.0	√	24.0	√

Unit……T_TOP9P……Serial No ……
Test Engineer ….Xen…….
Date …….28/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-133dB	-106dB	871Hz
Channel 2	Channel 1	-129dB	-108dB	832Hz
Channel 2	Channel 3	-132dB	-107dB	832Hz
Channel 3	Channel 2	-130dB	-107dB	479Hz
Channel 3	Channel 4	-129dB	-110dB	479Hz
Channel 4	Channel 3	-129dB	-111dB	484Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP9P……Serial No ……
Test Engineer ….Xen……..
Date …….23/10/09……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

Unit……T_TOP9P……Serial No ……
Test Engineer ….RMC……..
Date ……./3/10……..

FINAL NOISE MEASUREMENTS

Measure the noise output and noise monitor outputs of the completed unit. The extra screening provided by the enclosure protects the unit against extraneous noise, so the results will be more consistent.

If a channel exceeds the limits, replace the noisy ICs, note the work done. Re-measure and record the final result.

Output Noise

Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz (dB)	-60dB =	Measured in nV/√Hz	OK (+/-1dB) ?
Ch1	**-160dB**	-100.174 dB	-160.174 dB	6.77 nV/√Hz	OK
Ch2	**-160dB**	-101.64 dB	-161.64 dB	5.72 nV/√Hz	OK
Ch3	**-160dB**	-101.66 dB	-161.66 dB	5.7 nV/√Hz	OK
Ch4	**-160dB**	-100.94 dB	-160.94 dB	6.2 nV/√Hz	OK

Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in µV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	Output	/(Pre-amplifier gain)	Maximum value	Pass/Fail
1	22.4	2.24	**2.9 µV/√Hz**	OK
2	11.6	1.16	**2.9 µV/√Hz**	OK
3	16	1.6	**2.9 µV/√Hz**	OK
4	143	1.43	**2.9 µV/√Hz**	OK

Repair work (if any)

Monitors
Ch1 IC6 changed
Ch3 IC6 changed
Drive
Ch2 IC4, IC8 changed

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

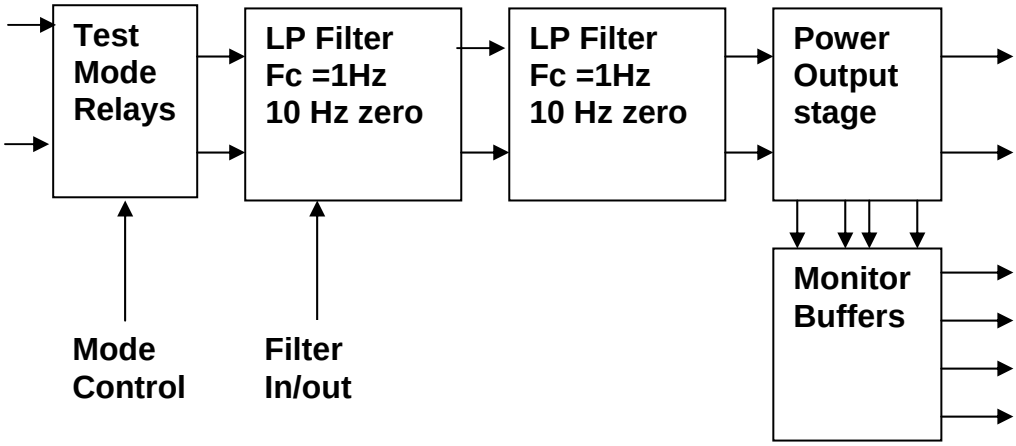
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP10P……Serial No ……
Test Engineer …..Xen……
Date ……..26/10/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP10P……Serial No ……
Test Engineer ….Xen……..
Date …….26/10/09……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

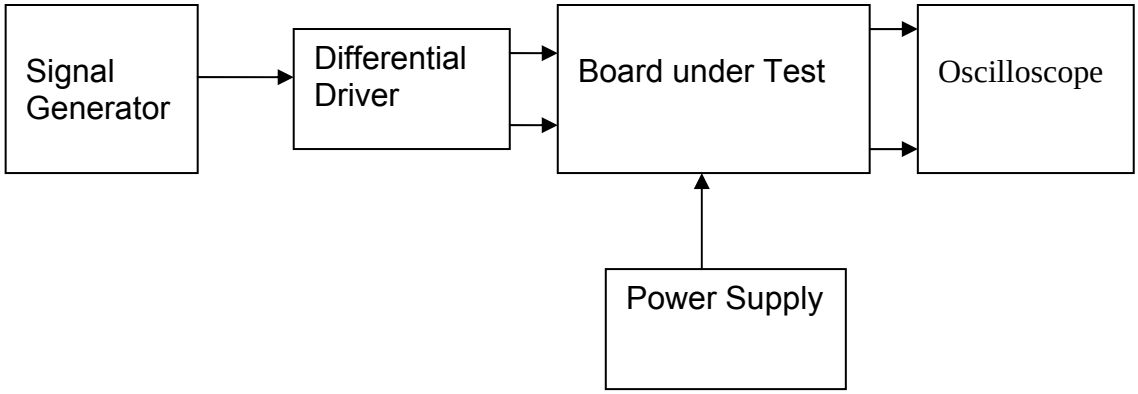
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP10P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.07	1mV	√
+15v TP4	14.98	1mV	√
-15v TP6	-15.00	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.35	**3.3v to 3.7v**	√
Ch3	3.35	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.15	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP10P……Serial No ……
Test Engineer ….Xen……
Date ……26/20/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.484	Pin 3 to Pin 4	0.485	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.486	√
3	0.47-0.49v	0.484	Pin 11 to Pin 12	0.486	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.487	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.1	√	-24.0	√	-24.0	√
-7v	-17.0	√	-16.9	√	-16.9	√	-16.9	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.8	√	16.8	√	16.8	√
10v	24.0	√	24.0	√	24.0	√	24.0	√

Unit……T_TOP10P……Serial No ……
Test Engineer ….Xen…….
Date …….28/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-139dB	-110dB	437Hz
Channel 2	Channel 1	-134dB	-110dB	575Hz
Channel 2	Channel 3	-133dB	-109dB	479Hz
Channel 3	Channel 2	-128dB	-108dB	479Hz
Channel 3	Channel 4	-128dB	-107dB	724Hz
Channel 4	Channel 3	-130dB	-110dB	832Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP10P……Serial No ……
Test Engineer ….Xen……..
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.42	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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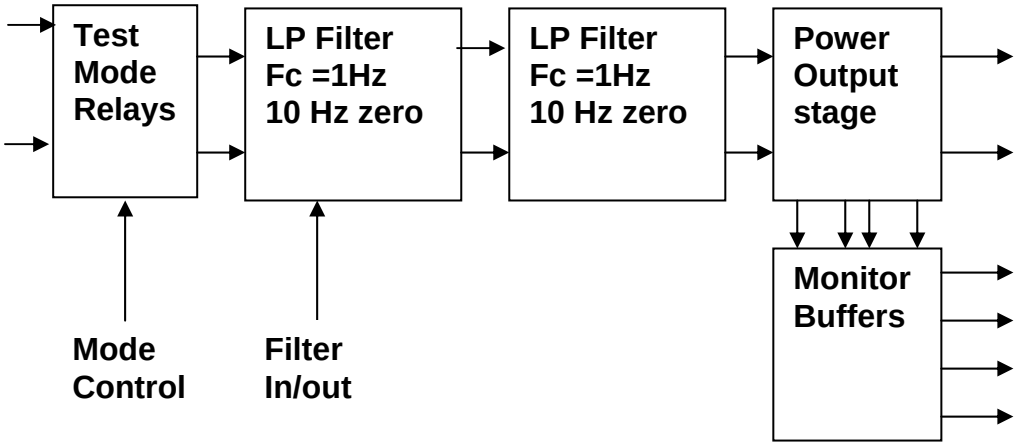
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP11P……Serial No ……
Test Engineer .Xen…..……
Date ……..26/10/09..……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen……..
Date …….26/10/09……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen…….
Date …….26/10/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen……
Date …….26/10/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

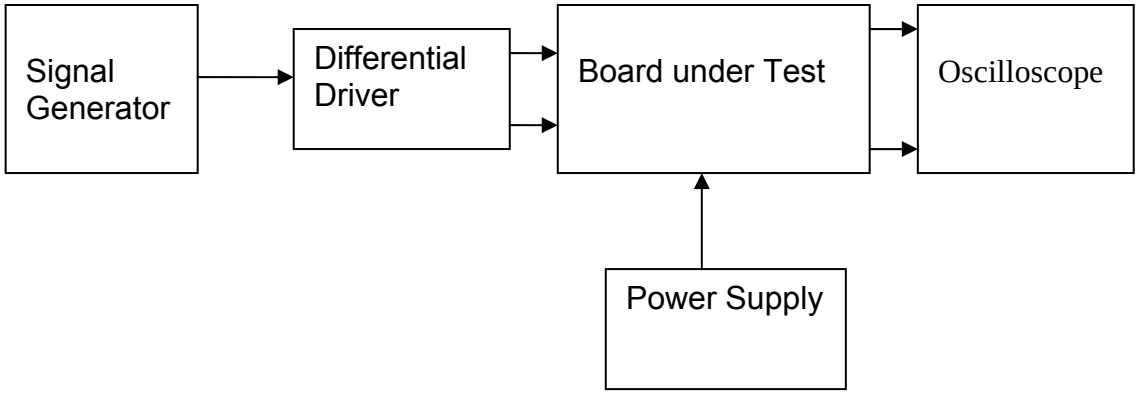
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen……
Date …….26/10/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.09	1mV	√
+15v TP4	14.94	1mV	√
-15v TP6	-15.08	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen…….
Date ……..26/10/09..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen……..
Date ……..26/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.64	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen……..
Date …….26/10/09……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.15	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.1	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.45	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen……
Date …….26/10/09…..……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen…….
Date …….26/10/09……..

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.2	√	-24.1	√	-24.2	√
-7v	-17.0	√	-17.0	√	-16.9	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	16.9	√	17.0	√
10v	24.1	√	24.2	√	24.0	√	24.1	√

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen…….
Date …….28/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-126dB	-108dB	724Hz
Channel 2	Channel 1	-132dB	-110dB	525Hz
Channel 2	Channel 3	-133dB	-109dB	871Hz
Channel 3	Channel 2	-113dB	-110dB	363Hz
Channel 3	Channel 4	-139dB	-109dB	437Hz
Channel 4	Channel 3	-142dB	-110dB	437Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP11P……Serial No ……
Test Engineer ….Xen……..
Date …….26/10/09……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

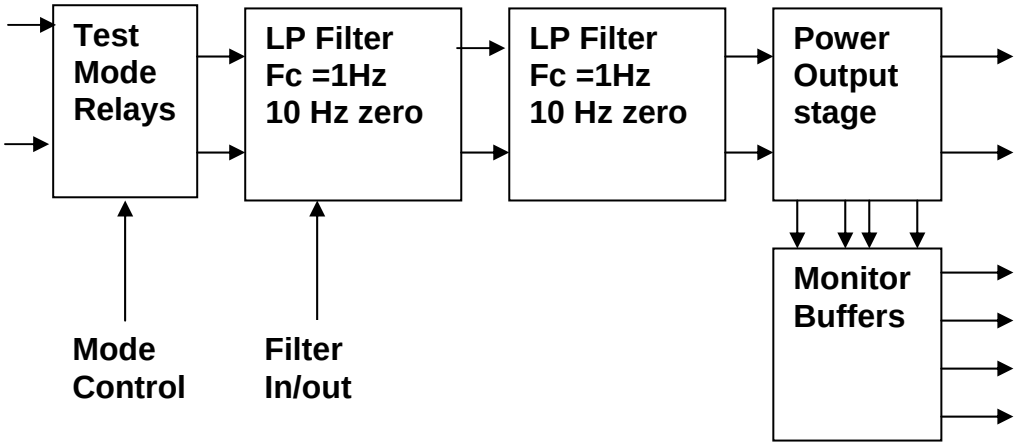
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP12P……Serial No ……
Test Engineer ….Xen……
Date …….26/10/09…..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP12P……Serial No ……
Test Engineer ….Xen……..
Date …….26/10/09……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP12P……Serial No ……
Test Engineer ….Xen…….
Date …….26/10/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP12P……Serial No ……
Test Engineer ….Xen……
Date …….26/10/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

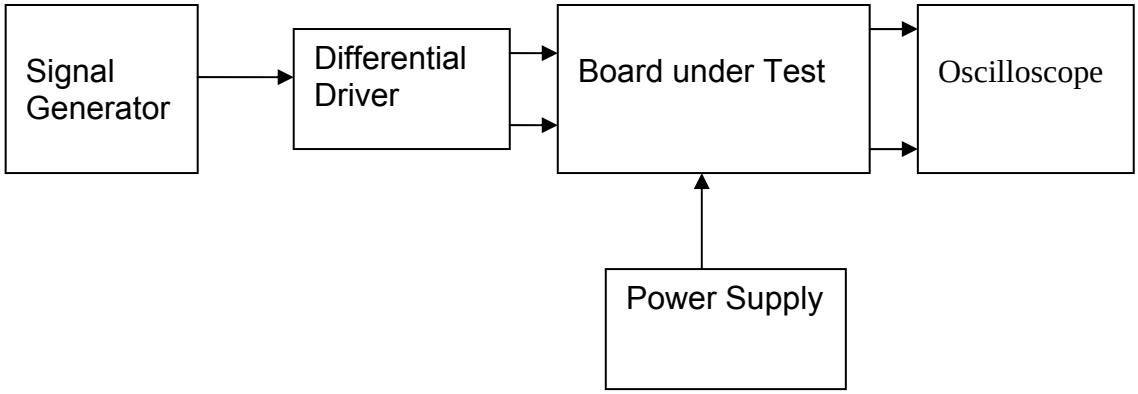
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP12P……Serial No ……
Test Engineer ….Xen……
Date …….26/10/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.01	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-14.96	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP12P……Serial No ……
Test Engineer ….Xen…….
Date …….26/10/09…..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP12P……Serial No ……
Test Engineer ….Xen……..
Date …….26/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.15	3v to 3.4v	√
Ch3	3.1	3v to 3.4v	√
Ch4	3.15	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.45	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**1.15-1.25v**	1.22	Pin 1 to Pin 2	1.22	√
2	**1.15-1.25v**	1.22	Pin 5 to Pin 6	1.22	√
3	**1.15-1.25v**	1.22	Pin 9 to Pin 10	1.22	√
4	**1.15-1.25v**	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**0.47-0.49v**	0.484	Pin 3 to Pin 4	0.486	√
2	**0.47-0.49v**	0.486	Pin 7 to Pin 8	0.487	√
3	**0.47-0.49v**	0.485	Pin 11 to Pin 12	0.488	√
4	**0.47-0.49v**	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.2	√	-24.1	√	-24.0	√
-7v	-17.0	√	-16.9	√	-16.9	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	11.9	√	12.0	√
7v	16.8	√	16.9	√	16.8	√	17.0	√
10v	24.0	√	24.1	√	24.0	√	24.1	√

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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-133dB	-111dB	437Hz
Channel 2	Channel 1	-127dB	-109dB	871Hz
Channel 2	Channel 3	-132dB	-112dB	550Hz
Channel 3	Channel 2	-142dB	-112dB	363Hz
Channel 3	Channel 4	-136dB	-108dB	871Hz
Channel 4	Channel 3	-130dB	-108dB	525Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.42	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

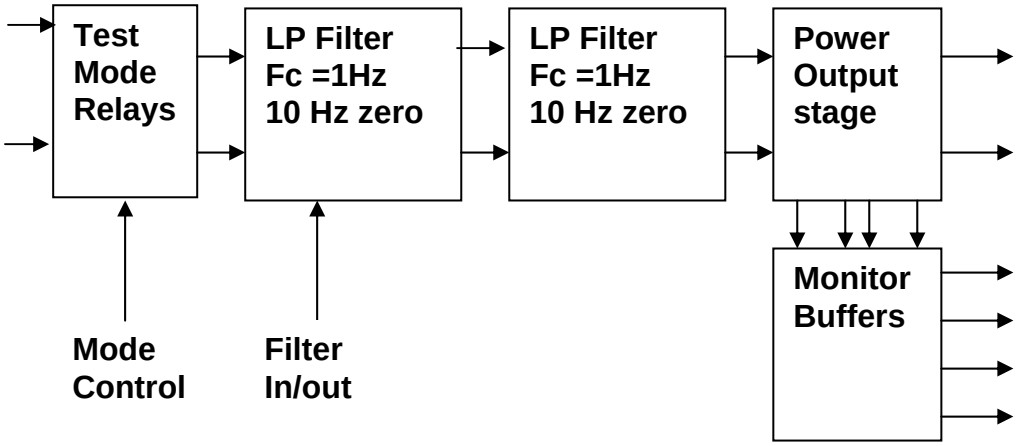
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP13P……Serial No ……
Test Engineer …..Xen……
Date ……..27/10/09……..

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

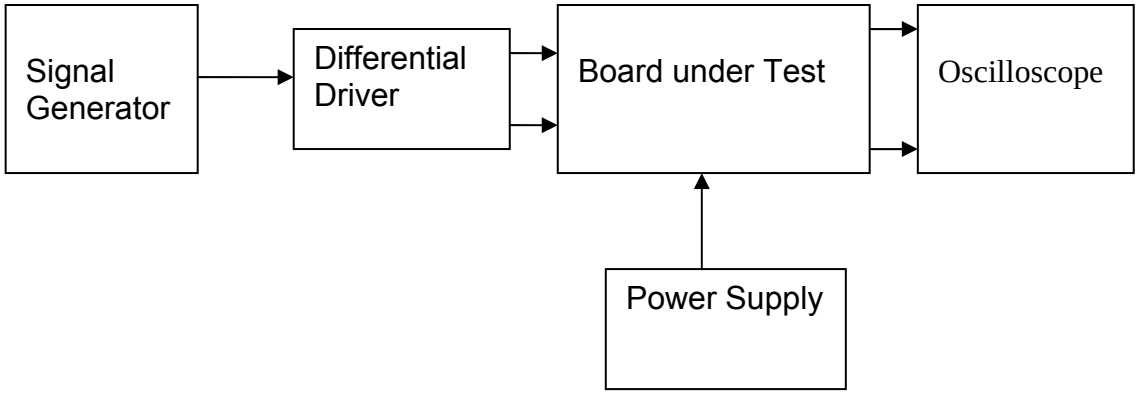
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.99	1mV	√
+15v TP4	14.92	1mV	√
-15v TP6	-15.02	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP13P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.64	**0.48 to 0.75v**	√
Ch2	0.64	**0.48 to 0.75v**	√
Ch3	0.64	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.1	3v to 3.4v	√
Ch2	3.1	3v to 3.4v	√
Ch3	3.1	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.45	0.4v to 0.5v	√
Ch2	0.45	0.4v to 0.5v	√
Ch3	0.45	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP13P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.487	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.1	√	-24.2	√	-24.2	√
-7v	-17.0	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.8	√	17.0	√	16.9	√
10v	24.0	√	24.0	√	24.1	√	24.0	√

Unit……T_TOP13P……Serial No ……
Test Engineer ….Xen…….
Date …….29/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-140dB	-109dB	759Hz
Channel 2	Channel 1	-122dB	-108dB	479Hz
Channel 2	Channel 3	-121dB	-109dB	661Hz
Channel 3	Channel 2	-126dB	-109dB	437Hz
Channel 3	Channel 4	-124dB	-107dB	955Hz
Channel 4	Channel 3	-132dB	-109dB	944Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP13P……Serial No ……
Test Engineer ….Xen……..
Date …….27/10/09……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

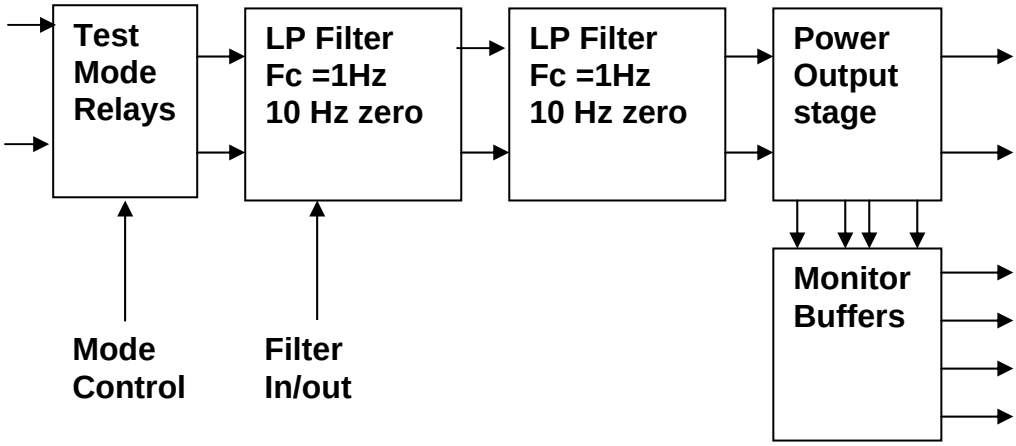
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP14P……Serial No ……
Test Engineer ….Xen……
Date …….27/10/09…..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP14P……Serial No ……
Test Engineer ….Xen……..
Date …….27/10/09……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP14P……Serial No ……
Test Engineer ….Xen…….
Date …….27/10/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP14P……Serial No ……
Test Engineer ….Xen……
Date …….27/10/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

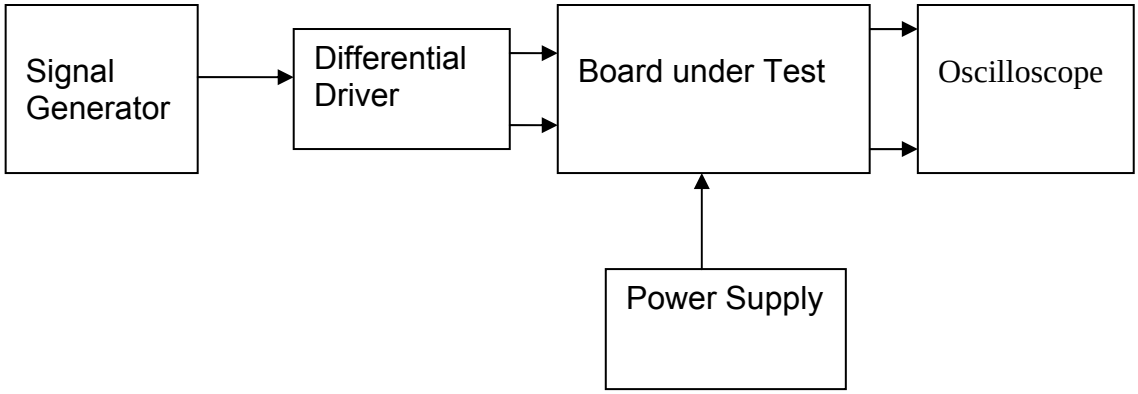
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP14P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.06	1mV	√
+15v TP4	14.95	1mV	√
-15v TP6	-15.03	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP14P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP14P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP14P……Serial No ……
Test Engineer ….Xen……..
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.1	3v to 3.4v	√
Ch2	3.1	3v to 3.4v	√
Ch3	3.1	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.489	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.2	√	-24.0	√	-24.2	√
-7v	-17.0	√	-17.0	√	-16.9	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	16.9	√	16.9	√
10v	24.0	√	24.0	√	24.0	√	24.0	√

Unit……T_TOP14P……Serial No ……
Test Engineer ….Xen…….
Date …….29/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-127dB	-111dB	263Hz
Channel 2	Channel 1	-120dB	-111dB	832Hz
Channel 2	Channel 3	-118dB	-108dB	661Hz
Channel 3	Channel 2	-123dB	-111dB	550Hz
Channel 3	Channel 4	-124dB	-109dB	832Hz
Channel 4	Channel 3	-120dB	-107dB	347Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP14P……Serial No ……
Test Engineer ….Xen……..
Date …….27/10/09……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

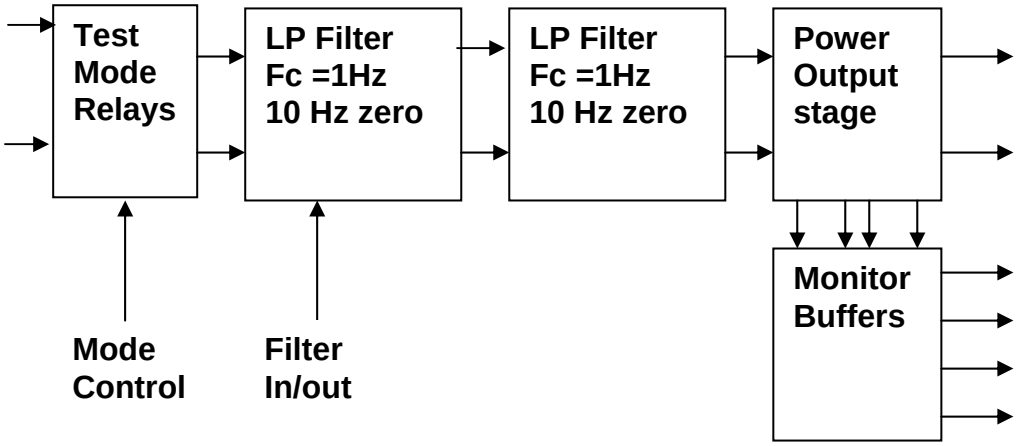
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen……
Date …….27/10/09…..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

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This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen……..
Date …….27/10/09……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen…….
Date …….27/10/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen……
Date …….27/10/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

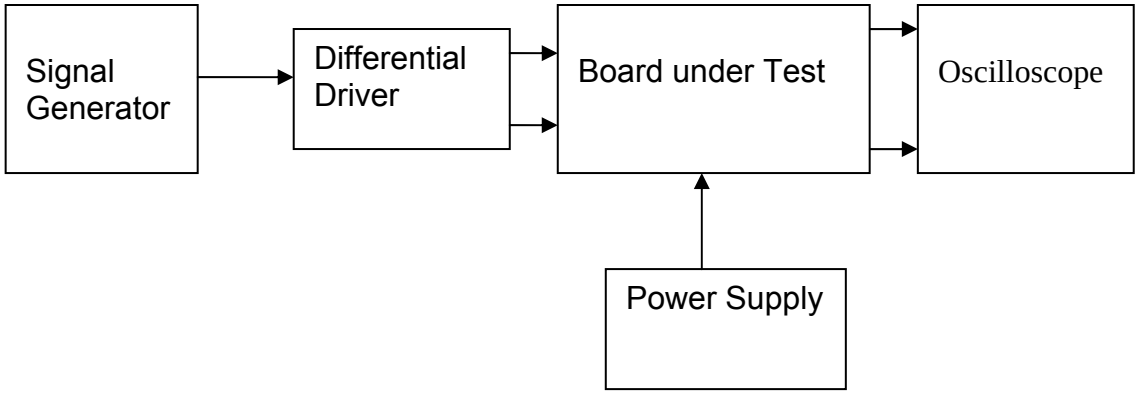
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen……
Date …….27/10/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.10	1mV	√
+15v TP4	14.78	1mV	√
-15v TP6	-14.95	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen…….
Date …….27/10/09…..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen……..
Date …….27/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.65	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen……..
Date …….27/10/09…..……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen……
Date …….27/10/09…..……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**1.15-1.25v**	1.22	Pin 1 to Pin 2	1.22	√
2	**1.15-1.25v**	1.22	Pin 5 to Pin 6	1.22	√
3	**1.15-1.25v**	1.22	Pin 9 to Pin 10	1.22	√
4	**1.15-1.25v**	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**0.47-0.49v**	0.484	Pin 3 to Pin 4	0.486	√
2	**0.47-0.49v**	0.486	Pin 7 to Pin 8	0.487	√
3	**0.47-0.49v**	0.485	Pin 11 to Pin 12	0.486	√
4	**0.47-0.49v**	0.486	Pin 15 to Pin 16	0.489	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen…….
Date …….27/10/09……..

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.2	√	-24.2	√	-24.1	√
-7v	-17.0	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	16.9	√	16.9	√
10v	24.0	√	24.0	√	24.0	√	24.1	√

Unit……T_TOP15P……Serial No ……
Test Engineer ….Xen…….
Date …….29/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-134dB	-110dB	229Hz
Channel 2	Channel 1	-127dB	-114dB	417Hz
Channel 2	Channel 3	-127dB	-112dB	575Hz
Channel 3	Channel 2	-129dB	-112dB	275Hz
Channel 3	Channel 4	-133dB	-111dB	575Hz
Channel 4	Channel 3	-140dB	-111dB	933Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP15P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

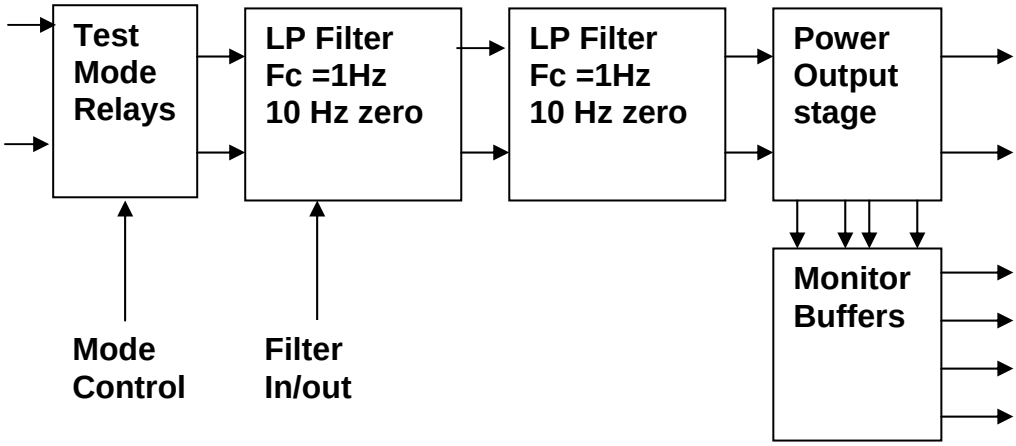
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP16P……Serial No ……
Test Engineer ….Xen……
Date …….28/10/09…..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP16P……Serial No ……
Test Engineer ….Xen……..
Date …….28/10/09……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP16P……Serial No ……
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Date …….28/10/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP16P……Serial No ……
Test Engineer ….Xen……
Date …….28/10/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

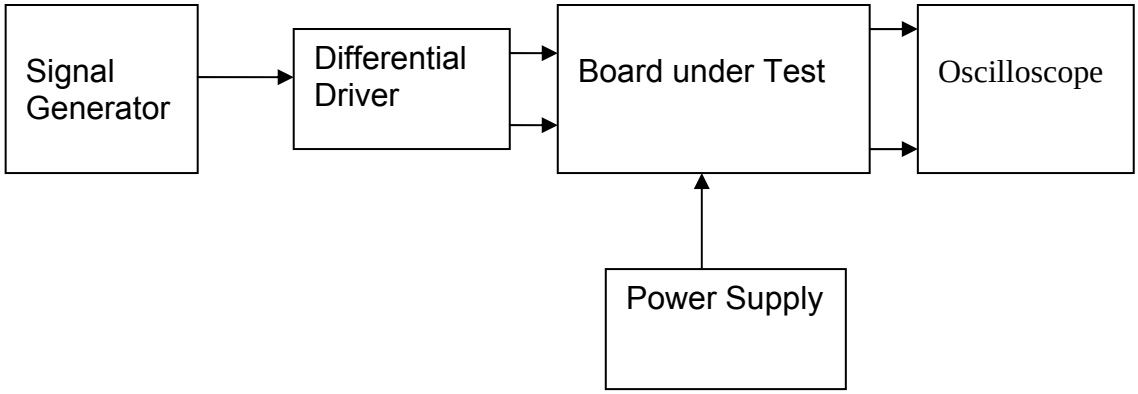
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP16P……Serial No ……
Test Engineer ….Xen……
Date …….28/10/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.08	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-15.06	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP16P……Serial No ……
Test Engineer ….Xen…….
Date …….28/10/09…..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP16P……Serial No ……
Test Engineer ….Xen……..
Date …….28/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.65	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.65	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP16P……Serial No ……
Test Engineer ….Xen……..
Date …….28/10/09…..……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.1	3v to 3.4v	√
Ch2	3.1	3v to 3.4v	√
Ch3	3.1	3v to 3.4v	√
Ch4	3.1	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.44	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**1.15-1.25v**	1.22	Pin 1 to Pin 2	1.22	√
2	**1.15-1.25v**	1.22	Pin 5 to Pin 6	1.22	√
3	**1.15-1.25v**	1.22	Pin 9 to Pin 10	1.22	√
4	**1.15-1.25v**	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**0.47-0.49v**	0.485	Pin 3 to Pin 4	0.487	√
2	**0.47-0.49v**	0.487	Pin 7 to Pin 8	0.488	√
3	**0.47-0.49v**	0.485	Pin 11 to Pin 12	0.487	√
4	**0.47-0.49v**	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.1	√	-24.2	√	-24.2	√
-7v	-17.0	√	-17.0	√	-16.9	√	-16.9	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	-12.0	√	12.0	√
7v	17.0	√	16.9	√	16.9	√	16.9	√
10v	24.1	√	24.0	√	24.1	√	24.1	√

Unit……T_TOP16P……Serial No ……
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Date …….29/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-143dB	-111dB	832Hz
Channel 2	Channel 1	-125dB	-109dB	437Hz
Channel 2	Channel 3	-129dB	-110dB	437Hz
Channel 3	Channel 2	-130dB	-111dB	140Hz
Channel 3	Channel 4	-136dB	-110dB	724Hz
Channel 4	Channel 3	-135dB	-110dB	832Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP16P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

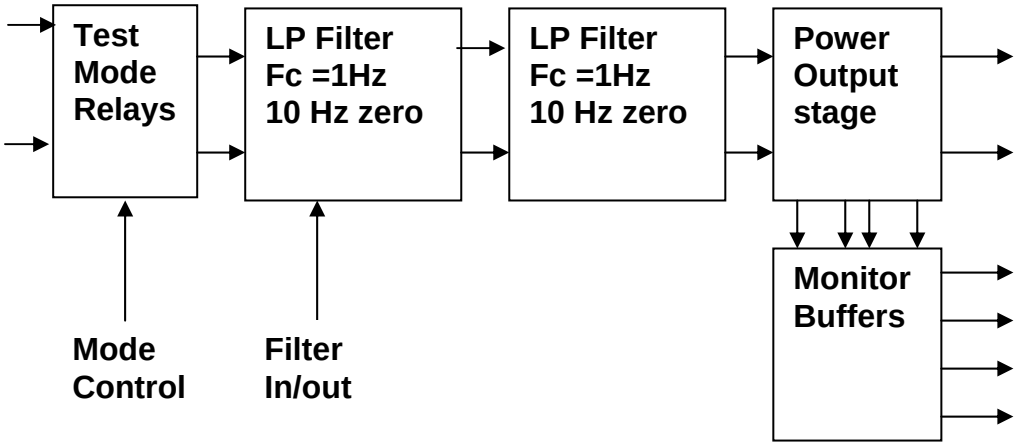
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP17P……Serial No ……
Test Engineer ….Xen……
Date …….28/10/09…..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

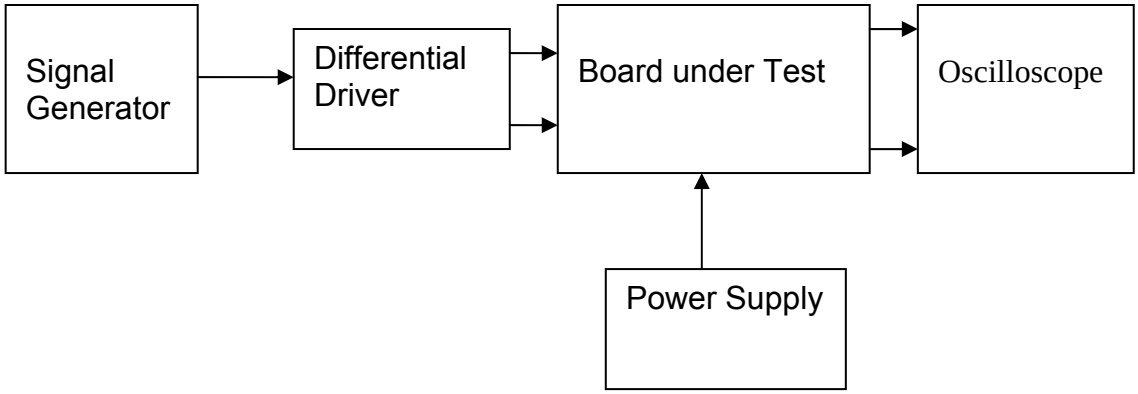
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.09	1mV	√
+15v TP4	14.92	1mV	√
-15v TP6	-14.93	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.65	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.15	3v to 3.4v	√
Ch4	3.1	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.45	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.487	Pin 7 to Pin 8	0.488	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.1	√	-24.1	√	-24.1	√
-7v	-17.0	√	-16.9	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	16.9	√	16.9	√
10v	24.1	√	24.0	√	24.1	√	24.0	√

Unit……T_TOP17P……Serial No ……
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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-133dB	-109dB	331Hz
Channel 2	Channel 1	-123dB	-108dB	479Hz
Channel 2	Channel 3	-114dB	-102dB	479Hz
Channel 3	Channel 2	-123dB	-107dB	229Hz
Channel 3	Channel 4	-125dB	-108dB	724Hz
Channel 4	Channel 3	-134dB	-107dB	437Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

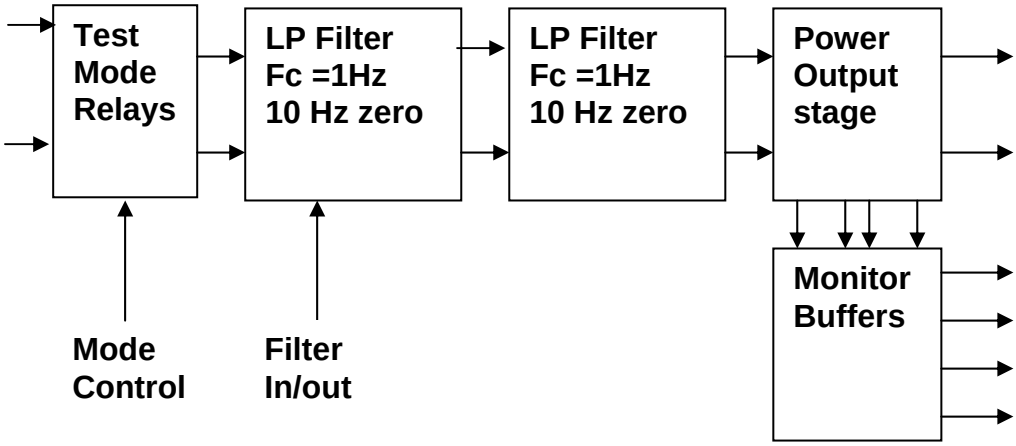
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP18P……Serial No ……
Test Engineer ….Xen……
Date …….28/10/09…..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP18P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP18P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

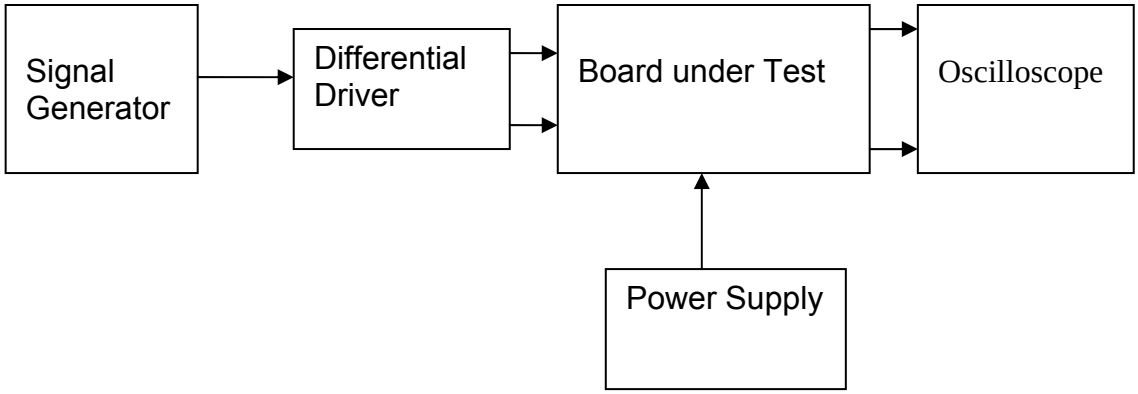
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP18P……Serial No ……
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Date …….28/10/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.12	1mV	√
+15v TP4	14.91	1mV	√
-15v TP6	-14.97	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP18P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP18P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.35	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.488	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.490	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.2	√	-24.2	√	-24.2	√
-7v	-17.0	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.2	√	12.0	√
7v	16.9	√	17.0	√	17.0	√	16.9	√
10v	24.0	√	24.2	√	24.2	√	24.0	√

Unit……T_TOP18P……Serial No ……
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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-132dB	-110dB	479Hz
Channel 2	Channel 1	-127dB	-112dB	479Hz
Channel 2	Channel 3	-119dB	-111dB	759Hz
Channel 3	Channel 2	-116dB	-112dB	525Hz
Channel 3	Channel 4	-117dB	-110dB	479Hz
Channel 4	Channel 3	-121dB	-110dB	437Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.42	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
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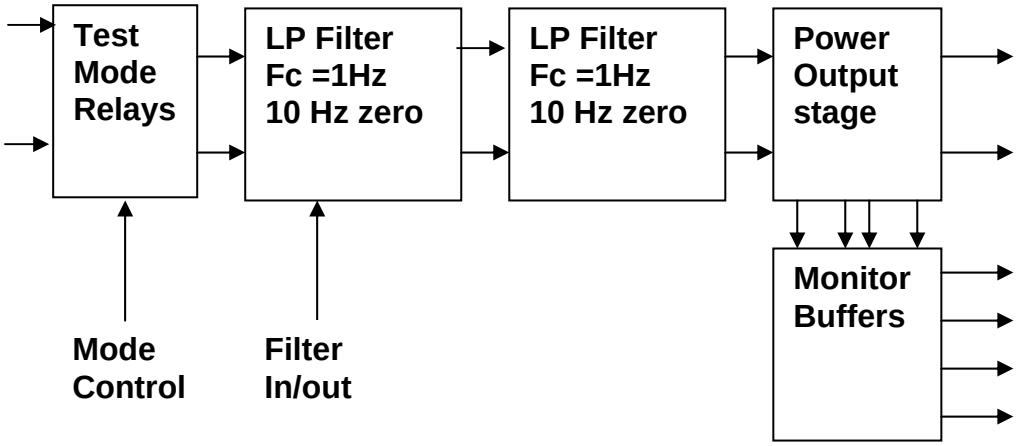

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J2

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2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

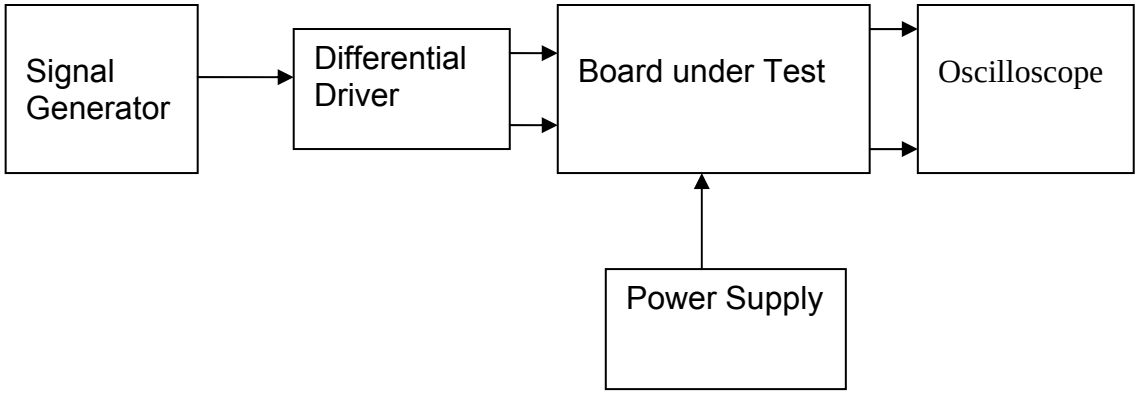
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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Check the polarity of the wiring:
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Set the power supply outputs to zero.
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If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.97	1mV	√
+15v TP4	14.91	1mV	√
-15v TP6	-14.96	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP19P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	4.7v to 5v	√
Ch2	4.75	4.9	4.9	4.7v to 5v	√
Ch3	4.8	4.9	4.9	4.7v to 5v	√
Ch4	4.75	4.9	4.9	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7 to 5v	√
Ch2	4.8	4.7 to 5v	√
Ch3	4.8	4.7 to 5v	√
Ch4	4.8	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3.3v to 3.7v	√
Ch2	3.3	3.3v to 3.7v	√
Ch3	3.3	3.3v to 3.7v	√
Ch4	3.3	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	0.48 to 0.75v	√
Ch2	0.66	0.48 to 0.75v	√
Ch3	0.66	0.48 to 0.75v	√
Ch4	0.65	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

Unit……T_TOP19P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.1	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.1	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP19P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**1.15-1.25v**	1.22	Pin 1 to Pin 2	1.22	√
2	**1.15-1.25v**	1.22	Pin 5 to Pin 6	1.22	√
3	**1.15-1.25v**	1.22	Pin 9 to Pin 10	1.22	√
4	**1.15-1.25v**	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**0.47-0.49v**	0.485	Pin 3 to Pin 4	0.487	√
2	**0.47-0.49v**	0.488	Pin 7 to Pin 8	0.489	√
3	**0.47-0.49v**	0.485	Pin 11 to Pin 12	0.486	√
4	**0.47-0.49v**	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.1	√	-24.2	√	-24.1	√
-7v	-17.0	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	17.0	√	16.9	√
10v	24.0	√	24.0	√	24.0	√	24.0	√

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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-135dB	-113dB	347Hz
Channel 2	Channel 1	-126dB	-108dB	479Hz
Channel 2	Channel 3	-131dB	-108dB	437Hz
Channel 3	Channel 2	-137dB	-106dB	437Hz
Channel 3	Channel 4	-131dB	-110dB	437Hz
Channel 4	Channel 3	-142dB	-107dB	479Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

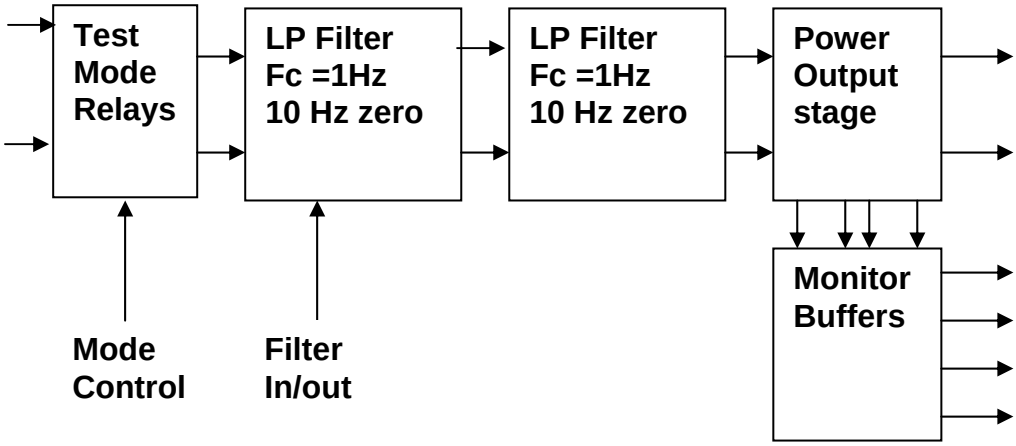
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP20P……Serial No ……
Test Engineer…..Xen……
Date……..30/10/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

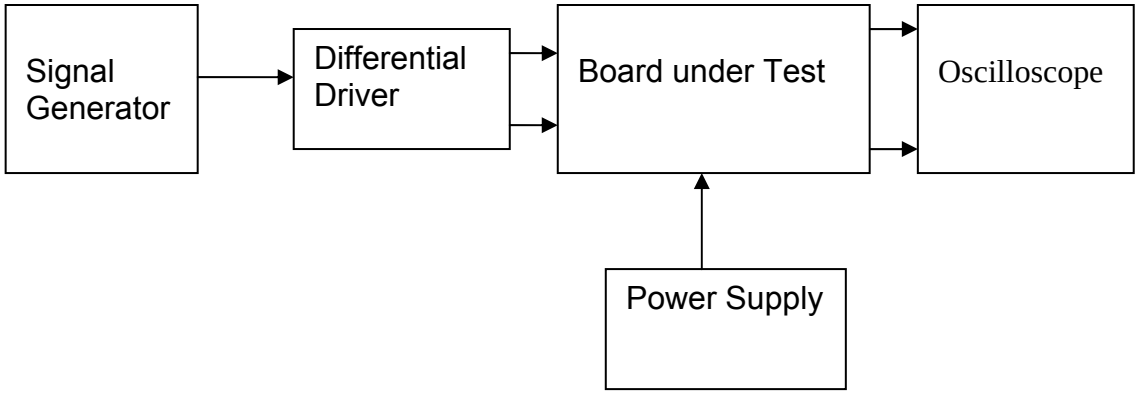
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.94	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-14.98	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP20P……Serial No ……
Test Engineer ….Xen……..
Date …….30/10/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.1	3v to 3.4v	√
Ch3	3.15	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.45	0.4v to 0.5v	√
Ch2	0.45	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP20P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.484	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.485	Pin 7 to Pin 8	0.486	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP20P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.1	√	-24.1	√	-24.1	√
-7v	-17.0	√	-16.9	√	-17.0	√	-16.9	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	16.9	√	16.9	√
10v	24.0	√	24.0	√	24.0	√	24.1	√

Unit……T_TOP20P……Serial No ……
Test Engineer ….Xen…….
Date …….30/10/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-141dB	-112dB	479Hz
Channel 2	Channel 1	-133dB	-115dB	331Hz
Channel 2	Channel 3	-133dB	-111dB	437Hz
Channel 3	Channel 2	-129dB	-111dB	575Hz
Channel 3	Channel 4	-138dB	-111dB	240Hz
Channel 4	Channel 3	-139dB	-112dB	479Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP20P……Serial No ……
Test Engineer ….Xen……..
Date …….30/10/09……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.43	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

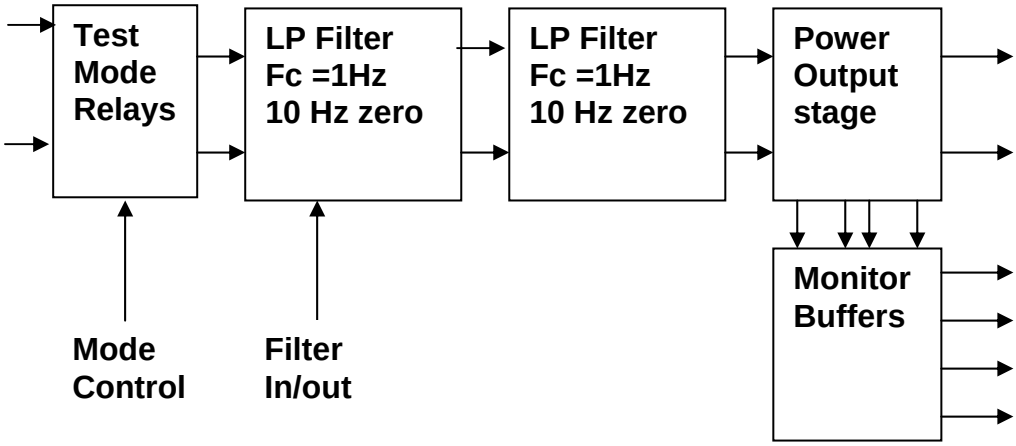
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP21P……Serial No ……
Test Engineer…..Xen……
Date……..30/10/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP21P……Serial No ……
Test Engineer ……Xen……..
Date ……30/10/09……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP21P……Serial No ……
Test Engineer ….Xen…….
Date …….30/10/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP21P……Serial No ……
Test Engineer ….Xen……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

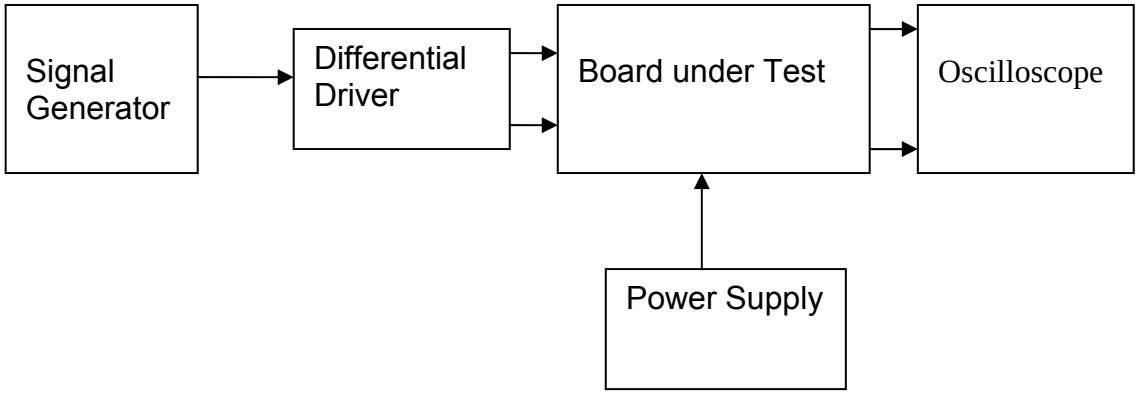
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP21P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.06	1mV	√
+15v TP4	14.94	1mV	√
-15v TP6	-15.02	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP21P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP21P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.15	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.15	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.486	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.0	√	-24.0	√	-24.0	√	-24.1	√
-7v	-17.0	√	-16.9	√	-16.9	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.3	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	17.0	√	17.0	√	17.0	√	16.9	√
10v	24.1	√	24.2	√	24.1	√	24.1	√

Unit……T_TOP21P……Serial No ……
Test Engineer ….Xen…….
Date …….2/11/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-118dB	-110dB	860Hz
Channel 2	Channel 1	-135dB	-107dB	525Hz
Channel 2	Channel 3	-139dB	-111dB	631Hz
Channel 3	Channel 2	-133dB	-108dB	479Hz
Channel 3	Channel 4	-127dB	-86dB	347Hz
Channel 4	Channel 3	-135dB	-111dB	479Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP21P……Serial No ……
Test Engineer ….Xen……..
Date …….30/10/09……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.43	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

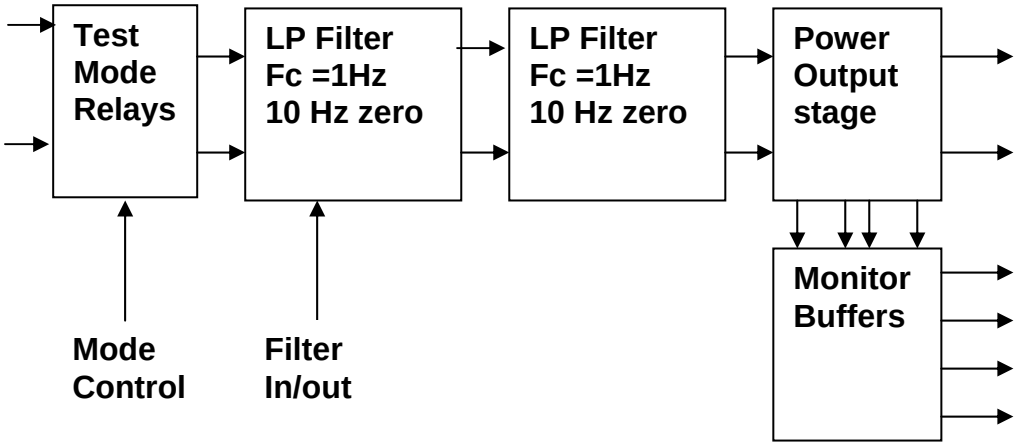
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP22P……Serial No ……
Test Engineer…..Xen……
Date……..2/11/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

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This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP22P……Serial No ……
Test Engineer ….Xen……..
Date …….2/11/09..……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP22P……Serial No ……
Test Engineer ….Xen…….
Date …….2/11/09..…….

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP22P……Serial No ……
Test Engineer ….Xen……
Date …….2/11/09..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

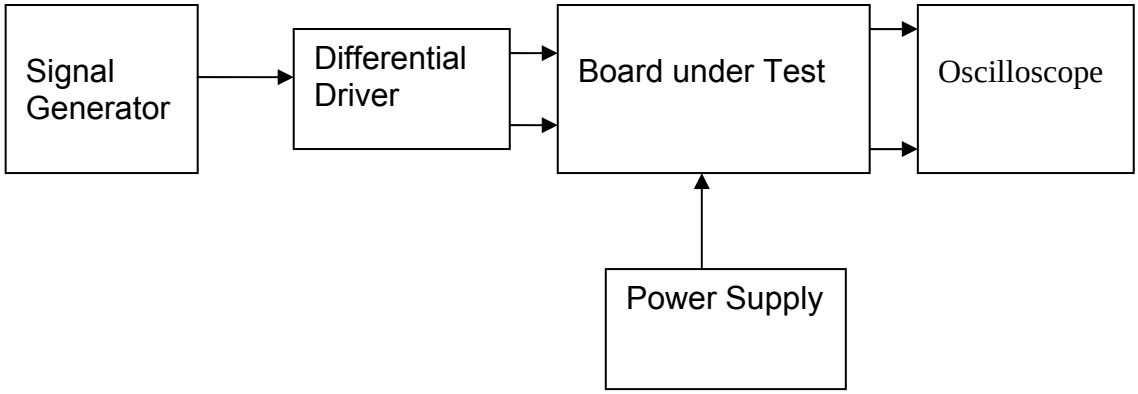
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP22P……Serial No ……
Test Engineer ….Xen……
Date …….2/11/09..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.08	1mV	√
+15v TP4	14.92	1mV	√
-15v TP6	-14.98	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP22P……Serial No ……
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Date …….2/11/09……..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP22P……Serial No ……
Test Engineer ….Xen……..
Date …….2//11/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP22P……Serial No ……
Test Engineer ….Xen……..
Date …….2/11/09……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.15	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.49	0.4v to 0.5v	√
Ch4	0.45	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP22P……Serial No ……
Test Engineer ….Xen……
Date ……2/11/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.487	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP22P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.1	√	-24.1	√	-24.1	√
-7v	-17.0	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	17.0	√	16.9	√	16.9	√	16.9	√
10v	24.1	√	24.1	√	24.0	√	24.1	√

Unit……T_TOP22P……Serial No ……
Test Engineer ….Xen…….
Date …….2/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-142dB	-107dB	1kHz
Channel 2	Channel 1	-126dB	-109dB	955Hz
Channel 2	Channel 3	-121dB	-108dB	692Hz
Channel 3	Channel 2	-124dB	-113dB	631Hz
Channel 3	Channel 4	-127dB	-112dB	462Hz
Channel 4	Channel 3	-130dB	-114dB	331Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP22P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

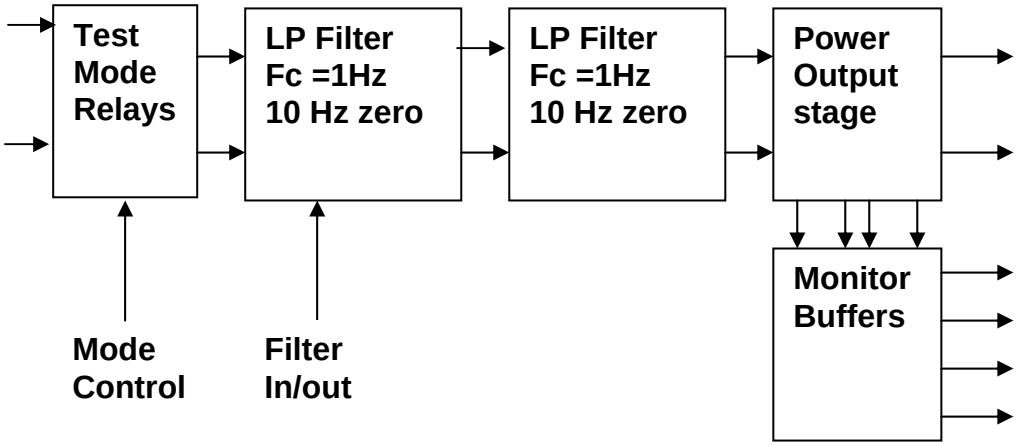
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP23P……Serial No ……
Test Engineer…..Xen……
Date……..2/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP23P……Serial No ……
Test Engineer ….Xen……..
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP23P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP23P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

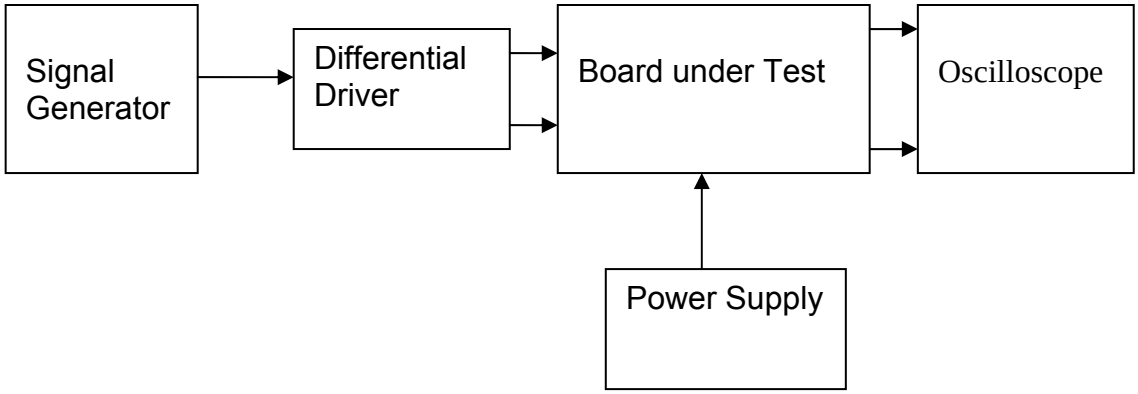
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP23P……Serial No ……
Test Engineer ….Xen……
Date …….2/11/09..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.01	1mV	√
+15v TP4	14.85	1mV	√
-15v TP6	-14.99	1mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP23P……Serial No ……
Test Engineer ….Xen…….
Date …….2/11/09……..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP23P……Serial No ……
Test Engineer ….Xen……..
Date …….2/11/09……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.35	**3.3v to 3.7v**	√
Ch3	3.35	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP23P……Serial No ……
Test Engineer ….Xen……..
Date …….2/11/09……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.15	3v to 3.4v	√
Ch4	3.15	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.45	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.1	√	-24.1	√	-24.1	√
-7v	-17.0	√	-16.9	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	17.0	√	16.9	√	17.0	√	17.0	√
10v	24.1	√	24.0	√	24.1	√	24.1	√

Unit……T_TOP23P……Serial No ……
Test Engineer ….Xen…….
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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-128dB	-113dB	437Hz
Channel 2	Channel 1	-129dB	-111dB	525Hz
Channel 2	Channel 3	-140dB	-112dB	437Hz
Channel 3	Channel 2	-144dB	-115dB	575Hz
Channel 3	Channel 4	-135dB	-113dB	437Hz
Channel 4	Channel 3	-130dB	-111dB	479Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP23P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

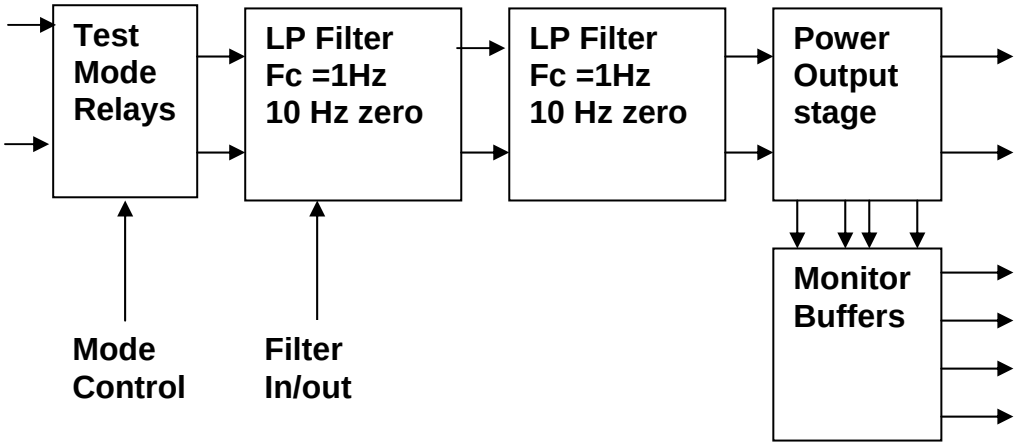
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP24P……Serial No ……
Test Engineer…..Xen……
Date……..3/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

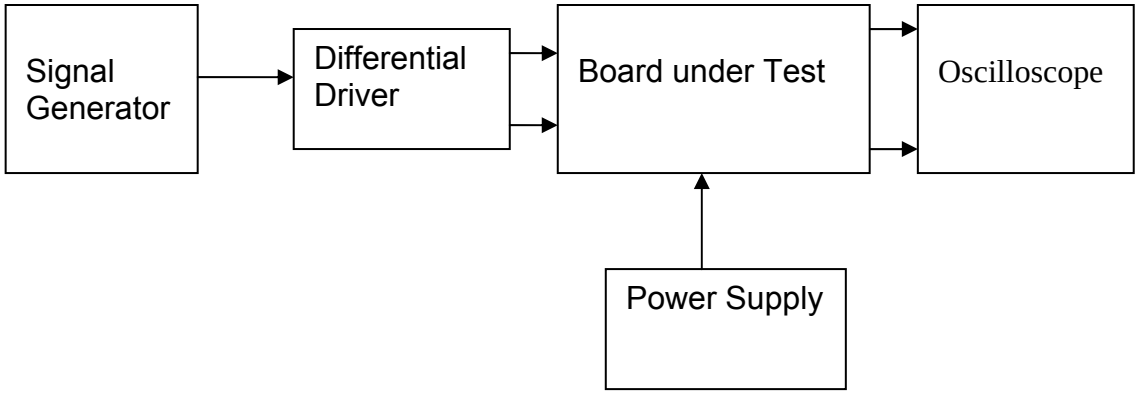
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.04	1mV	√
+15v TP4	14.81	1mV	√
-15v TP6	-14.95	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.1	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.45	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP24P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.486	Pin 3 to Pin 4	0.488	√
2	0.47-0.49v	0.487	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.486	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP24P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.2	√	-24.2	√	-24.2	√
-7v	-17.0	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.1	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	17.0	√	16.8	√	16.8	√	16.8	√
10v	24.1	√	24.0	√	24.0	√	24.0	√

Unit……T_TOP24P……Serial No ……
Test Engineer ….Xen…….
Date …….3/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-137dB	-115dB	871Hz
Channel 2	Channel 1	-137dB	-108dB	479Hz
Channel 2	Channel 3	-122dB	-81dB	145Hz
Channel 3	Channel 2	-96dB	-74dB	422Hz
Channel 3	Channel 4	-111dB	-76dB	575Hz
Channel 4	Channel 3	-102dB	-72dB	178Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP24P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

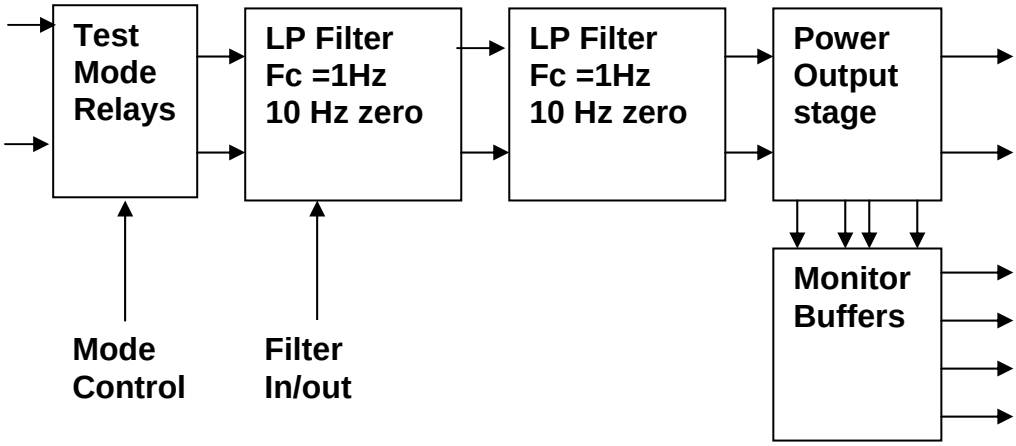
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP25P……Serial No ……
Test Engineer…..Xen……
Date……..3/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP25P……Serial No ……
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Date …….3/11/09..……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP25P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

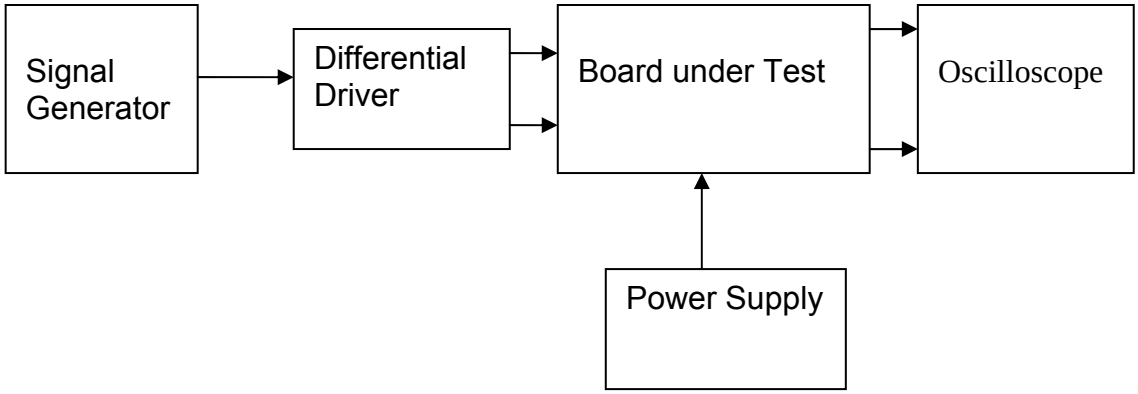
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP25P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.10	1mV	√
+15v TP4	14.89	1mV	√
-15v TP6	-15.04	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP25P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.64	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.1	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.486	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.489	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.1	√	-24.2	√	-24.2	√
-7v	-17.0	√	-16.9	√	-17.0	√	-17.0	√
-5v	-12.1	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	17.0	√	17.0	√	12.0	√
10v	24.1	√	24.1	√	24.2	√	24.1	√

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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-127dB	-110dB	437Hz
Channel 2	Channel 1	-131dB	-110dB	437Hz
Channel 2	Channel 3	-143dB	-111dB	229Hz
Channel 3	Channel 2	-138dB	-110dB	437Hz
Channel 3	Channel 4	-102dB	-69dB	166Hz
Channel 4	Channel 3	-107dB	-70dB	166Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP26P……Serial No ……
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Contents

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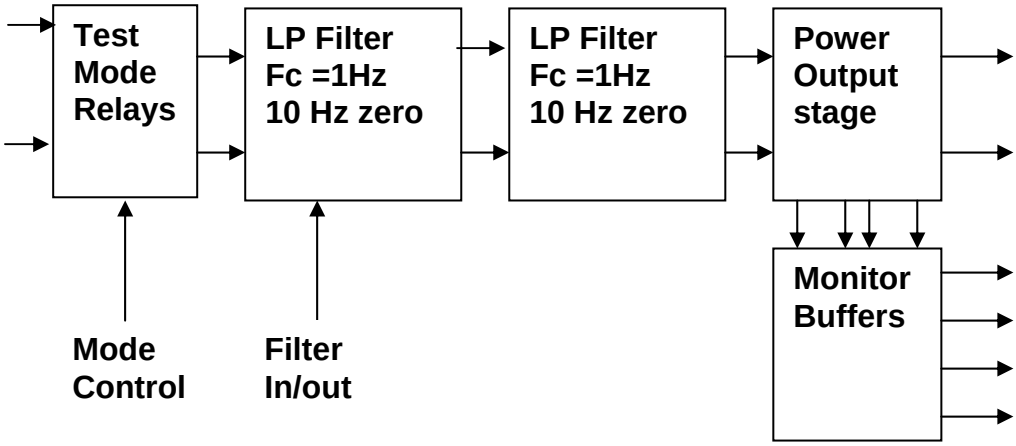

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
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Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

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2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

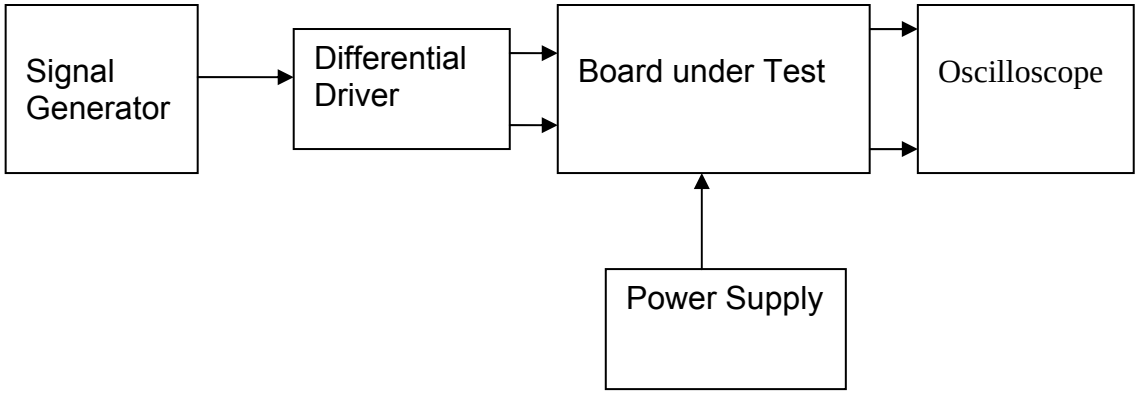
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

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Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
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Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.98	√	
+15v TP4	14.94	√	
-15v TP6	-14.95	√	

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP26P……Serial No ……
Test Engineer ….Xen…….
Date …….3/11/09……..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP26P……Serial No ……
Test Engineer ….Xen……..
Date …….3/11/09..……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP26P……Serial No ……
Test Engineer ….Xen……..
Date …….3/11/09……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.49	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP26P……Serial No ……
Test Engineer ….Xen……
Date ……3/11/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.486	Pin 3 to Pin 4	0.488	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.489	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP26P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.1	√	-24.1	√	-24.2	√
-7v	-17.0	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.1	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	17.0	√	16.9	√	17.0	√	17.0	√
10v	24.2	√	24.1	√	24.1	√	24.1	√

Unit……T_TOP26P……Serial No ……
Test Engineer ….Xen…….
Date ……4/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-137dB	-111dB	473Hz
Channel 2	Channel 1	-142dB	-112dB	263Hz
Channel 2	Channel 3	-136dB	-111dB	275Hz
Channel 3	Channel 2	-141dB	-111dB	219Hz
Channel 3	Channel 4	-130dB	-111dB	266Hz
Channel 4	Channel 3	-143dB	-111dB	219Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP26P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

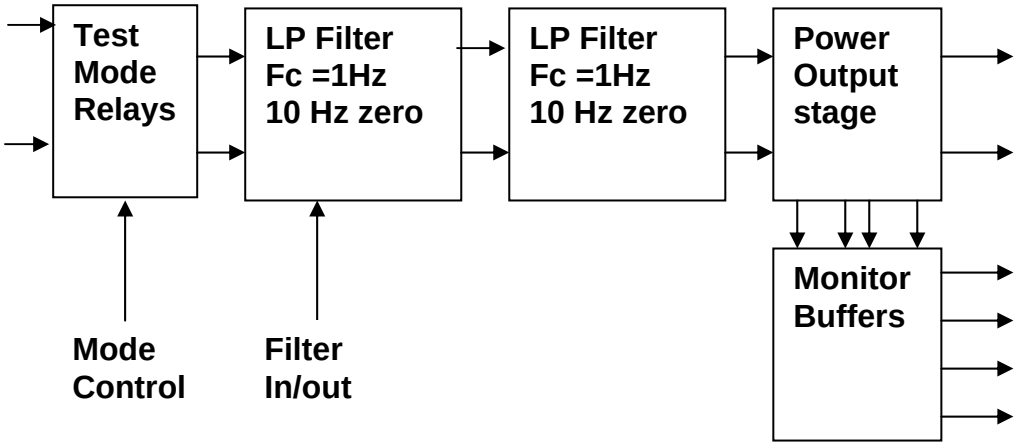
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP27P……Serial No ……
Test Engineer…..Xen……
Date……..4/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP27P……Serial No ……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP27P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

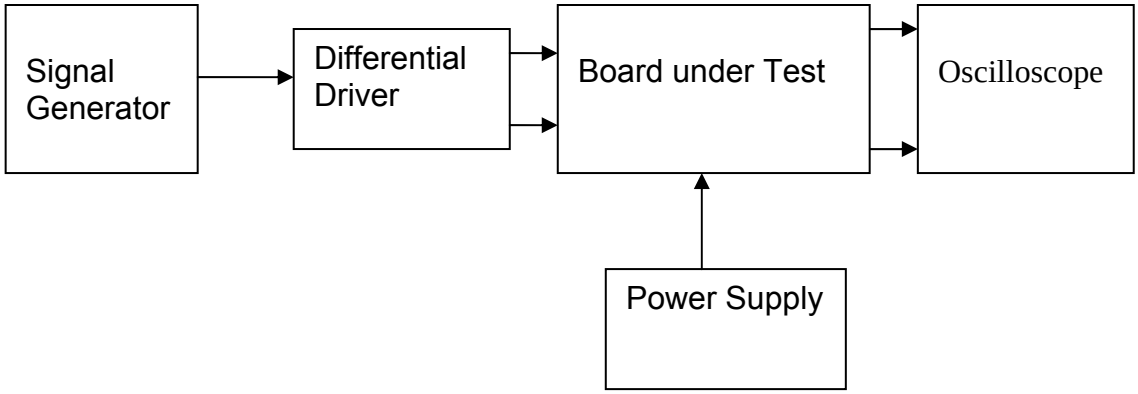
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP27P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.05	1mV	√
+15v TP4	14.95	1mV	√
-15v TP6	-14.99	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP27P……Serial No ……
Test Engineer ….Xen…….
Date ……4/11/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP27P……Serial No ……
Test Engineer ….Xen……..
Date ……4/11/09..……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.65	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP27P……Serial No ……
Test Engineer ….Xen……..
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP27P……Serial No ……
Test Engineer ….Xen……
Date ……4/11/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.488	Pin 7 to Pin 8	0.488	√
3	0.47-0.49v	0.486	Pin 11 to Pin 12	0.488	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP27P……Serial No ……
Test Engineer ….Xen…….
Date ……4/11/09……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.2	√	-24.1	√	-24.1	√
-7v	-17.0	√	-17.0	√	-17.0	√	-16.9	√
-5v	-12.0	√	-12.1	√	-12.0	√	-12.0	√
-1v	-2.4	√	2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	17.0	√	16.9	√	16.9	√
10v	24.0	√	24.1	√	24.0	√	24.0	√

Unit……T_TOP27P……Serial No ……
Test Engineer ….Xen…….
Date ……4/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-132dB	-115dB	631Hz
Channel 2	Channel 1	-136dB	-113dB	525Hz
Channel 2	Channel 3	-134dB	110dB	750Hz
Channel 3	Channel 2	-135dB	-111dB	363Hz
Channel 3	Channel 4	-111dB	-73dB	166Hz
Channel 4	Channel 3	-135dB	-111dB	871Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP27P……Serial No ……
Test Engineer ….Xen……..
Date ……4/11/09..……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

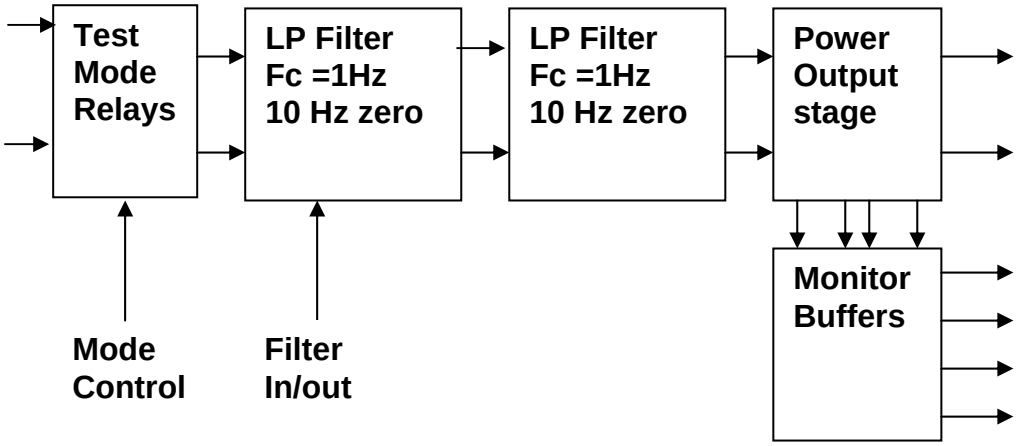
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP28P……Serial No ……
Test Engineer…..Xen……
Date……..4/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP28P……Serial No ……
Test Engineer ….Xen……..
Date ……4/11/09..……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP28P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

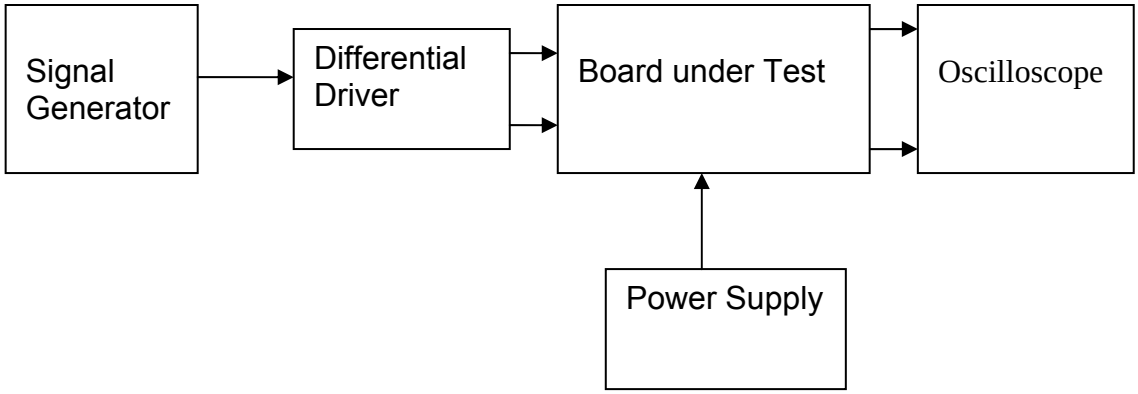
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP28P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.10	1mV	√
+15v TP4	14.91	1mV	√
-15v TP6	-14.98	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP28P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP28P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.15	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	
2	0.47-0.49v	0.485	Pin 7 to Pin 8	0.486	
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.488	

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.2	√	-24.1	√	-24.1	√
-7v	-17.0	√	-17.0	√	-16.9	√	-16.9	√
-5v	-12.1	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	17.0	√	16.9	√	17.0	√
10v	24.0	√	24.1	√	24.1	√	24.2	√

Unit……T_TOP28P……Serial No ……
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12. Crosstalk Tests

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Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-135dB	-113dB	871Hz
Channel 2	Channel 1	-141dB	-110dB	479Hz
Channel 2	Channel 3	-140dB	-111dB	422Hz
Channel 3	Channel 2	-136dB	-115dB	575Hz
Channel 3	Channel 4	-139dB	-112dB	575Hz
Channel 4	Channel 3	-101dB	-72dB	437Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP28P……Serial No ……
Test Engineer ….Xen……..
Date ……4/11/09..……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.43	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

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Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

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1. Description

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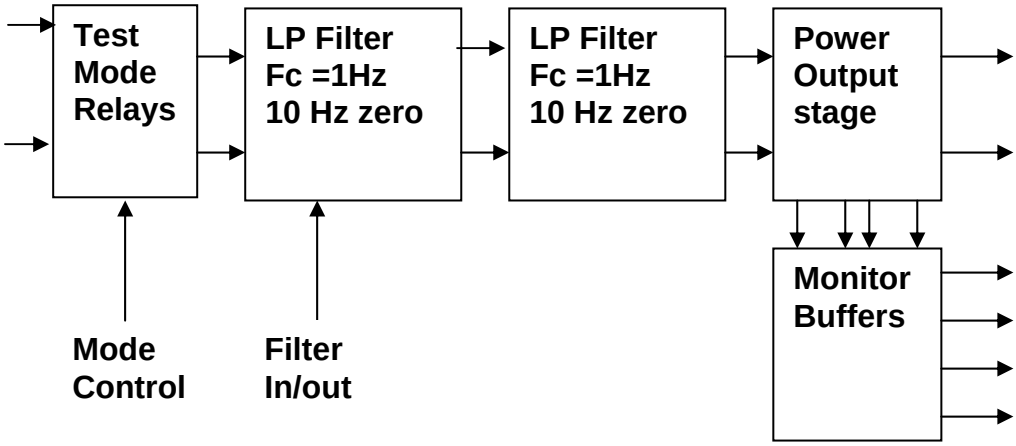

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

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Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP29P……Serial No ……
Test Engineer ….Xen…….
Date ……4/11/09..…….

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP29P……Serial No ……
Test Engineer ….Xen……
Date ……4/11/09..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

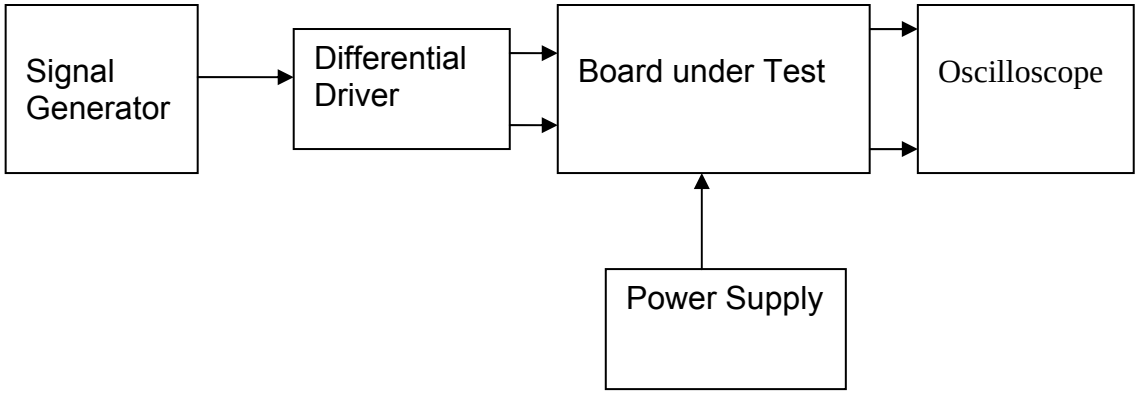
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP29P……Serial No ……
Test Engineer ….Xen……
Date ……4/11/09..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.08	1mV	√
+15v TP4	14.92	1mV	√
-15v TP6	-15.16	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP29P……Serial No ……
Test Engineer ….Xen…….
Date ……4/11/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP29P……Serial No ……
Test Engineer ….Xen……..
Date ……4/11/09..……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP29P……Serial No ……
Test Engineer ….Xen……..
Date ……4/11/09……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP29P……Serial No ……
Test Engineer ….Xen……
Date ……4/11/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.488	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.484	Pin 15 to Pin 16	0.487	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP29P……Serial No ……
Test Engineer ….Xen…….
Date ……4/11/09……..

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.0	√	-24.1	√	-24.0	√
-7v	-17.0	√	-16.9	√	-16.9	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	16.9	√	16.9	√
10v	24.0	√	24.1	√	24.0	√	24.0	√

Unit……T_TOP29P……Serial No ……
Test Engineer ….Xen…….
Date ……4/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-138dB	-112dB	437Hz
Channel 2	Channel 1	-136dB	-116dB	275Hz
Channel 2	Channel 3	-149dB	-113dB	479Hz
Channel 3	Channel 2	-142dB	-114dB	479Hz
Channel 3	Channel 4	-143dB	-113dB	437Hz
Channel 4	Channel 3	-140dB	-113dB	923Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP29P……Serial No ……
Test Engineer ….Xen……..
Date ……4/11/09..……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

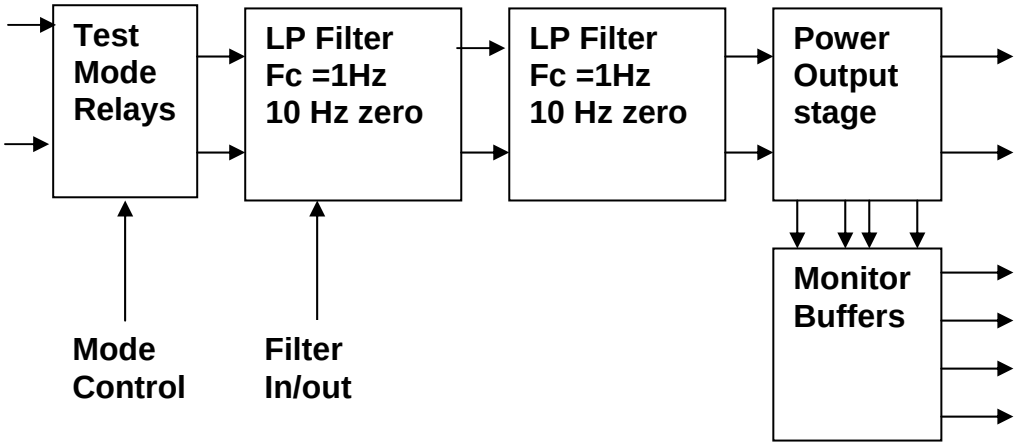
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP30P……Serial No ……
Test Engineer…..Xen……
Date……..5/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP30P……Serial No ……
Test Engineer ….Xen……..
Date …….5/11/09..……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP30P……Serial No ……
Test Engineer ….Xen…….
Date ……4/11/09..…….

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP30P……Serial No ……
Test Engineer ….Xen……
Date ……4/11/09..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

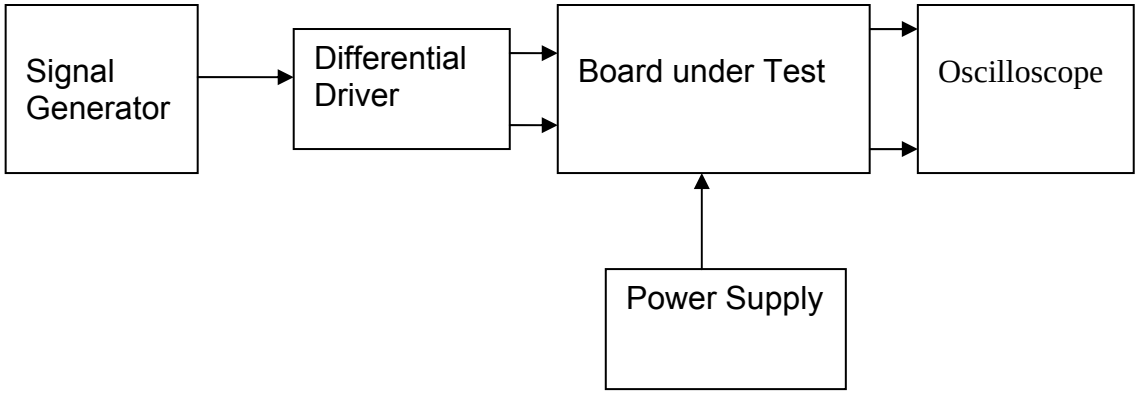
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP30P……Serial No ……
Test Engineer ….Xen……
Date ……4/11/09..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.11	1mV	√
+15v TP4	14.97	1mV	√
-15v TP6	-15.01	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP30P……Serial No ……
Test Engineer ….Xen…….
Date ……4/11/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP30P……Serial No ……
Test Engineer ….Xen……..
Date ……4/11/09..……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP30P……Serial No ……
Test Engineer ….Xen……..
Date …….5/11/09……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP30P……Serial No ……
Test Engineer ….Xen……
Date …….5/11/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.487	Pin 7 to Pin 8	0.488	√
3	0.47-0.49v	0.486	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.1	√	-24.2	√	-24.1	√
-7v	-17.0	√	-17.0	√	-17.0	√	-16.9	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	17.0	√	17.0	√	17.0	√
10v	24.0	√	24.1	√	24.1	√	24.1	√

Unit……T_TOP30P……Serial No ……
Test Engineer ….Xen…….
Date …….5/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-131dB	-114dB	275Hz
Channel 2	Channel 1	-141dB	-114dB	437Hz
Channel 2	Channel 3	-129dB	-113dB	437Hz
Channel 3	Channel 2	-130dB	-112dB	479Hz
Channel 3	Channel 4	-137dB	-113dB	631Hz
Channel 4	Channel 3	-109dB	-71dB	174Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP30P……Serial No ……
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Date …….5/11/09..……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

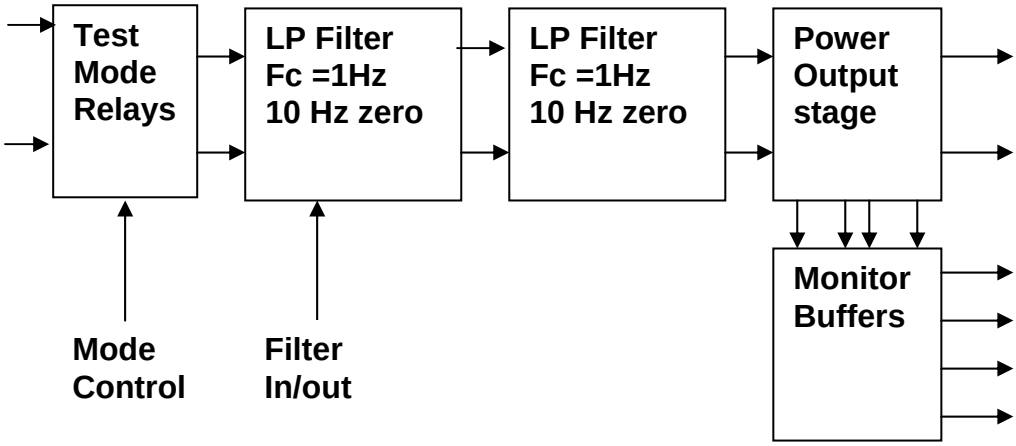
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP31P……Serial No ……
Test Engineer…..Xen……
Date……..5/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP31P……Serial No ……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

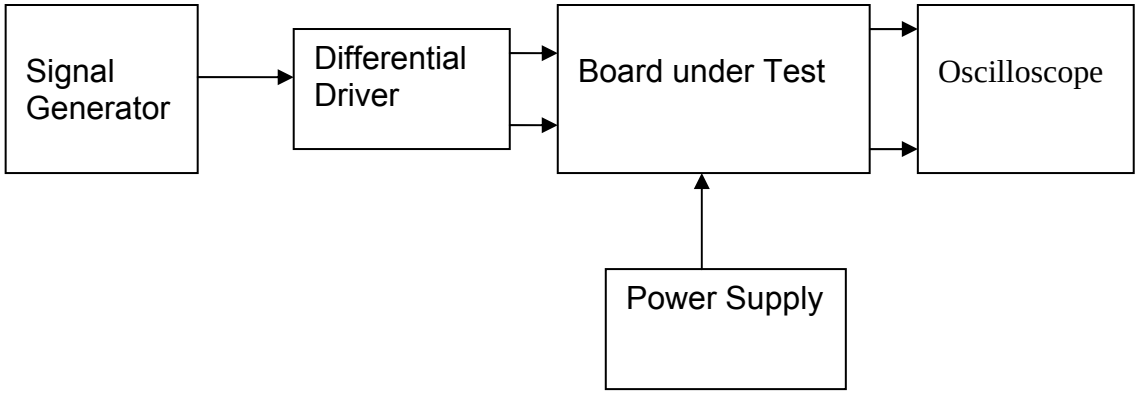
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.99	1mV	√
+15v TP4	14.98	1mV	√
-15v TP6	-14.99	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP31P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP31P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP31P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP31P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.2	√	-24.1	√	-24.1	√
-7v	-17.0	√	-17.0	√	-16.9	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	17.0	√	16.9	√	16.9	√
10v	24.0	√	24.0	√	24.1	√	24.2	√

Unit……T_TOP31P……Serial No ……
Test Engineer ….Xen…….
Date …….5/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-132dB	-106dB	437Hz
Channel 2	Channel 1	-139dB	-111dB	417Hz
Channel 2	Channel 3	-136dB	-112dB	479Hz
Channel 3	Channel 2	-136dB	-113dB	479Hz
Channel 3	Channel 4	-140dB	-110dB	229Hz
Channel 4	Channel 3	-156dB	-112dB	661Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP31P……Serial No ……
Test Engineer ….Xen……..
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

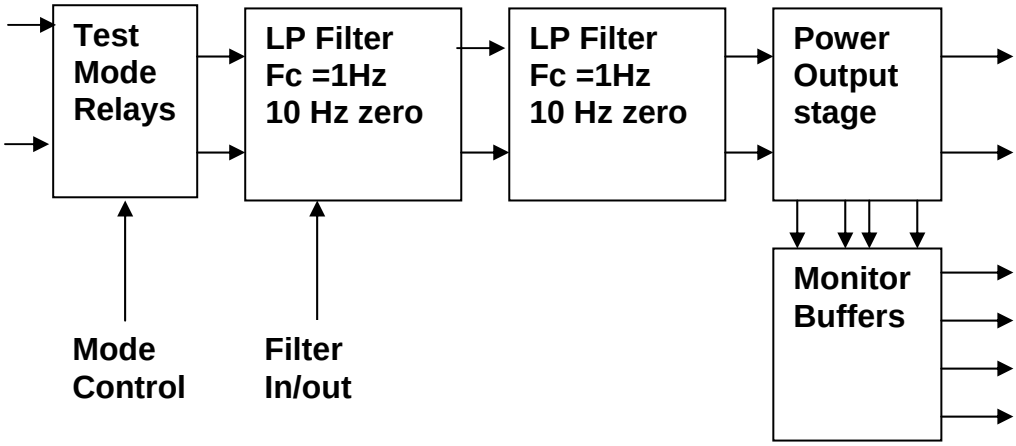
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP32P……Serial No ……
Test Engineer…..Xen……
Date……..5/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP32P……Serial No ……
Test Engineer ….Xen……..
Date …….5/11/09..……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP32P……Serial No ……
Test Engineer ….Xen…….
Date …….5/11/09..……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP32P……Serial No ……
Test Engineer ….Xen……
Date …….5/11/09..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

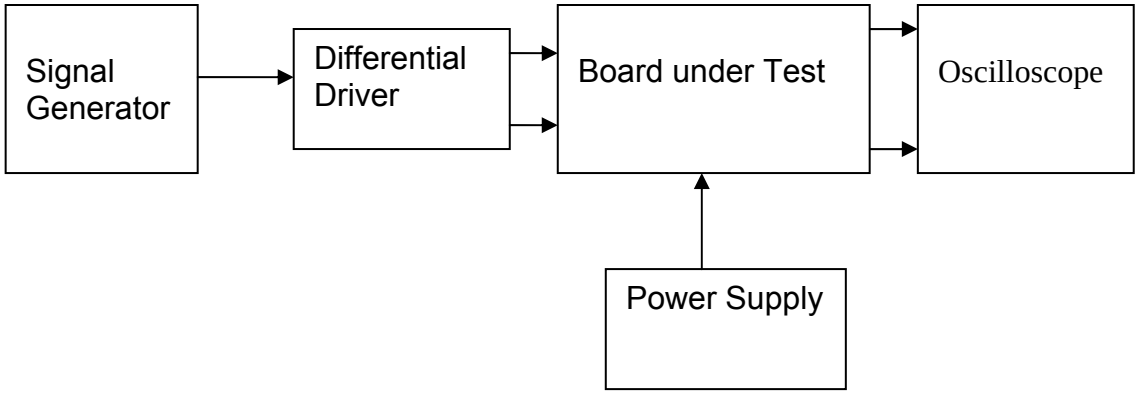
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP32P……Serial No ……
Test Engineer ….Xen……
Date …….5/11/09..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.03	1mV	√
+15v TP4	14.80	1mV	√
-15v TP6	-15.01	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP32P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP32P……Serial No ……
Test Engineer ….Xen……..
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.65	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP32P……Serial No ……
Test Engineer ….Xen……..
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.486	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.486	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.0	√	-24.2	√	-24.1	√
-7v	-17.0	√	-16.9	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.1	√	-12.0	√
-1v	-2.4	√	-2.4	√	2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.9	√	16.9	√	16.9	√
10v	24.0	√	24.0	√	24.0	√	24.0	√

Unit……T_TOP32P……Serial No ……
Test Engineer ….Xen…….
Date …….5/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-146dB	-107dB	457Hz
Channel 2	Channel 1	-132dB	-108dB	479Hz
Channel 2	Channel 3	-127dB	-111dB	437Hz
Channel 3	Channel 2	-137dB	-111dB	437Hz
Channel 3	Channel 4	-142dB	-112dB	229Hz
Channel 4	Channel 3	-131dB	-109dB	479Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP32P……Serial No ……
Test Engineer ….Xen……..
Date ……4/11/09..……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

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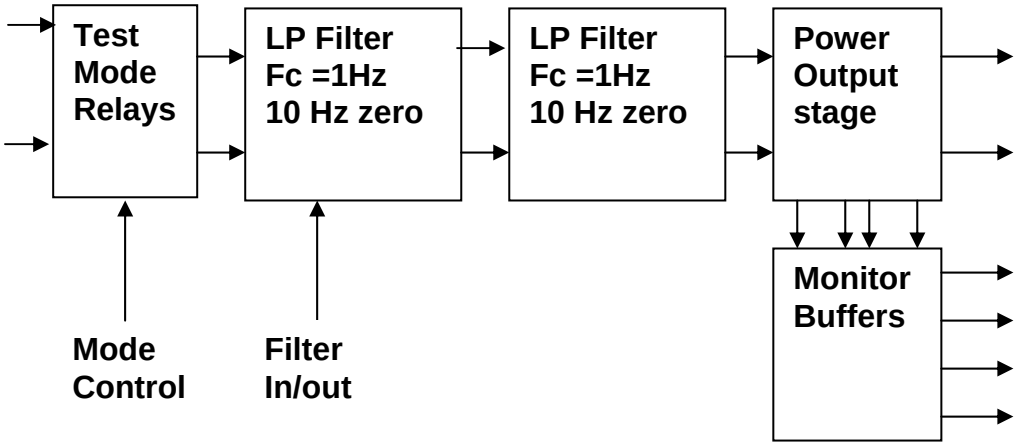

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
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Low noise Balanced Driver circuit
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Record the Models and serial numbers of the test equipment used below.

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Unit……T_TOP33P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP33P……Serial No ……
Test Engineer ….Xen……
Date ……6/11/09..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

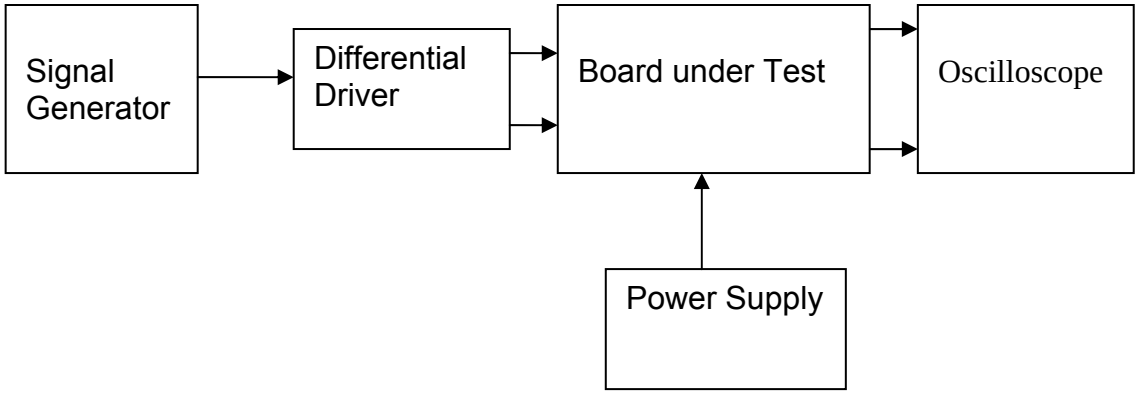
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP33P……Serial No ……
Test Engineer ….Xen……
Date …….6/11/09..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.09	1mV	√
+15v TP4	14.84	1mV	√
-15v TP6	-14.89	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP33P……Serial No ……
Test Engineer ….Xen…….
Date …….6/11/09……..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP33P……Serial No ……
Test Engineer ….Xen……..
Date …….6/11/09..……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP33P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP33P……Serial No ……
Test Engineer ….Xen……
Date ……6/11/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.486	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.489	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.0	√	-24.0	√	-24.1	√	-24.0	√
-7v	-17.0	√	-16.9	√	-16.9	√	-16.9	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	17.0	√	16.9	√	16.9	√
10v	24.0	√	24.1	√	24.1	√	24.0	√

Unit……T_TOP33P……Serial No ……
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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-138dB	-115dB	363Hz
Channel 2	Channel 1	-137dB	-114dB	240Hz
Channel 2	Channel 3	-135dB	-107dB	363Hz
Channel 3	Channel 2	-150dB	-110dB	479Hz
Channel 3	Channel 4	-116dB	-110dB	631Hz
Channel 4	Channel 3	-117dB	-111dB	550Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

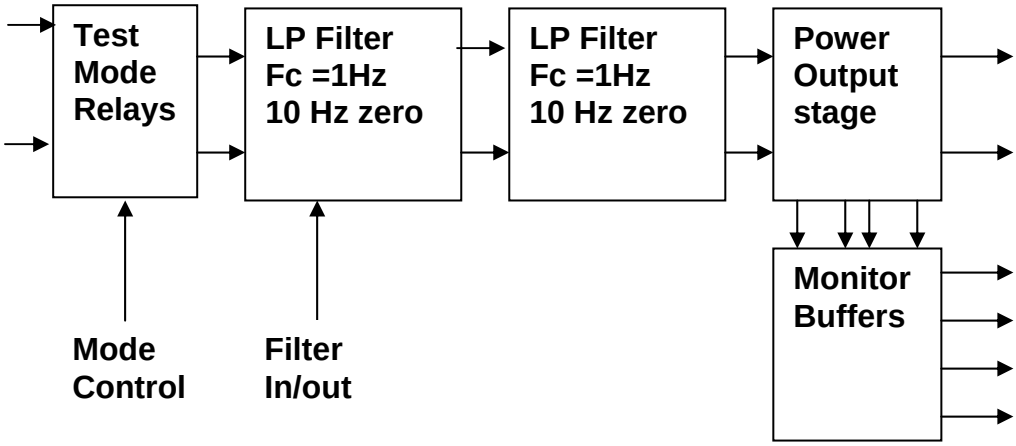
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP34P……Serial No ……
Test Engineer…..Xen……
Date……..6/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP34P……Serial No ……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

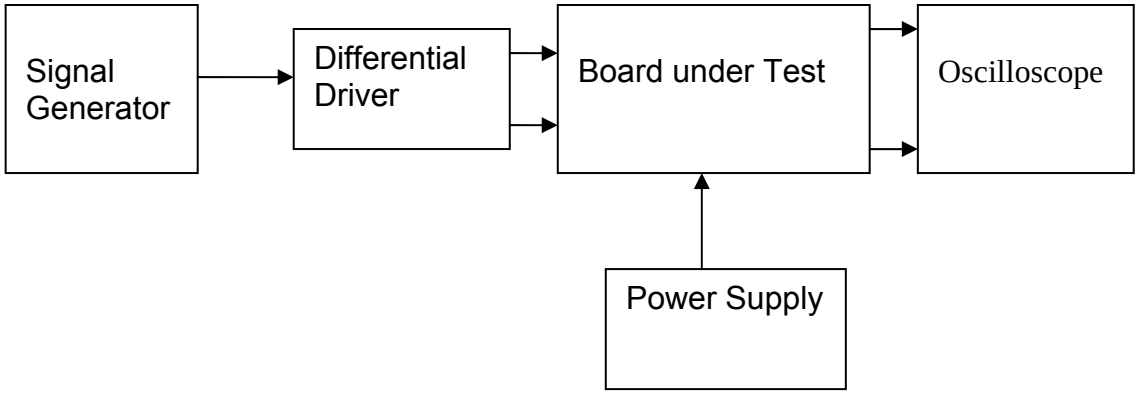
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP34P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.07	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-14.92	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP34P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP34P……Serial No ……
Test Engineer ….Xen……..
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.65	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP34P……Serial No ……
Test Engineer ….Xen……
Date ……6/11/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.486	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.484	Pin 11 to Pin 12	0.486	√
4	0.47-0.49v	0.487	Pin 15 to Pin 16	0.489	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP34P……Serial No ……
Test Engineer ….Xen…….
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.1	√	-24.1	√	-24.1	√
-7v	-17.0	√	-17.0	√	-17.0	√	-16.9	√
-5v	-12.1	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	17.0	√	17.0	√	16.9	√	16.9	√
10v	24.1	√	24.1	√	24.1	√	24.1	√

Unit……T_TOP34P……Serial No ……
Test Engineer ….Xen…….
Date …….6/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-143dB	-111dB	417Hz
Channel 2	Channel 1	-141dB	-112dB	661Hz
Channel 2	Channel 3	-134dB	-110dB	479Hz
Channel 3	Channel 2	-136dB	-109dB	229Hz
Channel 3	Channel 4	-136dB	-110dB	275Hz
Channel 4	Channel 3	-133dB	-109dB	422Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP34P……Serial No ……
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Date …….6/11/09……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.45	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

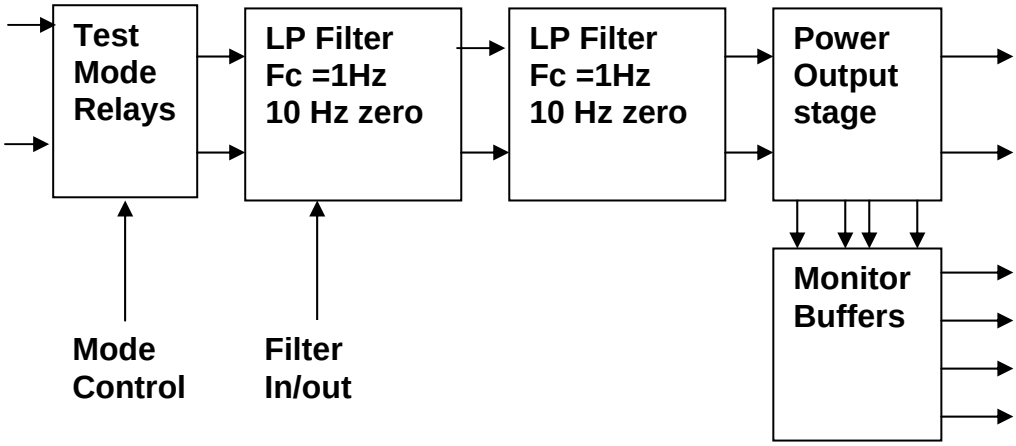
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP35P……Serial No ……
Test Engineer…..Xen……
Date……..9/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP35P……Serial No ……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP35P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

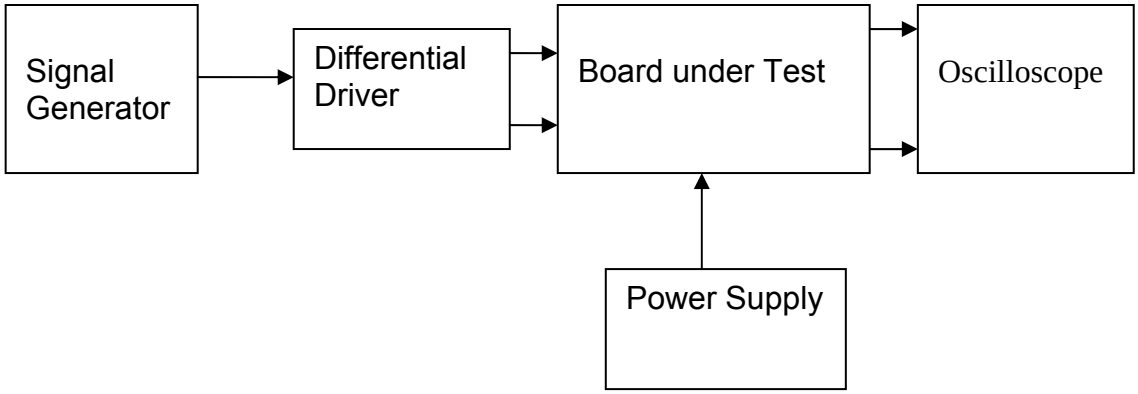
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP35P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.08	1mV	√
+15v TP4	14.94	1mV	√
-15v TP6	-15.07	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP35P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.65	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.15	3v to 3.4v	√
Ch3	3.15	3v to 3.4v	√
Ch4	3.15	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.486	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.487	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.486	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.487	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP35P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.2	√	-24.2	√	-24.2	√
-7v	-16.9	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.0	√	-12.0	√	-12.1	√	-12.1	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.8	√	16.9	√	16.9	√	17.0	√
10v	24.1	√	24.2	√	24.0	√	24.1	√

Unit……T_TOP35P……Serial No ……
Test Engineer ….Xen…….
Date …….9/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-137dB	-112dB	417Hz
Channel 2	Channel 1	-130dB	-114dB	871Hz
Channel 2	Channel 3	-144dB	-113dB	437Hz
Channel 3	Channel 2	-136dB	-111dB	692Hz
Channel 3	Channel 4	-136dB	-111dB	479Hz
Channel 4	Channel 3	-140dB	-112dB	661Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP35P……Serial No ……
Test Engineer ….Xen……..
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

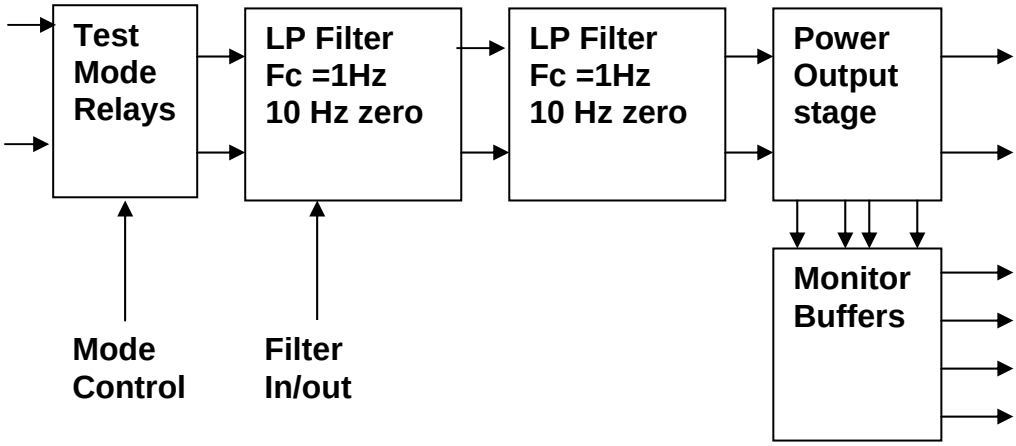
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP36P……Serial No ……
Test Engineer…..Xen……
Date……..9/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen……..
Date …….9/11/09..……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen…….
Date …….9/11/09..……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen……
Date …….9/11/09..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

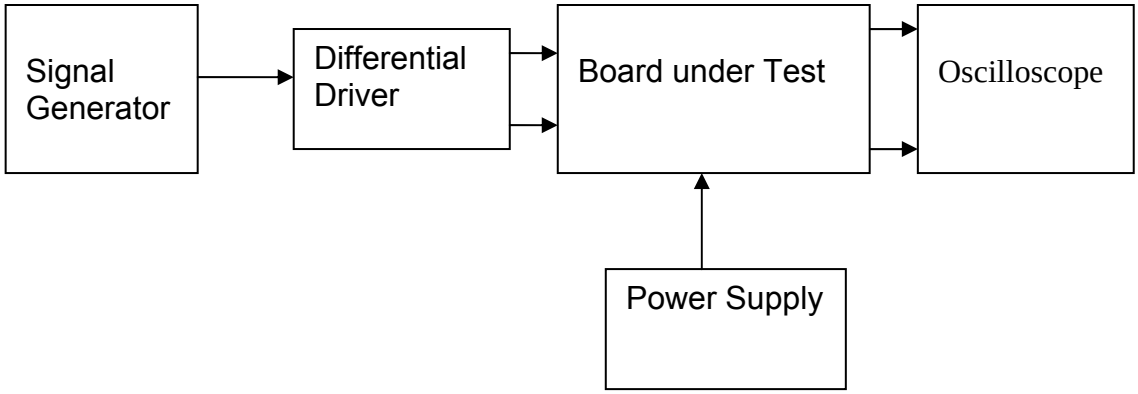
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen……
Date …….9/11/09..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.04	1mV	√
+15v TP4	14.92	1mV	√
-15v TP6	-14.93	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen…….
Date …….9/11/09……..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen……..
Date …….9/11/09..……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	**4.7v to 5v**	√
Ch2	4.8	4.9	4.9	**4.7v to 5v**	√
Ch3	4.8	4.9	4.9	**4.7v to 5v**	√
Ch4	4.8	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen……..
Date ……9/11/09……..

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen……
Date ……9/11/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.486	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.486	Pin 7 to Pin 8	0.487	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.486	Pin 15 to Pin 16	0.488	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen…….
Date …….9/11/09……..

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.1	√	-24.1	√	-24.1	√	-24.1	√
-7v	-17.0	√	-17.0	√	-16.9	√	-16.8	√
-5v	-12.0	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	17.0	√	16.9	√	17.0	√	17.0	√
10v	24.2	√	24.1	√	24.1	√	24.2	√

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen…….
Date …….9/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-132dB	-110dB	229Hz
Channel 2	Channel 1	-145dB	-108dB	219Hz
Channel 2	Channel 3	-135dB	-113dB	232Hz
Channel 3	Channel 2	-118dB	-110dB	525Hz
Channel 3	Channel 4	-136dB	-110dB	479Hz
Channel 4	Channel 3	-131dB	-113dB	871Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP36P……Serial No ……
Test Engineer ….Xen……..
Date …….9/11/09..……..

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

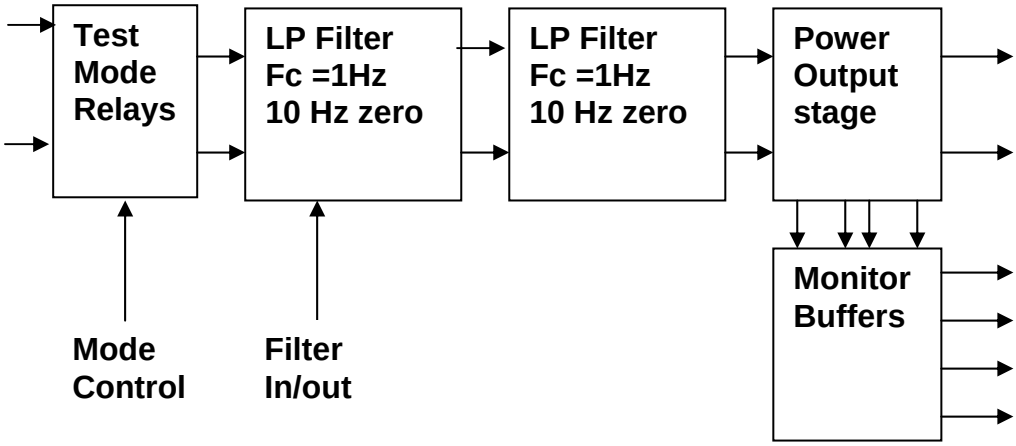
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP37P……Serial No ……
Test Engineer…..Xen……
Date……..10/11/09..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP37P……Serial No ……
Test Engineer ….Xen……..
Date ……10/11/09..……..

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	Tektronix	2225	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP37P……Serial No ……
Test Engineer ….Xen…….
Date …….9/11/09..…….

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP37P……Serial No ……
Test Engineer ….Xen……
Date …….9/11/09..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

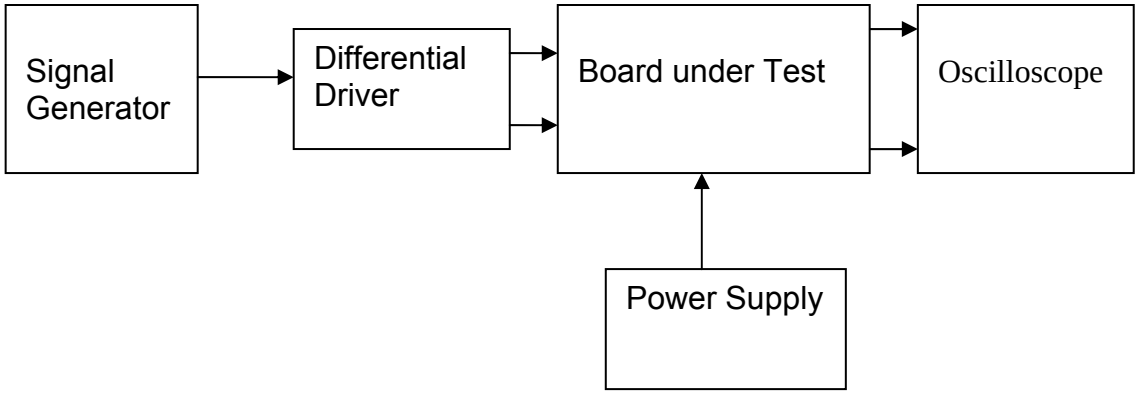
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP37P……Serial No ……
Test Engineer ….Xen……
Date …….9/11/09..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.97	1mV	√
+15v TP4	14.80	1mV	√
-15v TP6	-14.90	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP37P……Serial No ……
Test Engineer ….Xen…….
Date …….9/11/09……..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP37P……Serial No ……
Test Engineer ….Xen……..
Date …….9/11/09..……..

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.75	4.9	4.9	**4.7v to 5v**	√
Ch2	4.75	4.9	4.9	**4.7v to 5v**	√
Ch3	4.75	4.9	4.9	**4.7v to 5v**	√
Ch4	4.75	4.9	4.9	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP37P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP37P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.22	Pin 1 to Pin 2	1.22	√
2	1.15-1.25v	1.22	Pin 5 to Pin 6	1.22	√
3	1.15-1.25v	1.22	Pin 9 to Pin 10	1.22	√
4	1.15-1.25v	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.485	Pin 3 to Pin 4	0.487	√
2	0.47-0.49v	0.485	Pin 7 to Pin 8	0.486	√
3	0.47-0.49v	0.485	Pin 11 to Pin 12	0.487	√
4	0.47-0.49v	0.485	Pin 15 to Pin 16	0.487	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.1	√	-24.2	√	-24.2	√
-7v	-17.0	√	-17.0	√	-17.0	√	-17.0	√
-5v	-12.1	√	-12.0	√	-12.0	√	-12.0	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.3	√	2.4	√	2.4	√
5v	12.0	√	12.0	√	12.0	√	12.0	√
7v	16.9	√	16.8	√	16.9	√	16.8	√
10v	24.0	√	24.0	√	24.0	√	24.0	√

Unit……T_TOP37P……Serial No ……
Test Engineer ….Xen…….
Date …….9/11/09..……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-135dB	-116dB	240Hz
Channel 2	Channel 1	-143dB	-113dB	275Hz
Channel 2	Channel 3	-132dB	-111dB	955Hz
Channel 3	Channel 2	-143dB	-109dB	437Hz
Channel 3	Channel 4	-142dB	-112dB	832Hz
Channel 4	Channel 3	-138dB	-110dB	437Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

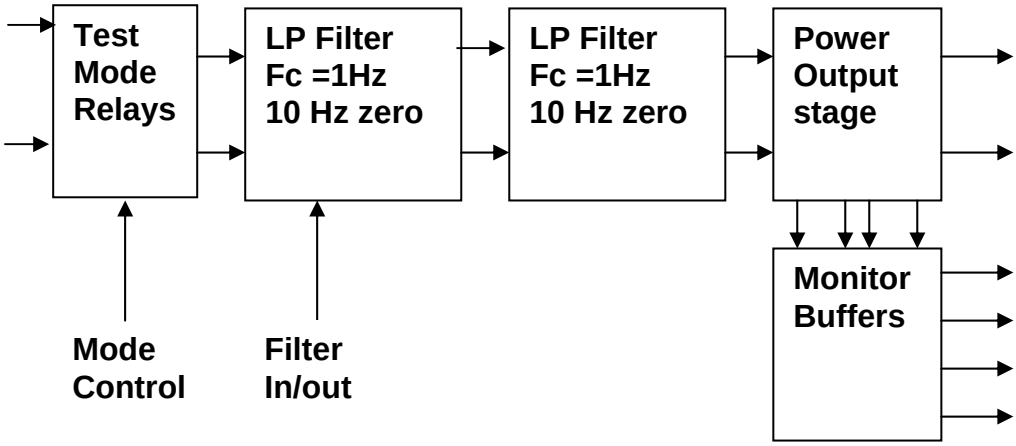
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP38P……Serial No ……
Test Engineer ….Xen……..……
Date ……10/12/09……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

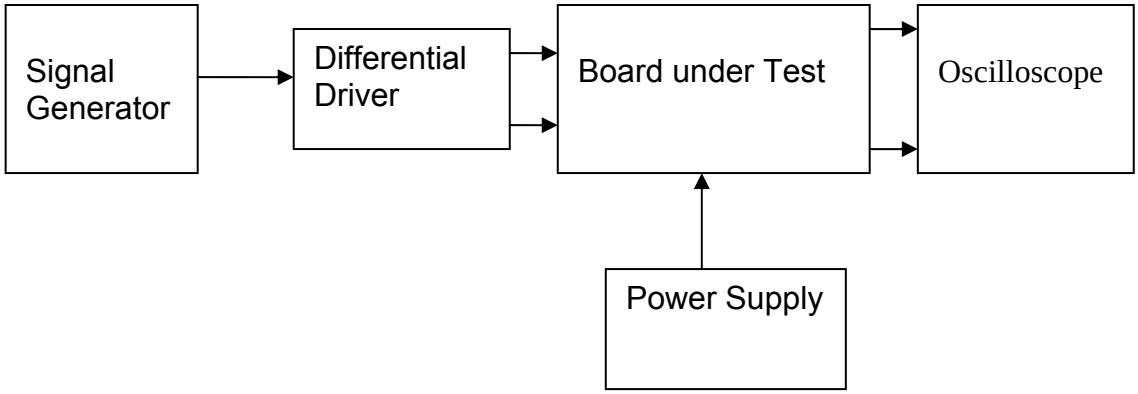
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.14	1mV	√
+15v TP4	14.94	1mV	√
-15v TP6	-15.10	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP38P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3.3v to 3.7v	√
Ch2	3.4	3.3v to 3.7v	√
Ch3	3.3	3.3v to 3.7v	√
Ch4	3.4	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	0.48 to 0.75v	√
Ch2	0.67	0.48 to 0.75v	√
Ch3	0.67	0.48 to 0.75v	√
Ch4	0.67	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP38P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.480	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP38P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.8	√	-24.8	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.3	√	-17.3	√	-17.2	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.42	√	2.4	√	2.4	√
5v	12.3	√	12.3	√	12.2	√	12.2	√
7v	17.2	√	17.1	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP38P……Serial No ……
Test Engineer ….Xen……..……
Date ……10/12/09……..……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

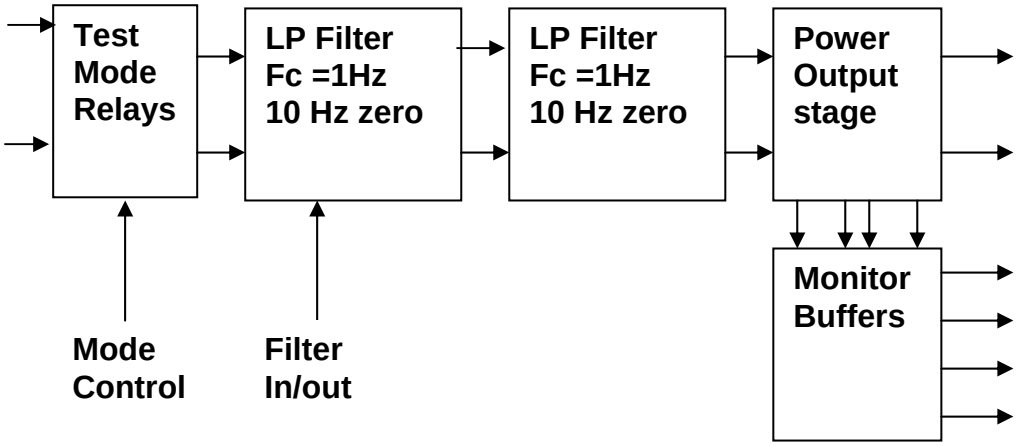
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP39P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP39P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP39P……Serial No ……
Test Engineer ….Xen……..……
Date ……10/12/09……..……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP39P……Serial No ……
Test Engineer ….Xen……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

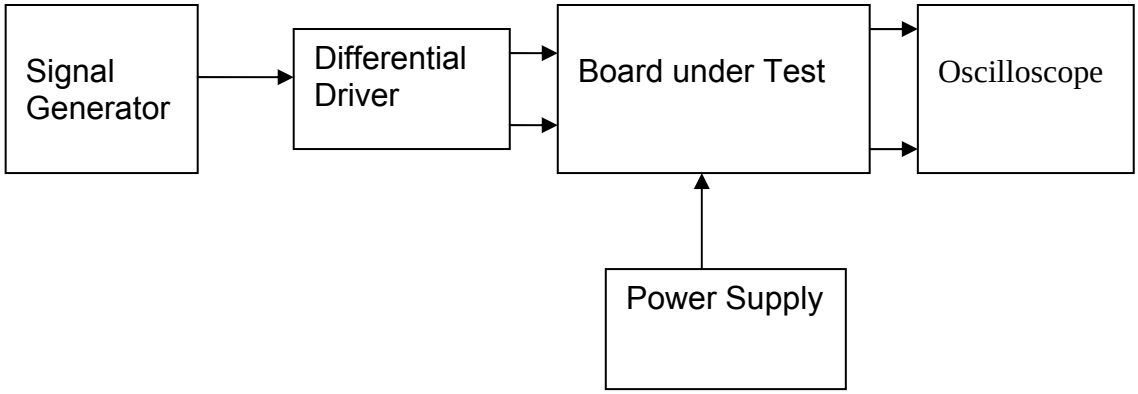
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP39P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.07	1mV	√
+15v TP4	14.92	1mV	√
-15v TP6	-15.06	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP39P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP39P……Serial No ……
Test Engineer ….Xen……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	**4.7v to 5v**	√
Ch2	4.9	5.0	5.0	**4.7v to 5v**	√
Ch3	4.9	5.0	5.0	**4.7v to 5v**	√
Ch4	4.9	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	**4.7 to 5v**	√
Ch2	4.9	**4.7 to 5v**	√
Ch3	4.9	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.68	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP39P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.25	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.49	0.4v to 0.5v	√
Ch2	0.49	0.4v to 0.5v	√
Ch3	0.49	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP39P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.482	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP39P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.3	√	-17.2	√	-17.1	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.4	√
5v	12.1	√	12.2	√	12.2	√	12.1	√
7v	17.0	√	17.0	√	17.1	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP39P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

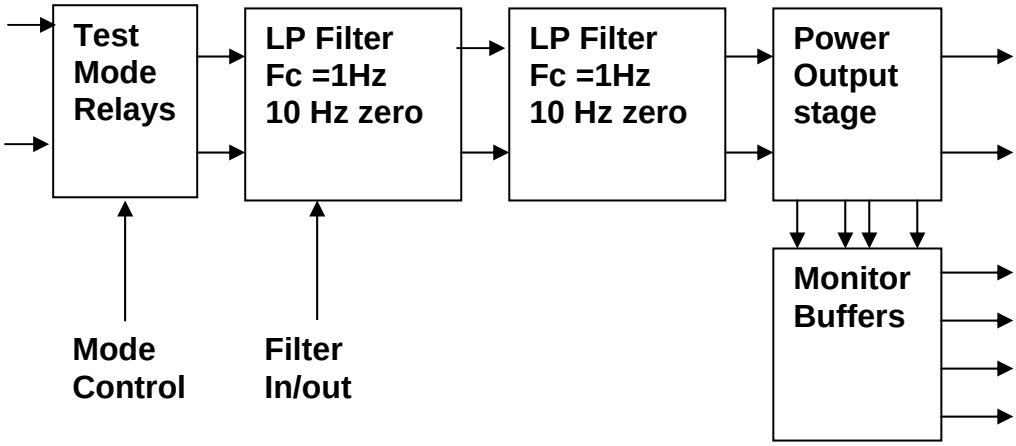
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP40P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

Contents

1. Description

Block diagram



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Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

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This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP40P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP40P……Serial No ……
Test Engineer ….Xen……..……
Date ……10/12/09……..……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C104 and C105 on all channels and replaced capacitors C102 and C103 with a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP40P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

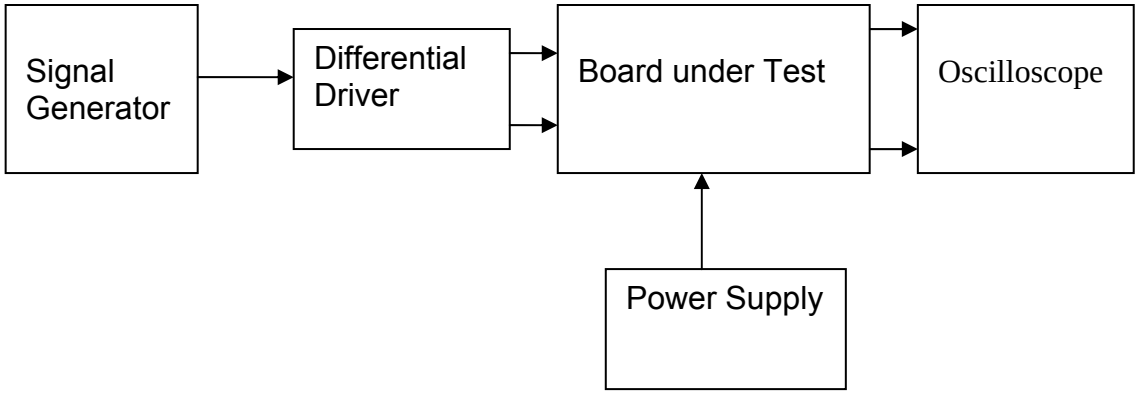
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP40P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.09	1mV	√
+15v TP4	14.89	1mV	√
-15v TP6	-14.98	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP40P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP40P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	**4.7v to 5v**	√
Ch2	4.9	5.0	5.0	**4.7v to 5v**	√
Ch3	4.9	5.0	5.0	**4.7v to 5v**	√
Ch4	4.9	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	**4.7 to 5v**	√
Ch2	4.9	**4.7 to 5v**	√
Ch3	4.9	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.35	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP40P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.5	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP40P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.480	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.482	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP40P……Serial No ……
Test Engineer ….Xen……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.0	√	-17.1	√	-17.0	√	-17.0	√
-5v	-12.2	√	-12.5	√	-12.2	√	-12.2	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.42	√	2.41	√
5v	12.1	√	12.1	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

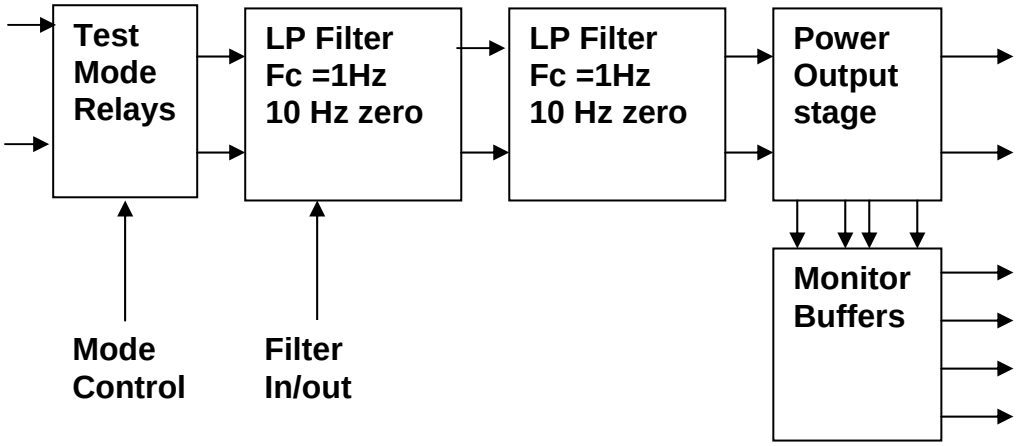
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP41P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP41P……Serial No ……
Test Engineer ….Xen……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP41P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP41P……Serial No ……
Test Engineer ….Xen……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

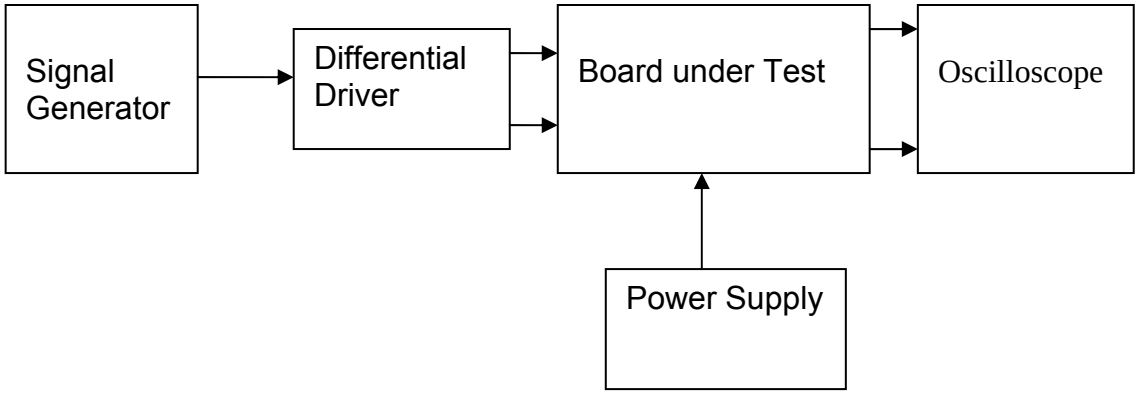
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP41P……Serial No ……
Test Engineer ….Xen……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.02	1mV	√
+15v TP4	14.92	1mV	√
-15v TP6	-14.95	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP41P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP41P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	**4.7v to 5v**	√
Ch2	4.9	5.0	5.0	**4.7v to 5v**	√
Ch3	4.9	5.0	5.0	**4.7v to 5v**	√
Ch4	4.9	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	**4.7 to 5v**	√
Ch2	4.9	**4.7 to 5v**	√
Ch3	4.9	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.45	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.68	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.48	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.48	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.48	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP41P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.25	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.15	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.49	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP41P……Serial No ……
Test Engineer ….Xen……
Date ……10/12/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.480	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP41P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.1	√	-17.4	√	-17.2	√	-17.2	√
-5v	-12.4	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.4	√	-2.42	√	-2.41	√	-2.41	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.41	√	2.41	√	2.42	√
5v	12.0	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.1	√	17.2	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP41P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

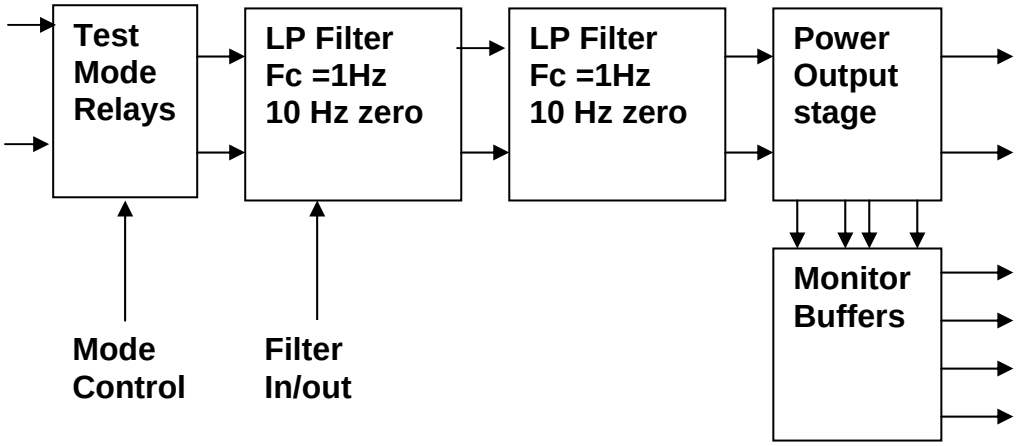
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP42P……Serial No ……
Test Engineer ….Xen……
Date ……11/12/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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Date ……11/12/09……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP42P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP42P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

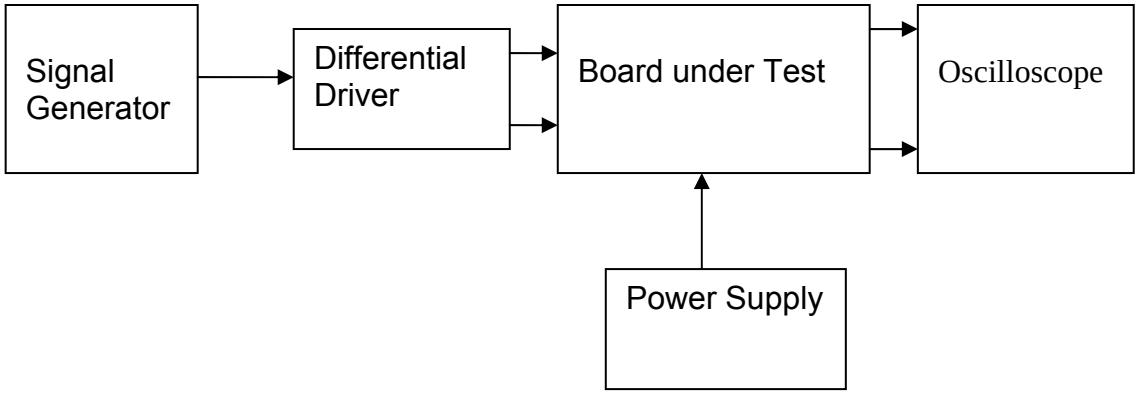
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP42P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.07	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-15.01	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP42P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.15	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.49	0.4v to 0.5v	√
Ch2	0.49	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.480	Pin 3 to Pin 4	0.481	√
2	0.47-0.49v	0.480	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.1	√	-17.1	√	-17.0	√
-5v	-12.4	√	-12.2	√	-12.3	√	-12.3	√
-1v	-2.41	√	-2.4	√	-2.41	√	-2.41	√
0v	0	√	0	√	0	√	0	√
1v	2.41	√	2.4	√	2.4	√	2.41	√
5v	12.2	√	12.1	√	12.1	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP42P……Serial No ……
Test Engineer ….Xen……
Date ……11/12/09……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

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LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

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Contents

1. Description

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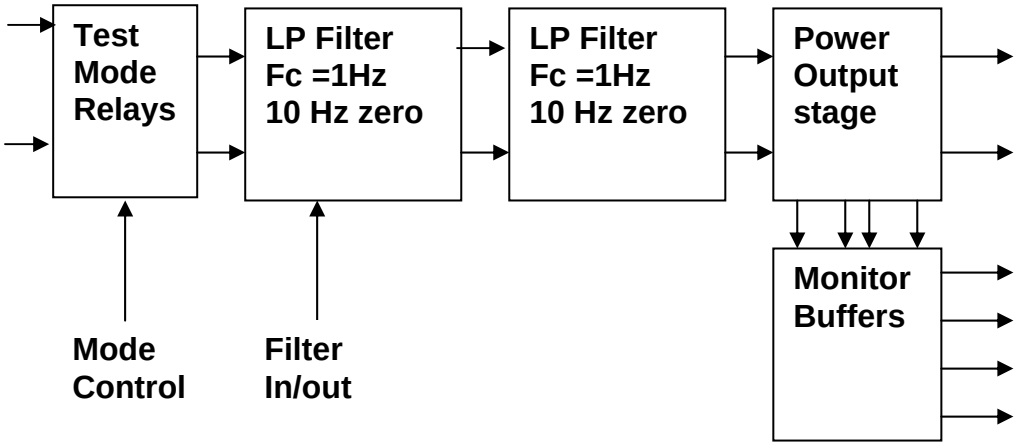

2. Description

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

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This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP43P……Serial No ……
Test Engineer ….Xen……
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2. Test equipment

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Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP43P……Serial No ……
Test Engineer ….Xen……
Date ……11/12/09……..…

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP43P……Serial No ……
Test Engineer ….Xen……
Date ……11/12/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

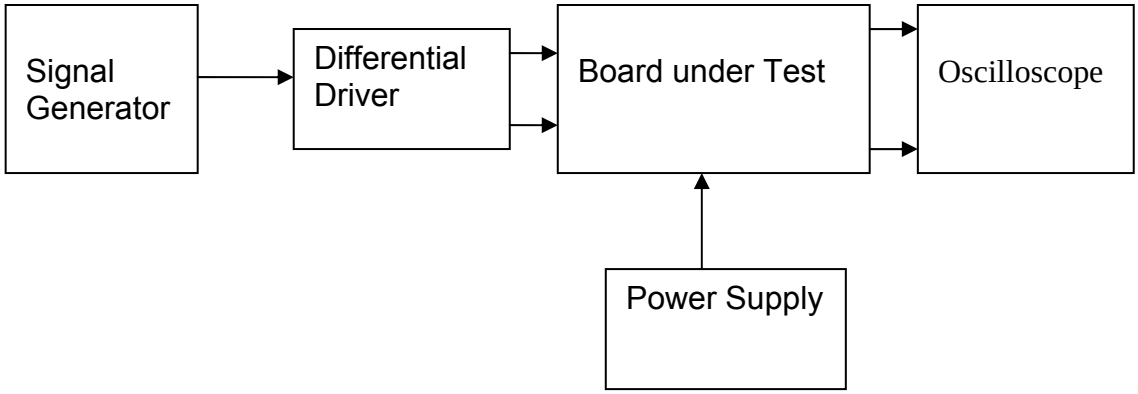
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP43P……Serial No ……
Test Engineer ….Xen……
Date ……11/12/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.07	1mV	√
+15v TP4	14.88	1mV	√
-15v TP6	-15.02	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP43P……Serial No ……
Test Engineer ….Xen……
Date ……11/12/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP43P……Serial No ……
Test Engineer ….Xen……
Date ……11/12/09……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP43P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP43P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.479	Pin 11 to Pin 12	0.481	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP43P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.2	√	-17.2	√	-17.2	√
-5v	-12.4	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.41	√	-2.41	√	-2.42	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.41	√	2.41	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	-12.2	√
7v	17.0	√	17.0	√	17.0	√	17.2	√
10v	24.3	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP43P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

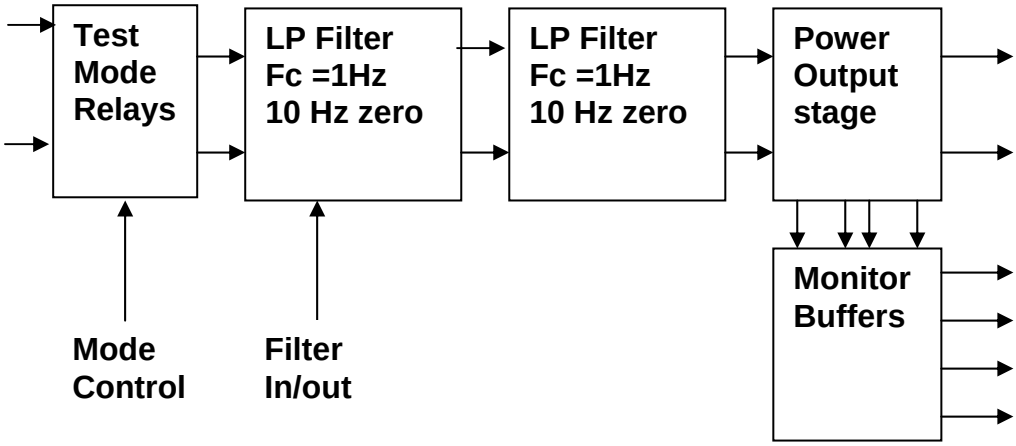
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP44P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP44P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP44P……Serial No ……
Test Engineer ….Xen……..……
Date ……14/12/09……..……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP44P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

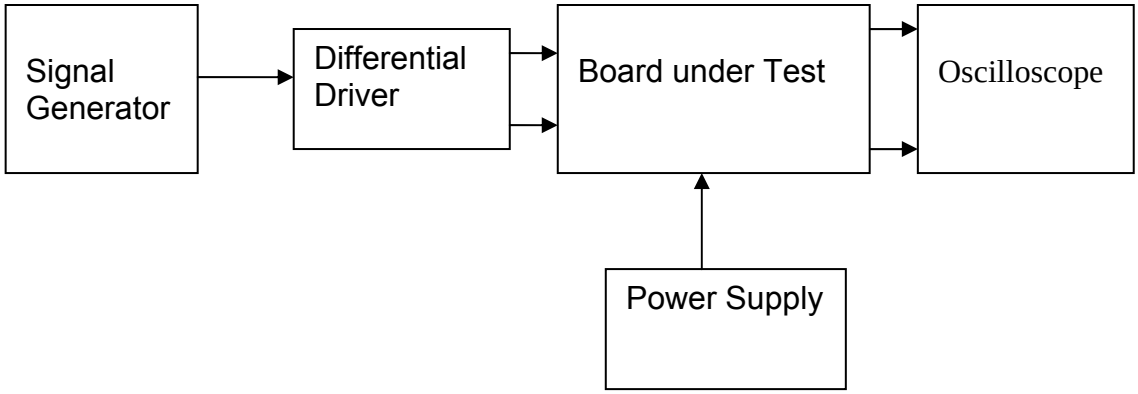
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP44P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.06	1mV	√
+15v TP4	14.92	1mV	√
-15v TP6	-15.03	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP44P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP44P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	**4.7v to 5v**	√
Ch2	4.9	5.0	5.0	**4.7v to 5v**	√
Ch3	4.9	5.0	5.0	**4.7v to 5v**	√
Ch4	4.9	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.9	**4.7 to 5v**	√
Ch3	4.9	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.48	**0.4v to 0.5v**	√
Ch4	0.48	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.48	**0.4v to 0.5v**	√
Ch4	0.48	**0.4v to 0.5v**	√

Unit……T_TOP44P……Serial No ……
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Date ……14/12/09……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.49	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP44P……Serial No ……
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Date ……14/12/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.479	Pin 11 to Pin 12	0.481	√
4	0.47-0.49v	0.480	Pin 15 to Pin 16	0.482	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP44P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.1	√	-17.2	√	-17.1	√	-17.1	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.41	√	-2.42	√	-2.42	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.1	√	17.1	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP44P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

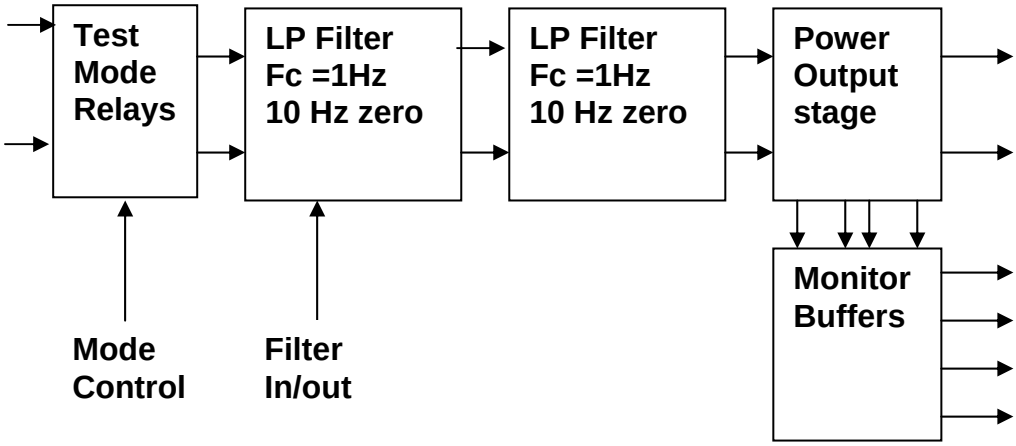
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP45P……Serial No ……
Test Engineer ….Xen……
Date ……14/12/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

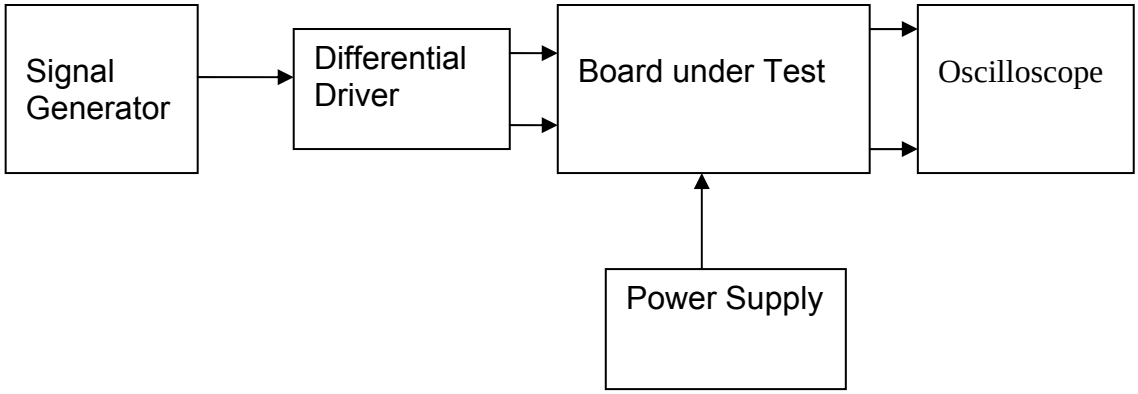
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.09	1mV	√
+15v TP4	14.80	1mV	√
-15v TP6	-14.96	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP45P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	**4.7v to 5v**	√
Ch2	4.9	5.0	5.0	**4.7v to 5v**	√
Ch3	4.9	5.0	5.0	**4.7v to 5v**	√
Ch4	4.9	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.9	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.68	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.68	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.25	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.5	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP45P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**1.15-1.25v**	1.203	Pin 1 to Pin 2	1.203	√
2	**1.15-1.25v**	1.203	Pin 5 to Pin 6	1.203	√
3	**1.15-1.25v**	1.203	Pin 9 to Pin 10	1.203	√
4	**1.15-1.25v**	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	**0.47-0.49v**	0.478	Pin 3 to Pin 4	0.479	
2	**0.47-0.49v**	0.480	Pin 7 to Pin 8	0.481	
3	**0.47-0.49v**	0.478	Pin 11 to Pin 12	0.480	
4	**0.47-0.49v**	0.479	Pin 15 to Pin 16	0.481	

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP45P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.1	√	-17.4	√	-17.0	√	-17.2	√
-5v	-12.2	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.4	√	-2.42	√	-2.4	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.41	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.1	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP45P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

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LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

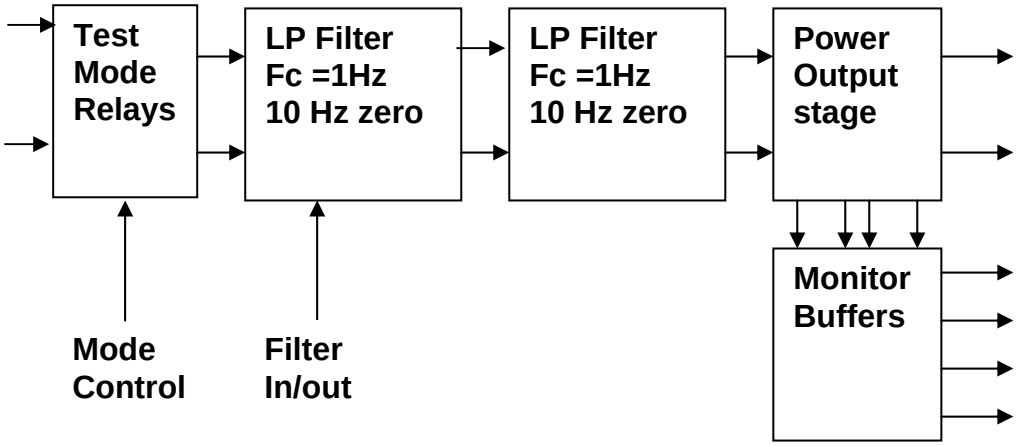
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP46P……Serial No ……
Test Engineer ….Xen……
Date ……15/12/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP46P……Serial No ……
Test Engineer ….Xen……..……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP46P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP46P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

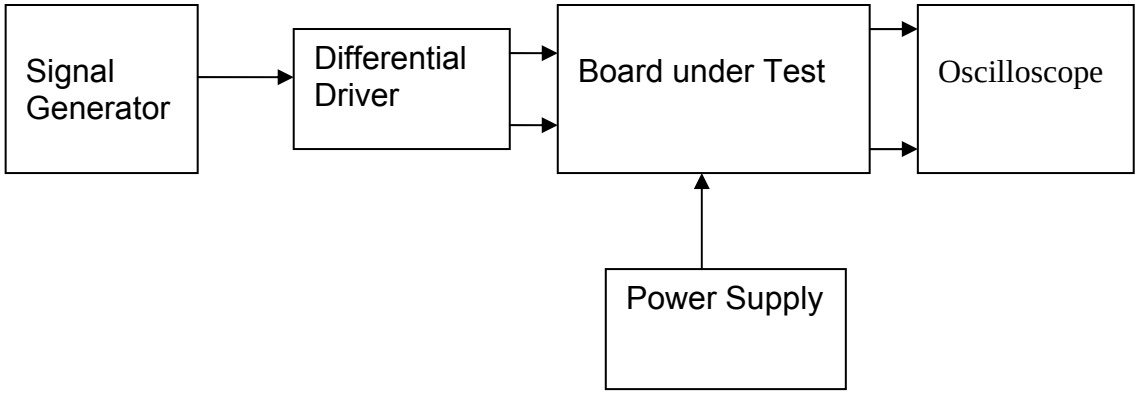
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP46P……Serial No ……
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Date ……15/12/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.07	1mV	√
+15v TP4	14.94	1mV	√
-15v TP6	-15.03	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP46P……Serial No ……
Test Engineer ….Xen……
Date ……15/12/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP46P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	**4.7v to 5v**	√
Ch2	4.9	5.0	5.0	**4.7v to 5v**	√
Ch3	4.9	5.0	5.0	**4.7v to 5v**	√
Ch4	4.9	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	**4.7 to 5v**	√
Ch2	4.9	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.68	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	**0.4v to 0.5v**	√
Ch2	0.48	**0.4v to 0.5v**	√
Ch3	0.48	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.48	**0.4v to 0.5v**	√
Ch2	0.48	**0.4v to 0.5v**	√
Ch3	0.48	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP46P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.5	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP46P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.479	
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.481	

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP46P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.2	√	-17.0	√	-17.1	√
-5v	-12.5	√	-12.5	√	-12.2	√	-12.5	√
-1v	-2.4	√	-2.42	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.4	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.1	√	17.0	√	17.1	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP46P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP47P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

Contents

1. Description

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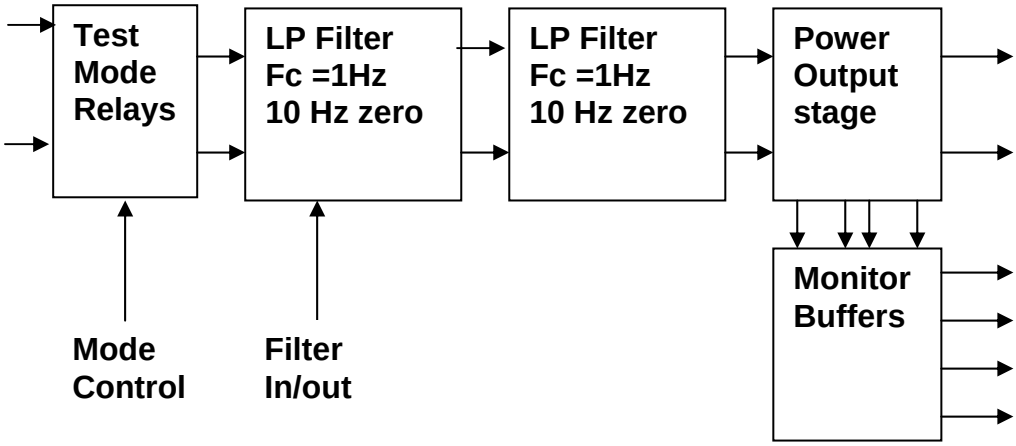

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This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP47P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
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PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

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Workmanship

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Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP47P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

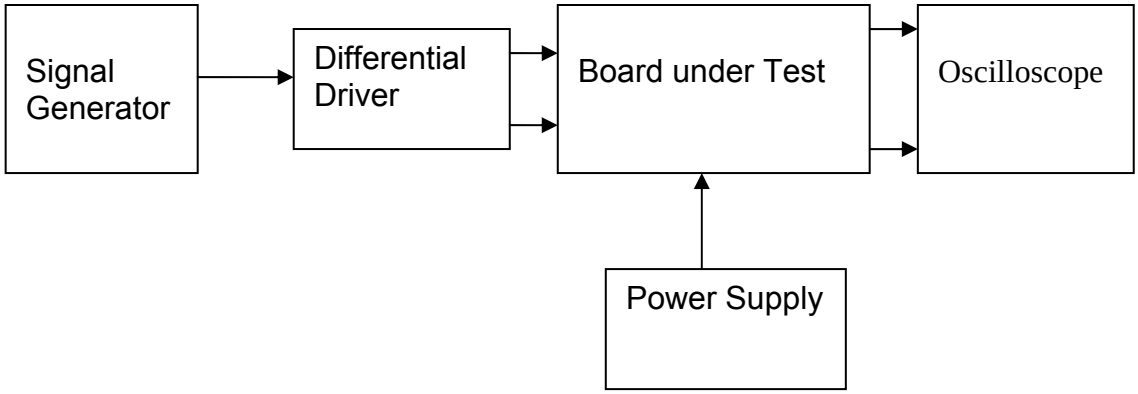
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP47P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.95	1mV	√
+15v TP4	14.79	1mV	√
-15v TP6	-15.02	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP47P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP47P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	**3.3v to 3.7v**	√
Ch2	3.35	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.68	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.48	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.48	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.48	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.5	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP47P……Serial No ……
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Date ……15/12/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.480	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.482	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.1	√	-17.0	√	-17.0	√	-17.2	√
-5v	-12.5	√	-12.2	√	-12.5	√	-12.5	√
-1v	-2.42	√	-2.41	√	-2.41	√	-2.43	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.41	√
5v	12.2	√	12.0	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.3	√	24.4	√	14.3	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

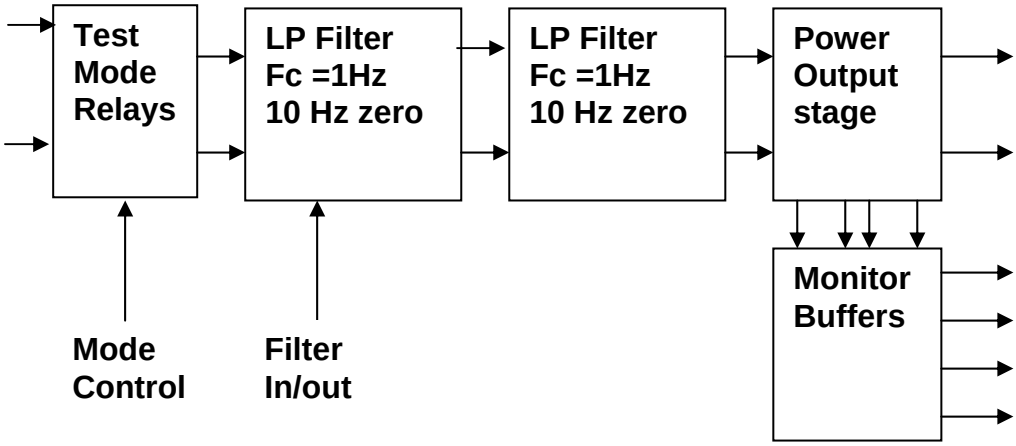
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP48P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

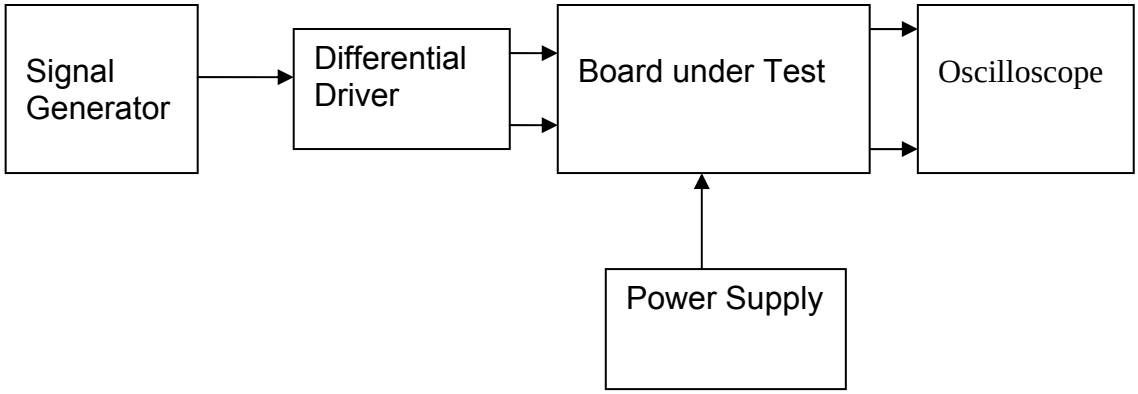
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.05	1mV	√
+15v TP4	14.95	1mV	√
-15v TP6	-15.02	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP48P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	**4.7v to 5v**	√
Ch2	4.8	5.0	5.0	**4.7v to 5v**	√
Ch3	4.8	5.0	5.0	**4.7v to 5v**	√
Ch4	4.8	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.9	**4.7 to 5v**	√
Ch3	4.9	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.68	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP48P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.25	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.49	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.202	Pin 9 to Pin 10	1.202	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.479	Pin 11 to Pin 12	0.481	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP48P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.1	√	-17.1	√	-17.1	√	-17.1	√
-5v	-12.4	√	-12.3	√	-12.4	√	-12.4	√
-1v	-2.4	√	-2.41	√	-2.41	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.4	√	2.4	√	2.42	√
5v	12.2	√	12.2	√	12.0	√	12.1	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.4	√	24.4	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP48P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

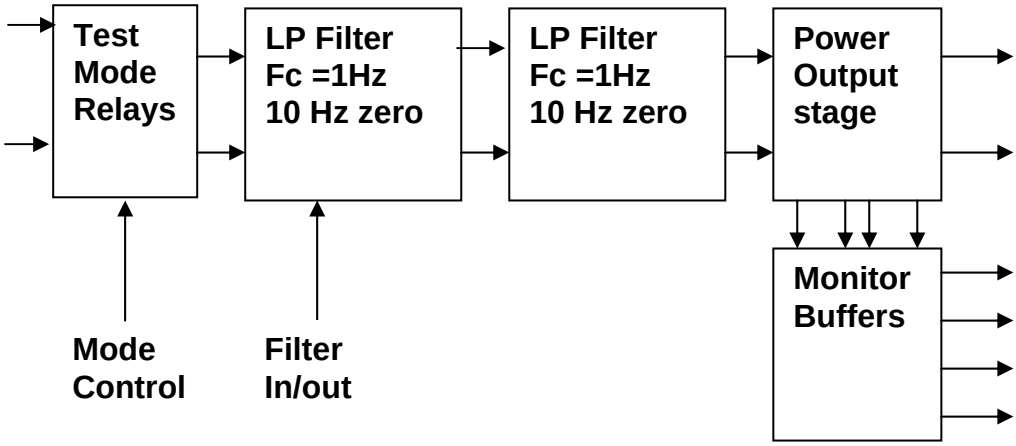
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP49P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP49P……Serial No ……
Test Engineer ….Xen……..……
Date ……16/12/09……..……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP49P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP49P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

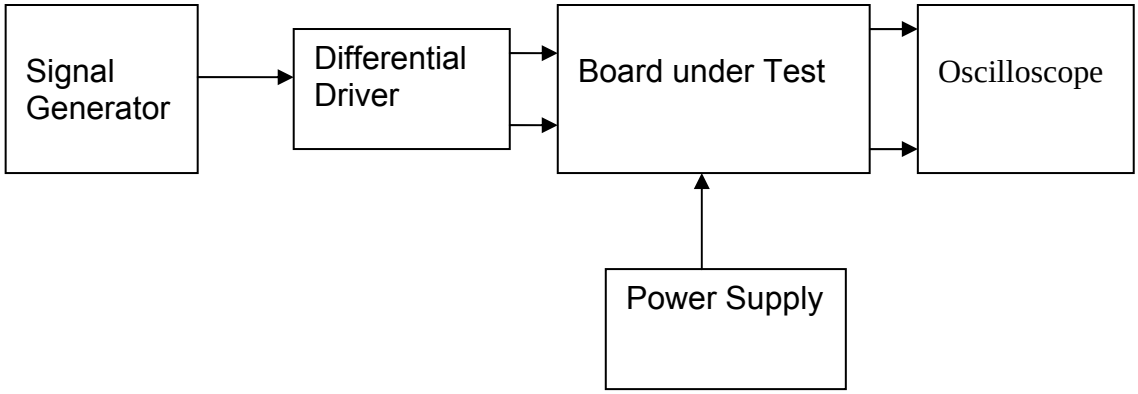
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP49P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.93	1mV	√
+15v TP4	14.95	1mV	√
-15v TP6	-14.97	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP49P……Serial No ……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP49P……Serial No ……
Test Engineer ….Xen……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.9	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP49P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.25	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.5	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP49P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.481	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.486	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.1	√	-12.2	√	-17.1	√	-17.1	√
-5v	-12.4	√	-12.4	√	-12.4	√	-12.3	√
-1v	-2.4	√	-2.42	√	-2.41	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.41	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.1	√	17.1	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP49P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.45	
Ch2	**3.3-3.5v**	3.45	
Ch3	**3.3-3.5v**	3.44	
Ch4	**3.3-3.5v**	3.44	

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

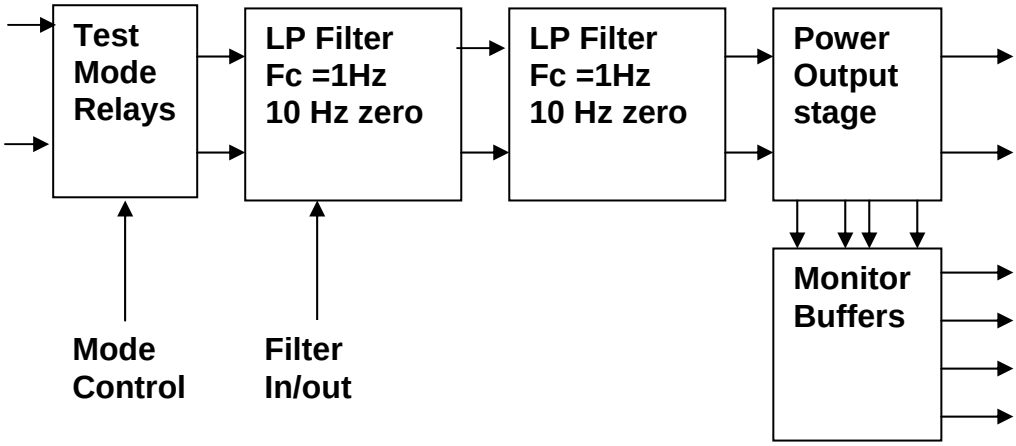
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP50P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

Contents

1. Description

Block diagram



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The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP50P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
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V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit……T_TOP50P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP50P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

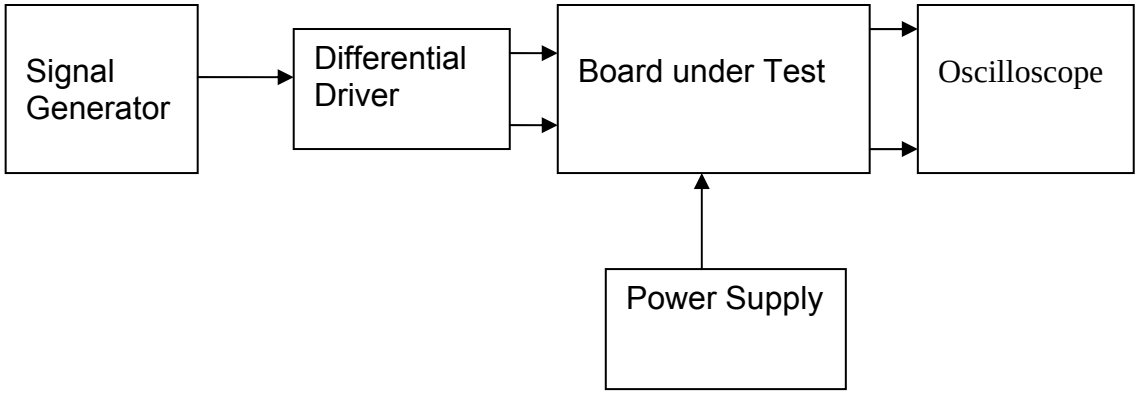
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP50P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.06	1mV	√
+15v TP4	14.94	1mV	√
-15v TP6	-14.95	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP50P……Serial No ……
Test Engineer ….Xen……
Date ……16/12/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP50P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP50P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.25	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.25	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP50P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.479	Pin 11 to Pin 12	0.481	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.480	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP50P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.1	√	-17.0	√	-17.0	√
-5v	-12.5	√	-12.5	√	-12.2	√	-12.2	√
-1v	-2.41	√	-2.42	√	-2.4	√	-2.41	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.42	√	2.42	√	2.41	√
5v	12.1	√	12.1	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……T_TOP50P……Serial No ……
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Date ……17/12/09……

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2	-143dB	-114dB	229Hz
Channel 2	Channel 1	-143dB	-115dB	275Hz
Channel 2	Channel 3	-139dB	-114dB	316Hz
Channel 3	Channel 2	-137dB	-116dB	240Hz
Channel 3	Channel 4	-158dB	-115dB	724Hz
Channel 4	Channel 3	-138dB	-113dB	871Hz

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

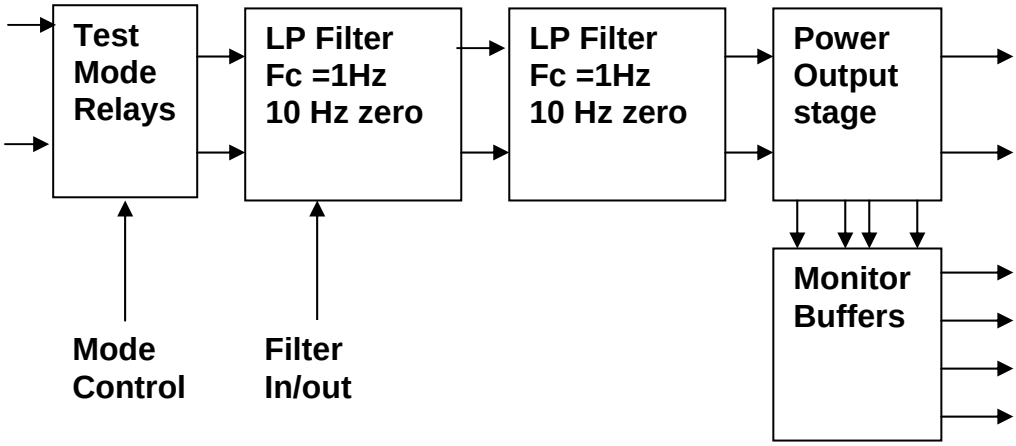
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP51P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP51P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

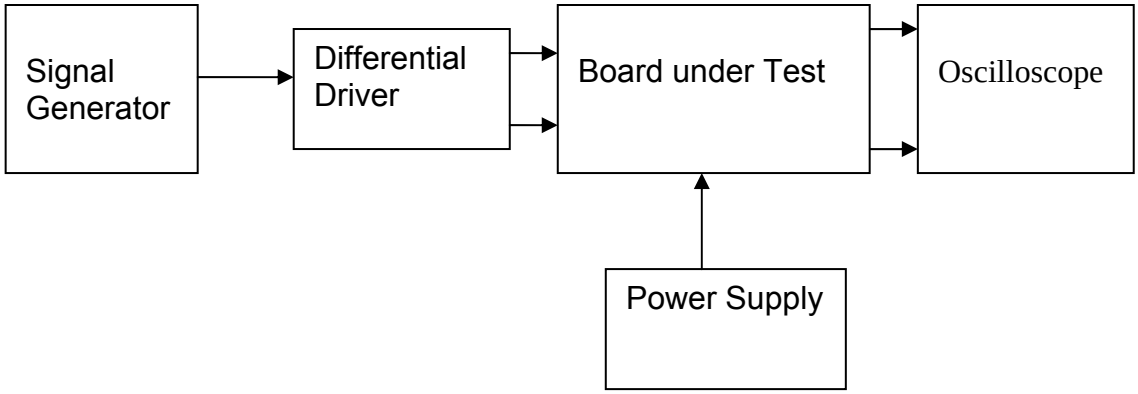
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP51P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.95	1mV	√
+15v TP4	14.94	1mV	√
-15v TP6	-15.04	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP51P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP51P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	**4.7v to 5v**	√
Ch2	4.9	5.0	5.0	**4.7v to 5v**	√
Ch3	4.9	5.0	5.0	**4.7v to 5v**	√
Ch4	4.9	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.9	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP51P……Serial No ……
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Date ……17/12/09……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.25	3v to 3.4v	√
Ch4	3.25	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP51P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.482	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP51P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.2	√	-17.2	√	-17.0	√
-5v	-12.4	√	-12.5	√	-12.5	√	-12.2	√
-1v	-2.4	√	-2.42	√	-2.42	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.41	√	2.42	√	2.41	√	2.41	√
5v	12.2	√	12.2	√	12.1	√	12.2	√
7v	17.0	√	17.1	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP51P……Serial No ……
Test Engineer ….Xen……
Date ……17/12/09……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

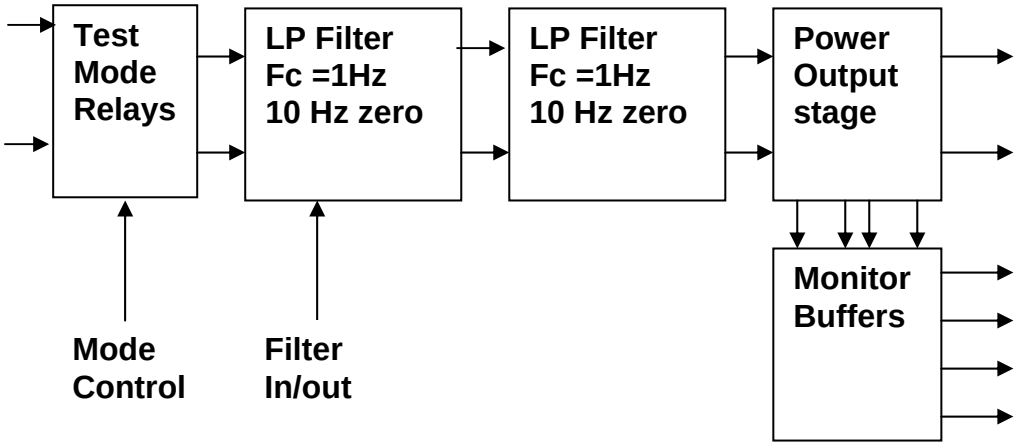
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP52P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP52P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP52P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP52P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

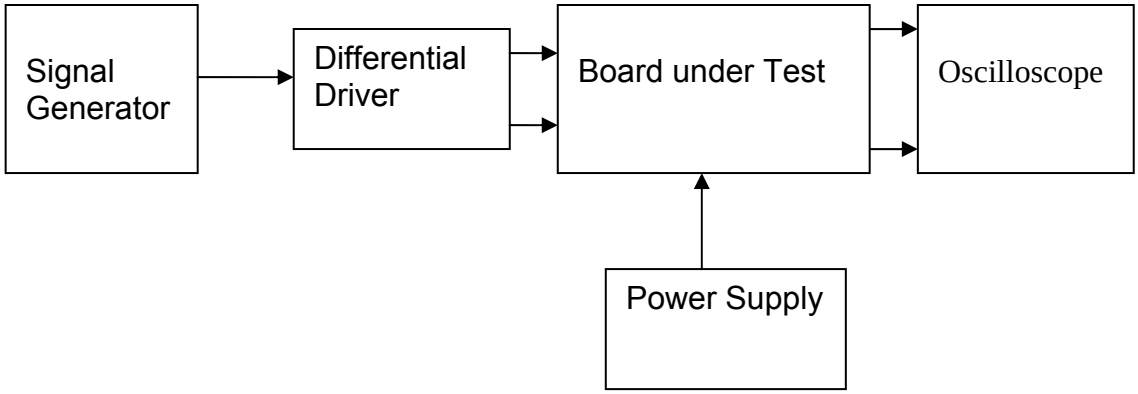
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP52P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.96	1mV	√
+15v TP4	14.88	1mV	√
-15v TP6	-15.10	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP52P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	**4.7v to 5v**	√
Ch2	4.9	5.0	5.0	**4.7v to 5v**	√
Ch3	4.9	5.0	5.0	**4.7v to 5v**	√
Ch4	4.9	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.9	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.35	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.68	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.5	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP52P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.479	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP52P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.1	√	-17.0	√	-17.1	√
-5v	-12.5	√	-12.4	√	-12.3	√	-12.3	√
-1v	-2.41	√	-2.41	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.41	√	2.41	√	2.41	√	2.42	√
5v	12.1	√	12.1	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.1	√	17.1	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……Serial No ……
Test Engineer …….
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The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP52P……Serial No ……
Test Engineer ….Xen……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
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Ch3	**3.3-3.5v**	3.44	√
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Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

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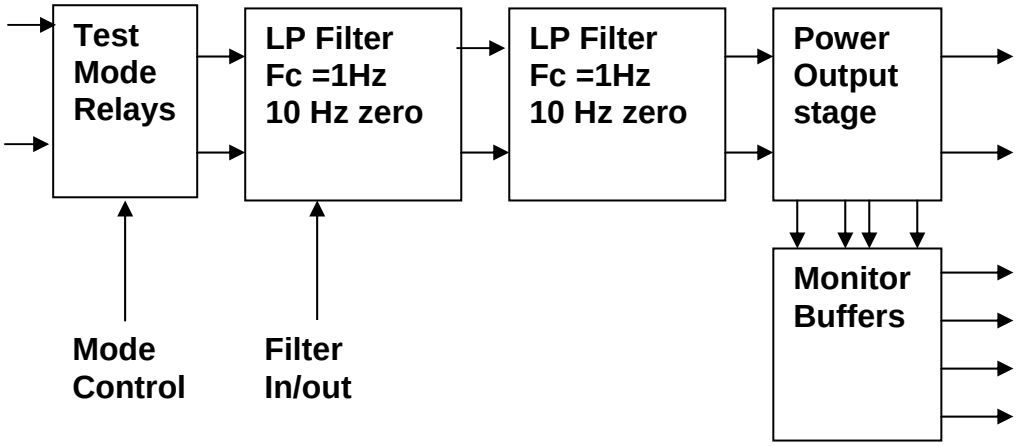

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PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP53P……Serial No ……
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Workmanship

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Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP53P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

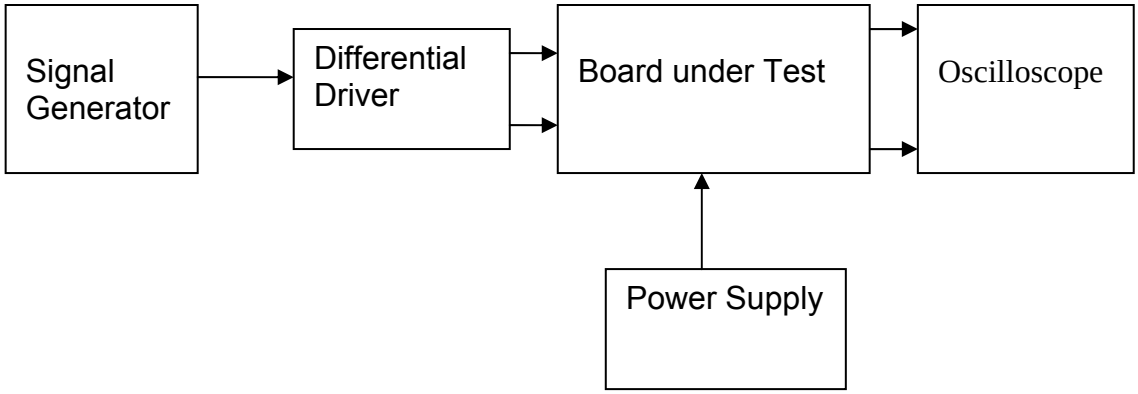
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP53P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.07	1mV	√
+15v TP4	14.94	1mV	√
-15v TP6	-15.06	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	350mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP53P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP53P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	**4.7v to 5v**	√
Ch2	4.9	5.0	5.0	**4.7v to 5v**	√
Ch3	4.9	5.0	5.0	**4.7v to 5v**	√
Ch4	4.9	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.9	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP53P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……..……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.5	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP53P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.480	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.479	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP53P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.2	√	-17.2	√	-17.1	√
-5v	-12.4	√	-12.3	√	-12.3	√	-12.3	√
-1v	-2.42	√	-2.41	√	-2.42	√	2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.41	√	2.4	√	2.42	√	2.41	√
5v	12.2	√	12.0	√	12.2	√	12.1	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.3	√	24.4	√	24.4	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP53P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.z

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

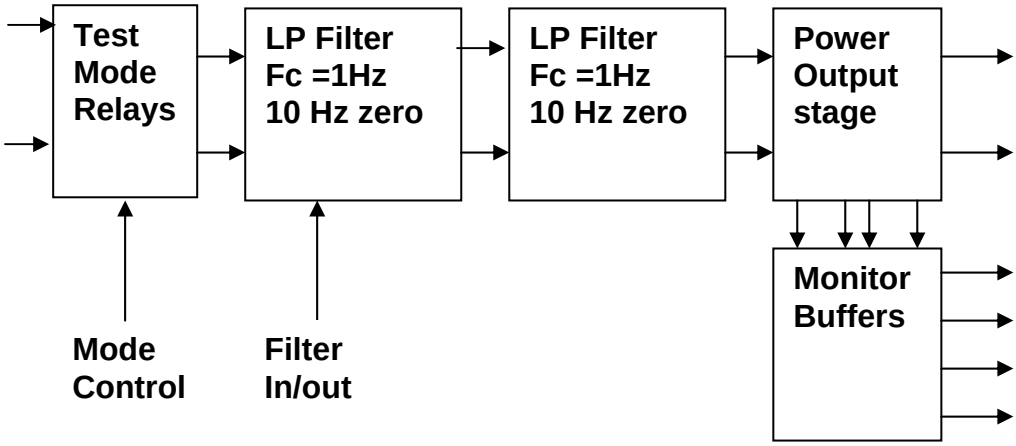
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

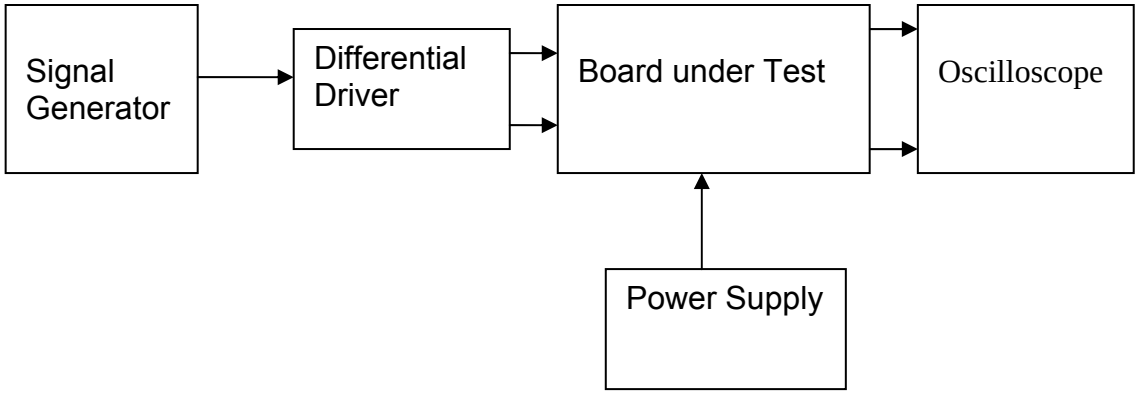
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.96	1mV	√
+15v TP4	14.91	1mV	√
-15v TP6	-14.91	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	**4.7v to 5v**	√
Ch2	4.9	5.0	5.0	**4.7v to 5v**	√
Ch3	4.9	5.0	5.0	**4.7v to 5v**	√
Ch4	4.9	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.49	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.477	Pin 3 to Pin 4	0.478	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.479	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.480	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.1	√	-17.1	√	-17.2	√
-5v	-12.3	√	-12.3	√	-12.3	√	-12.5	√
-1v	-2.42	√	-2.41	√	-2.41	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.1	√
7v	17.1	√	17.0	√	17.1	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.3	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP54P……Serial No ……
Test Engineer ….Xen……
Date ……4/1/10……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.42	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

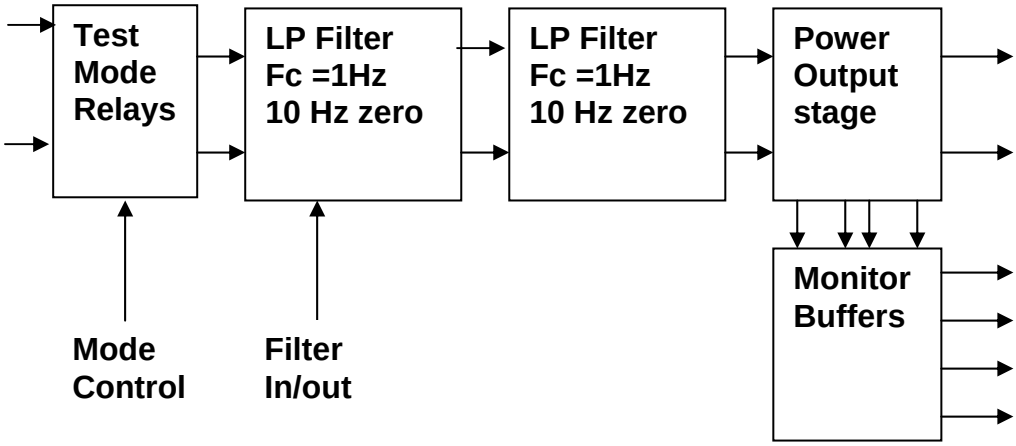
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP55P……Serial No ……
Test Engineer ….Xen……..……
Date ……5/1/10……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP55P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP55P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP55P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

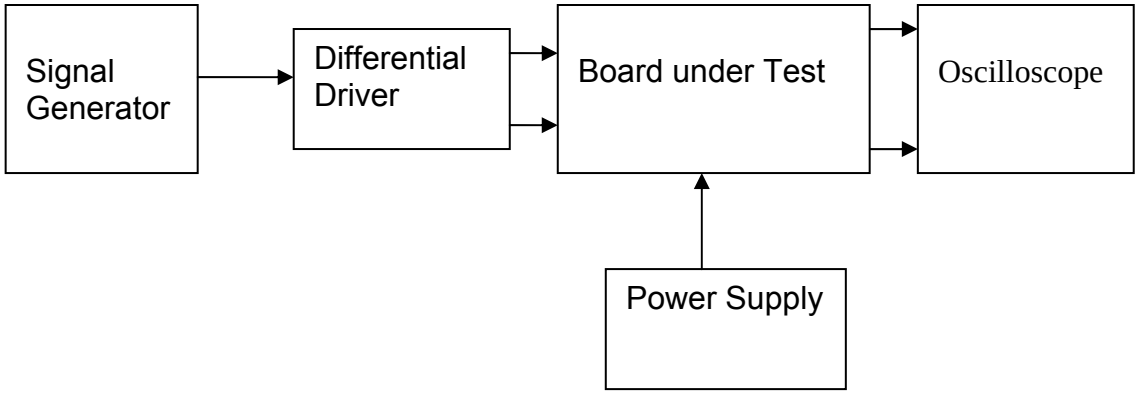
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP55P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.04	1mV	√
+15v TP4	14.92	1mV	√
-15v TP6	-15.00	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP55P……Serial No ……
Test Engineer ….Xen……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP55P……Serial No ……
Test Engineer ….Xen……
Date ……5/1/10……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	**4.7v to 5v**	√
Ch2	4.8	5.0	5.0	**4.7v to 5v**	√
Ch3	4.8	5.0	5.0	**4.7v to 5v**	√
Ch4	4.8	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP55P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.15	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP55P……Serial No ……
Test Engineer ….Xen……
Date ……5/1/10……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.495	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.485	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP55P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.1	√	-17.3	√	-17.2	√	-17.2	√
-5v	-12.3	√	-12.3	√	-12.3	√	-12.3	√
-1v	-2.4	√	-2.42	√	-2.41	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.41	√	2.42	√	2.42	√	2.41	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.1	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.3	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP55P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.41	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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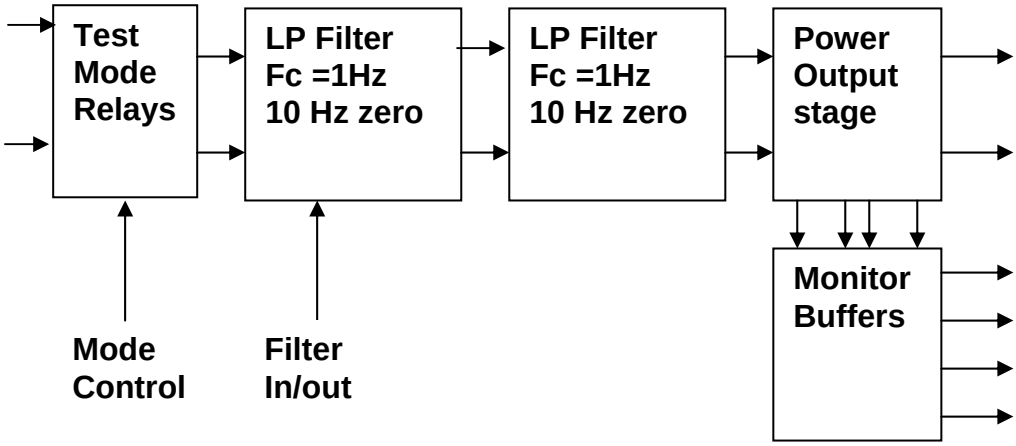
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……..……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……..……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date ……5/1/10……..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

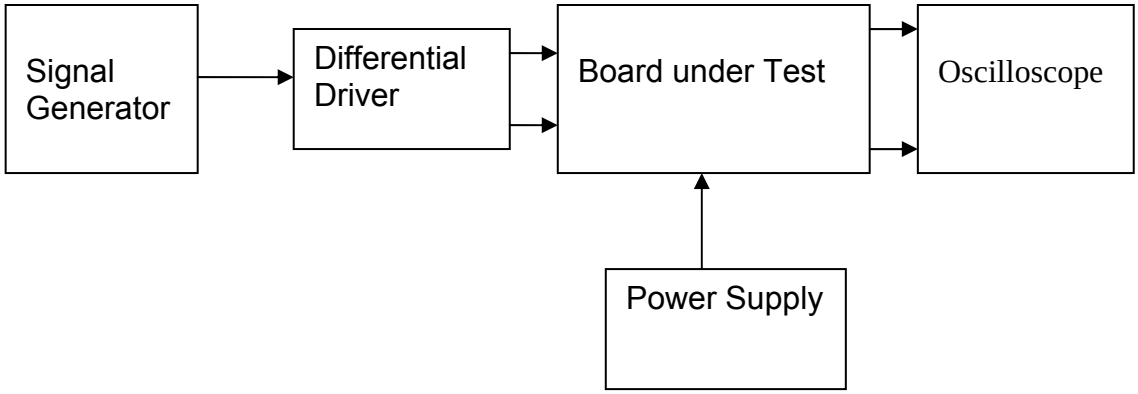
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.08	1mV	√
+15v TP4	14.91	1mV	√
-15v TP6	-15.05	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	**3.3v to 3.7v**	√
Ch2	3.35	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……..……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……..

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.204	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.204	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.477	Pin 11 to Pin 12	0.478	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……..……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.1	√	-17.2	√	-17.2	√
-5v	-12.3	√	-12.3	√	-12.4	√	-12.3	√
-1v	-2.42	√	-2.4	√	-2.42	√	-2.41	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.1	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.4	√	24.5	√	24.3	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP56P……Serial No ……
Test Engineer ….Xen……
Date …….5/1/10……..……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

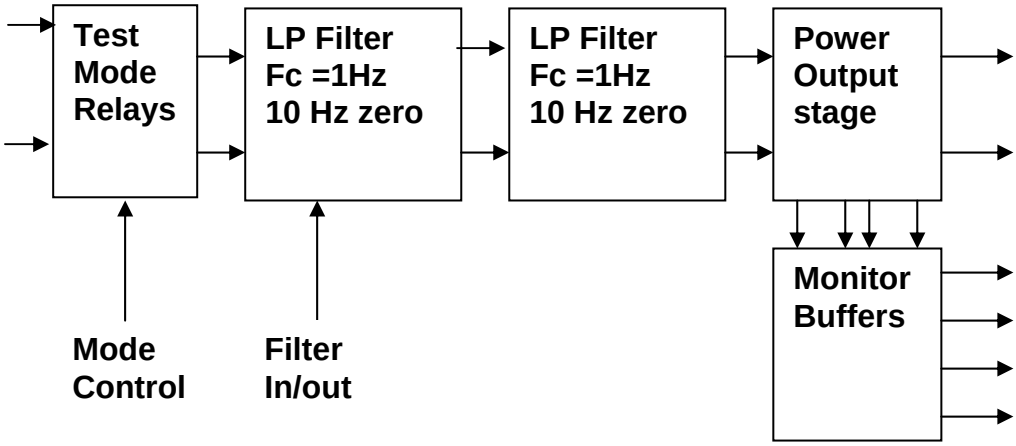
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP57P……Serial No ……
Test Engineer ….Xen……
Date ……6/1/10……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

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This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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Test Engineer ….Xen……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
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Analogue oscilloscope
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Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
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V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP57P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP57P……Serial No ……
Test Engineer ….Xen……
Date ……6/1/10……..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

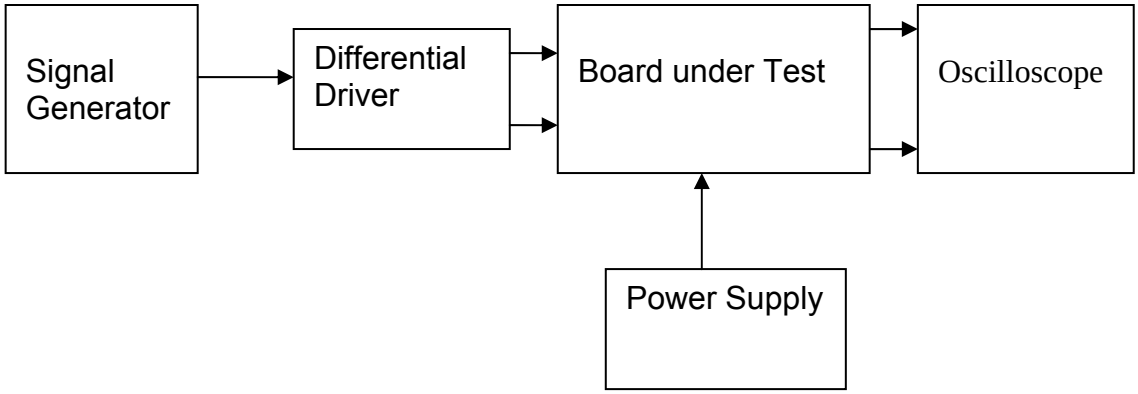
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP57P……Serial No ……
Test Engineer ….Xen……
Date …….6/1/10……..

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.00	1mV	√
+15v TP4	14.90	1mV	√
-15v TP6	-15.06	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP57P……Serial No ……
Test Engineer ….Xen……
Date ……6/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP57P……Serial No ……
Test Engineer ….Xen……
Date ……6/1/10……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	**3.3v to 3.7v**	√
Ch2	3.35	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP57P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.15	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP57P……Serial No ……
Test Engineer ….Xen……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.482	√
2	0.47-0.49v	0.480	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.479	Pin 11 to Pin 12	0.481	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP57P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.4	√
-7v	-17.2	√	-17.2	√	-17.2	√	-17.1	√
-5v	-12.3	√	-12.3	√	-12.4	√	-12.3	√
-1v	-2.4	√	-2.41	√	-2.42	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.1	√	17.0	√	17.0	√
10v	24.4	√	24.4	√	24.4	√	24.4	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP57P……Serial No ……
Test Engineer ….Xen……
Date …….6/1/10……..……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

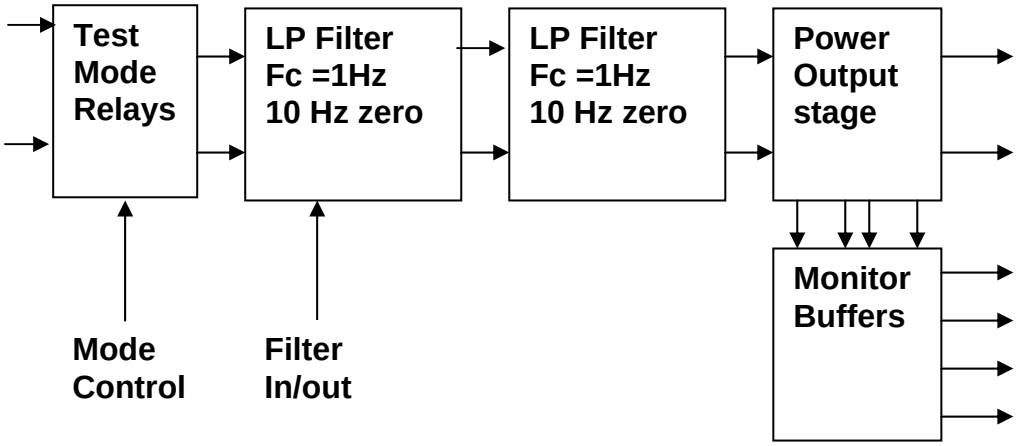
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP58P……Serial No ……
Test Engineer ….Xen……
Date ……6/1/10……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP58P……Serial No ……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

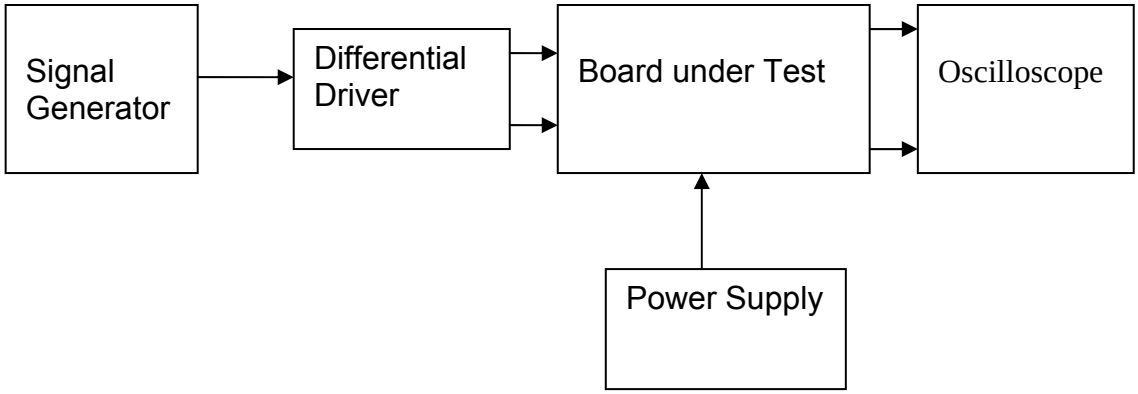
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.09	1mV	√
+15v TP4	14.82	1mV	√
-15v TP6	-15.00	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP58P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.35	**3.3v to 3.7v**	√
Ch3	3.35	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.68	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP58P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP58P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.477	Pin 3 to Pin 4	0.479	√
2	0.47-0.49v	0.478	Pin 7 to Pin 8	0.479	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.480	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP58P……Serial No ……
Test Engineer ….Xen……
Date …….6/1/10……..

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.2	√	-17.2	√	-17.1	√
-5v	-12.3	√	-12.3	√	-12.3	√	-12.2	√
-1v	-2.41	√	-2.42	√	-2.41	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.4	√	24.3	√	24.4	√	24.4	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP58P……Serial No ……
Test Engineer ….Xen……
Date …….6/1/10……..……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.42	√
Ch2	**3.3-3.5v**	3.43	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

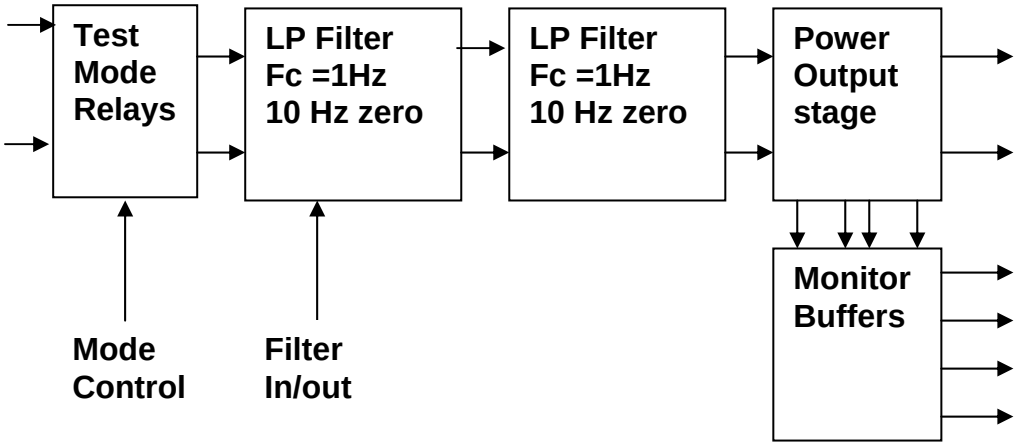
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP59P……Serial No ……
Test Engineer ….Xen……
Date ……7/1/10……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP59P……Serial No ……
Test Engineer ….Xen……
Date ……7/1/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP59P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP59P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

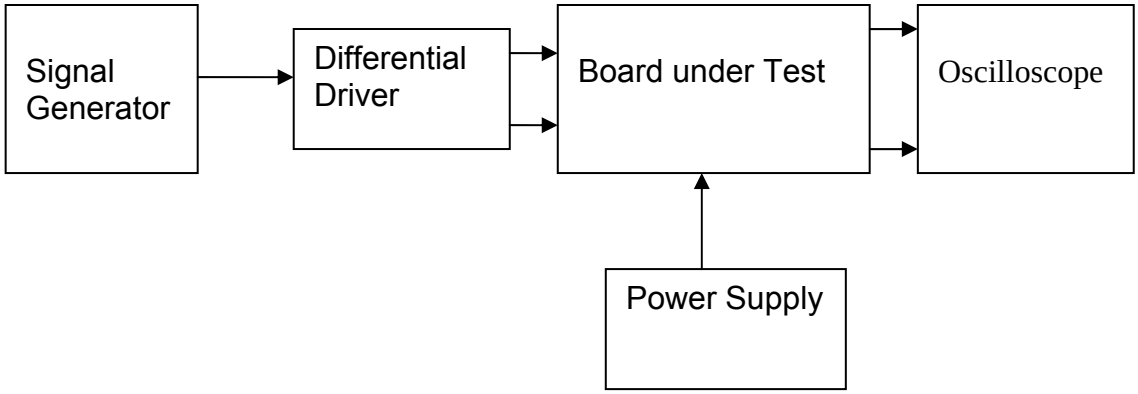
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP59P……Serial No ……
Test Engineer ….Xen……
Date …….6/1/10……..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.99	1mV	√
+15v TP4	14.88	1mV	√
-15v TP6	-14.90	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP59P……Serial No ……
Test Engineer ….Xen……
Date ……6/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP59P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.35	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.68	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP59P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP59P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.482	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP59P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.0	√	-17.2	√	-17.2	√	-17.2	√
-5v	-12.3	√	-12.3	√	-12.3	√	-12.3	√
-1v	-2.4	√	-2.42	√	-2.42	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.41	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.3	√	24.3	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP59P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

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http://www.physics.gla.ac.uk/igr/sus/

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

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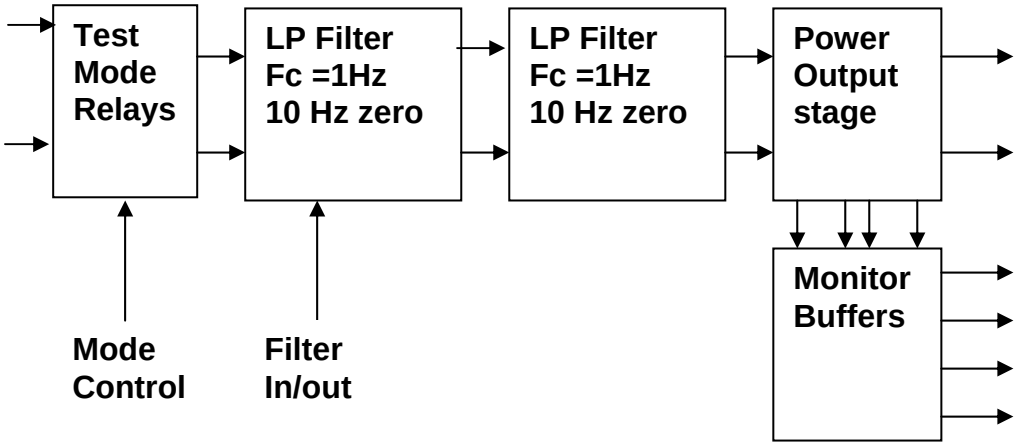

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Workmanship

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4. Continuity Checks

J2

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1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

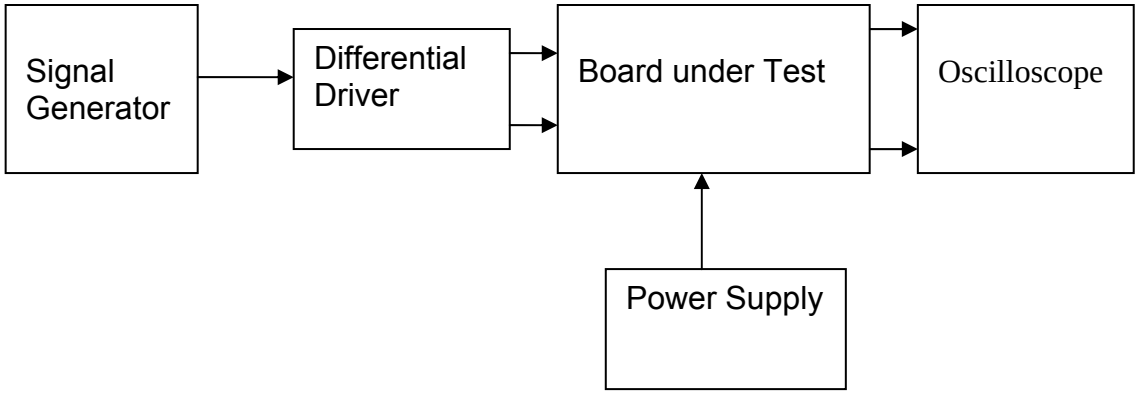
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.10	1mV	√
+15v TP4	14.79	1mV	√
-15v TP6	-15.02	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP60P……Serial No ……
Test Engineer ….Xen……
Date ……7/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP60P……Serial No ……
Test Engineer ….Xen……
Date ……7/1/10……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.9	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.68	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP60P……Serial No ……
Test Engineer ….Xen……
Date ……7/1/10……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.25	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.25	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP60P……Serial No ……
Test Engineer ….Xen……
Date ……7/1/10……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.484	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP60P……Serial No ……
Test Engineer ….Xen……
Date ……7/1/10……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.2	√	-17.2	√	-17.2	√
-5v	-12.3	√	-12.3	√	-12.3	√	-12.3	√
-1v	-2.42	√	-2.41	√	-2.41	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.41	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.1	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.4	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

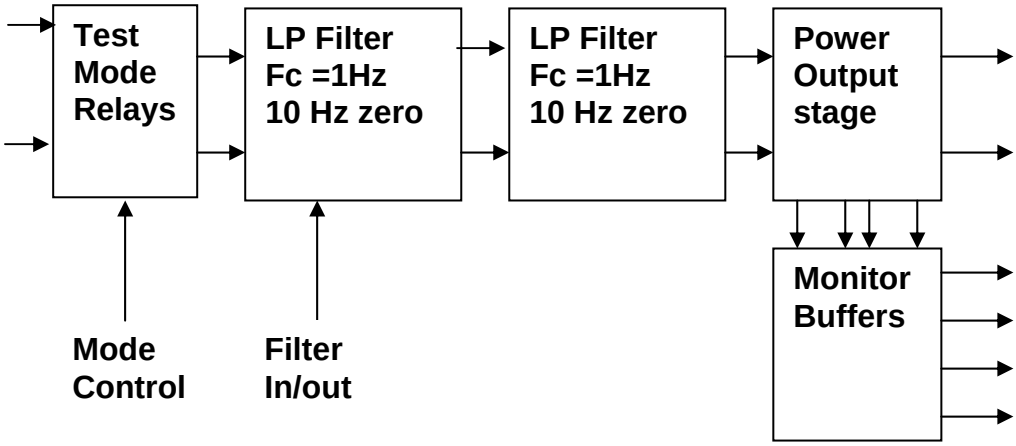
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP61P……Serial No ……
Test Engineer ….Xen……
Date …….8/1/10……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP61P……Serial No ……
Test Engineer ….Xen……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP61P……Serial No ……
Test Engineer ….Xen……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP61P……Serial No ……
Test Engineer ….Xen……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

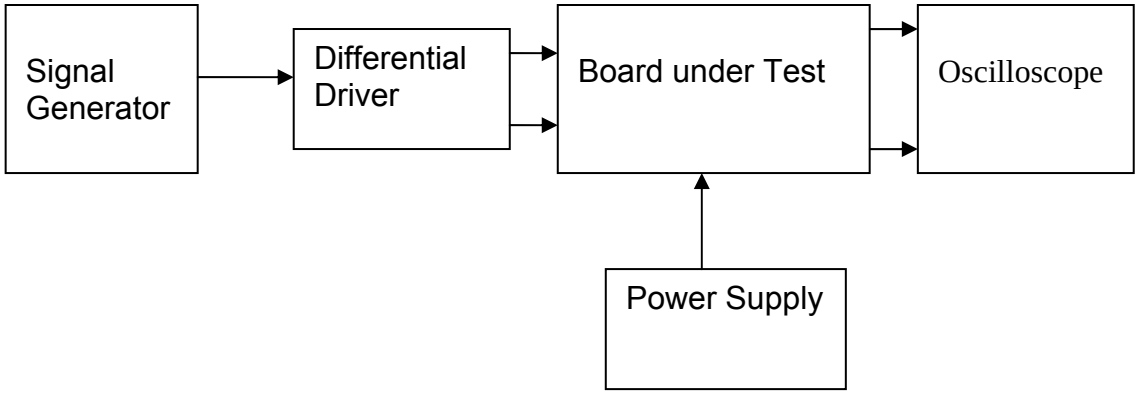
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP61P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.04	1mV	√
+15v TP4	14.91	1mV	√
-15v TP6	-14.99	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP61P……Serial No ……
Test Engineer ….Xen……
Date ……7/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP61P……Serial No ……
Test Engineer ….Xen……
Date ……8/1/10……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP61P……Serial No ……
Test Engineer ….Xen……
Date ……8/1/10……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.15	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.5	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP61P……Serial No ……
Test Engineer ….Xen……
Date ……8/1/10……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.477	Pin 11 to Pin 12	0.479	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP61P……Serial No ……
Test Engineer ….Xen……
Date ……8/1/10……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.0	√	-17.2	√	-17.2	√	-17.2	√
-5v	-12.2	√	-12.5	√	-12.3	√	-12.3	√
-1v	-2.4	√	-2.42	√	-2.42	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.1	√	17.0	√	17.0	√	17.1	√
10v	24.5	√	24.4	√	24.4	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP61P……Serial No ……
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Date …….8/1/10……..……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

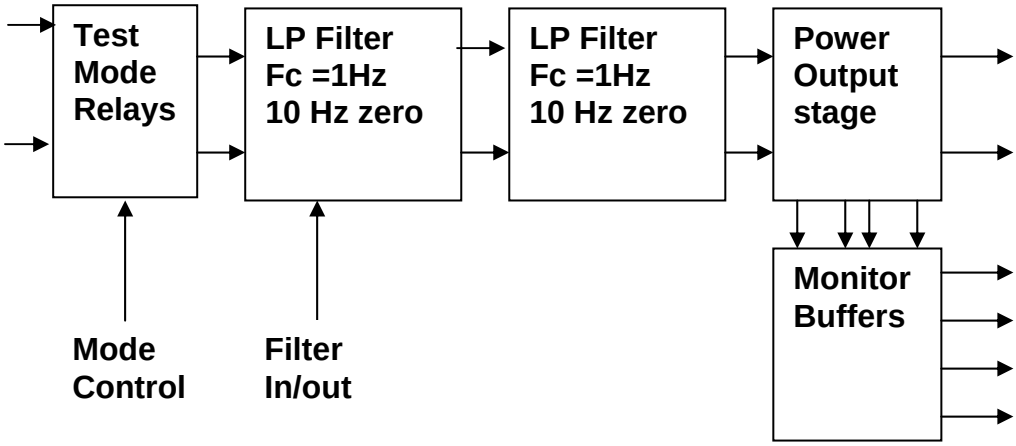
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP62P……Serial No ……
Test Engineer ….Xen……
Date ……8/1/10……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP62P……Serial No ……
Test Engineer ….Xen……
Date …….8/1/10……..……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP62P……Serial No ……
Test Engineer ….Xen……
Date …….8/1/10……..……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP62P……Serial No ……
Test Engineer ….Xen……
Date ……8/1/10……..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

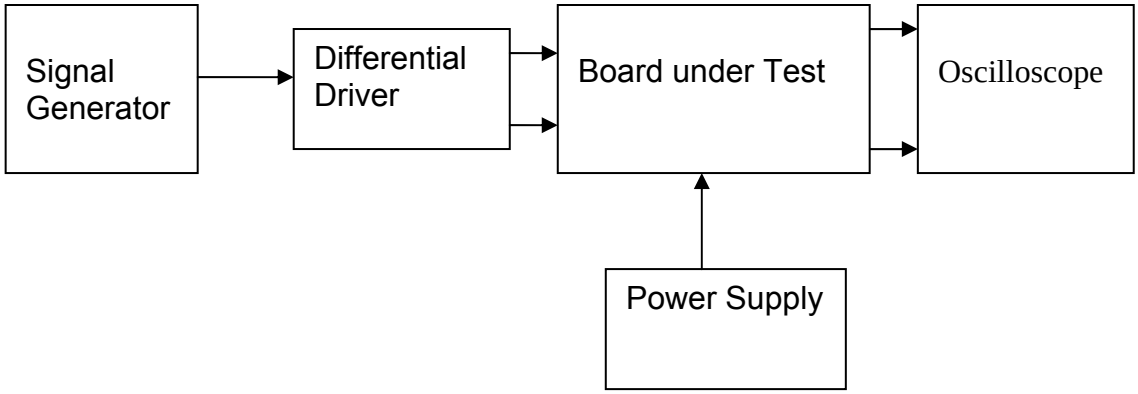
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP62P……Serial No ……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.08	1mV	√
+15v TP4	14.94	1mV	√
-15v TP6	-15.04	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP62P……Serial No ……
Test Engineer ….Xen……
Date ……8/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP62P……Serial No ……
Test Engineer ….Xen……
Date ……8/1/10……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.35	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.68	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP62P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP62P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.204	Pin 1 to Pin 2	1.204	√
2	1.15-1.25v	1.204	Pin 5 to Pin 6	1.204	√
3	1.15-1.25v	1.204	Pin 9 to Pin 10	1.204	√
4	1.15-1.25v	1.204	Pin 13 to Pin 14	1.204	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.477	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.477	Pin 11 to Pin 12	0.479	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.480	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP62P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.4	√	-24.4	√	-24.4	√	-24.5	√
-7v	-17.0	√	-17.0	√	-17.2	√	-17.1	√
-5v	-12.2	√	-12.2	√	-12.3	√	-12.3	√
-1v	-2.41	√	-2.4	√	-2.42	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.41	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.4	√	24.4	√	24.4	√	24.4	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP62P……Serial No ……
Test Engineer ….Xen……
Date ……8/1/10……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.42	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.42	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

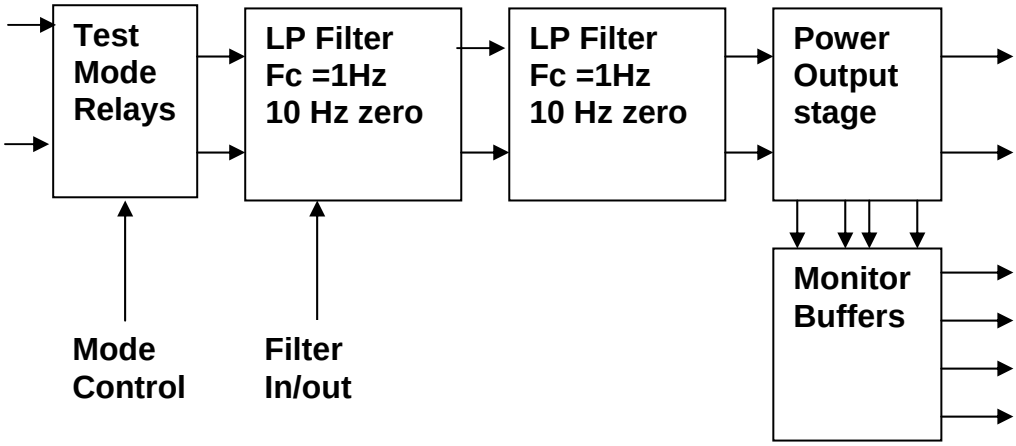
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP63P……Serial No ……
Test Engineer ….Xen……..……
Date ……11/1/10……..……

Contents

1. Description

Block diagram



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The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

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Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

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V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP63P……Serial No ……
Test Engineer ….Xen……..……
Date ……11/1/10……..……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP63P……Serial No ……
Test Engineer ….Xen……..……
Date ……11/1/10……..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

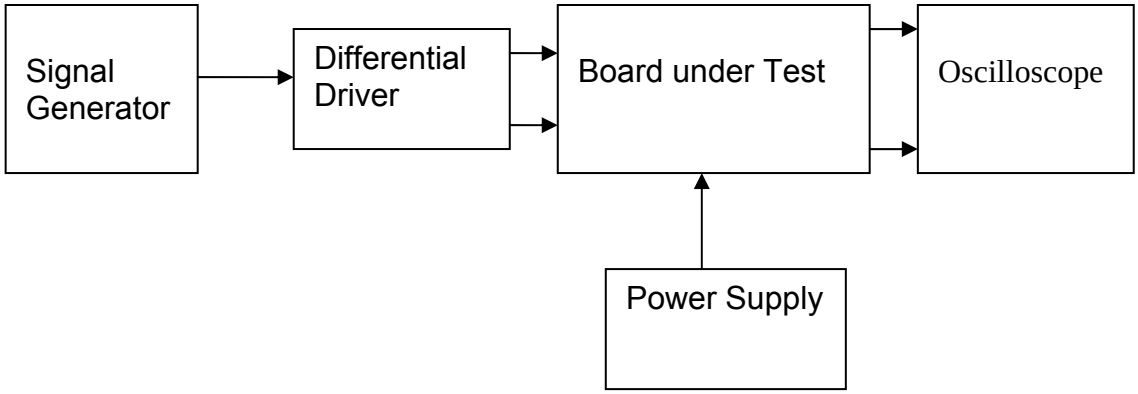
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP63P……Serial No ……
Test Engineer ….Xen……..……
Date ……11/1/10……..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.06	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-15.03	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP63P……Serial No ……
Test Engineer ….Xen……..……
Date ……11/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP63P……Serial No ……
Test Engineer ….Xen……..……
Date ……11/1/10……..……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.35	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.66	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP63P……Serial No ……
Test Engineer ….Xen……..……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.15	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.15	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.46	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP63P……Serial No ……
Test Engineer ….Xen……..……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.205	Pin 1 to Pin 2	1.204	√
2	1.15-1.25v	1.205	Pin 5 to Pin 6	1.204	√
3	1.15-1.25v	1.204	Pin 9 to Pin 10	1.204	√
4	1.15-1.25v	1.204	Pin 13 to Pin 14	1.204	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.483	√
2	0.47-0.49v	0.480	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.480	Pin 15 to Pin 16	0.483	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP63P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.4	√	-24.4	√
-7v	-17.2	√	-17.1	√	-17.0	√	-17.2	√
-5v	-12.3	√	-12.3	√	-12.3	√	-12.3	√
-1v	-2.41	√	-2.41	√	-2.41	√	-2.41	√
0v	0	√	0	√	0	√	0	√
1v	2.41	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.1	√
10v	24.3	√	24.3	√	24.3	√	24.3	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.42	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.44	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v1 Advanced LIGO UK 6 May 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

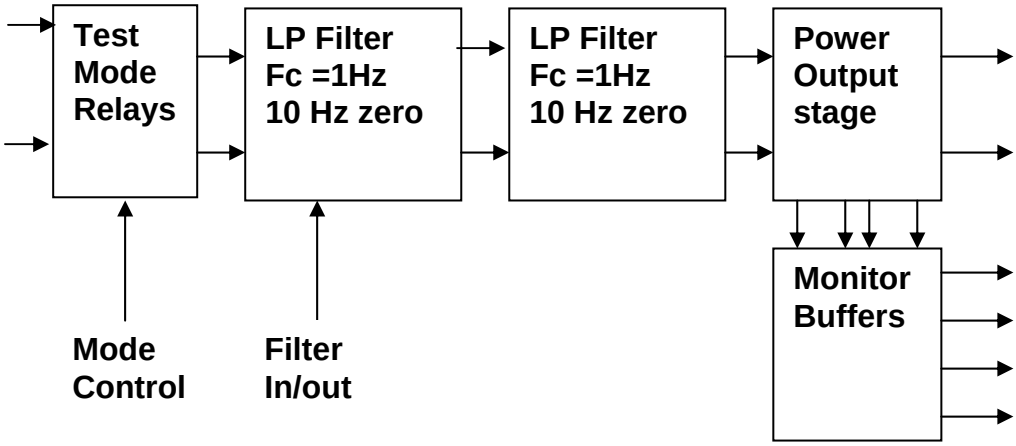
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP64P……Serial No ……
Test Engineer …..Xen……
Date ……..12/1/10……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP64P……Serial No ……
Test Engineer …..Xen……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP64P……Serial No ……
Test Engineer …..Xen……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Changed IC8 and also IC11 due to distortion on CH3.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP64P……Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

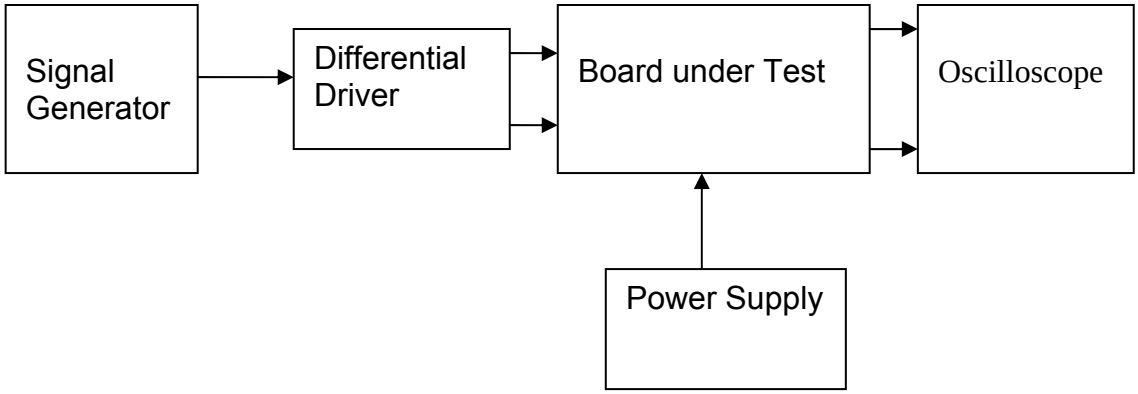
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP64P……Serial No ……
Test Engineer …..Xen……
Date ……..12/1/10……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.11	1mV	√
+15v TP4	14.97	1mV	√
-15v TP6	-14.96	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP64P……Serial No ……
Test Engineer …..Xen……
Date ……..12/1/10……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP64P……Serial No ……
Test Engineer …..Xen……
Date ……..12/1/10……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	**4.7 to 5v**	√
Ch2	4.8	**4.7 to 5v**	√
Ch3	4.8	**4.7 to 5v**	√
Ch4	4.8	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	**3.3v to 3.7v**	√
Ch2	3.3	**3.3v to 3.7v**	√
Ch3	3.3	**3.3v to 3.7v**	√
Ch4	3.3	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.65	**0.48 to 0.75v**	√
Ch2	0.66	**0.48 to 0.75v**	√
Ch3	0.65	**0.48 to 0.75v**	√
Ch4	0.66	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.46	**0.4v to 0.5v**	√
Ch2	0.46	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.46	**0.4v to 0.5v**	√

Unit……T_TOP64P……Serial No ……
Test Engineer …..Xen……
Date ……..12/1/10……..……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.8	4.7v to 5v	√
Ch2	4.8	4.7v to 5v	√
Ch3	4.8	4.7v to 5v	√
Ch4	4.8	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.1	3v to 3.4v	√
Ch4	3.1	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.46	0.4v to 0.5v	√
Ch3	0.45	0.4v to 0.5v	√
Ch4	0.45	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP64P……Serial No ……
Test Engineer …..Xen……
Date ……..12/1/10……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.202	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.480	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP64P……Serial No ……
Test Engineer …..Xen……
Date ……..12/1/10……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.2	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.0	√	-17.2	√	-17.1	√	-17.1	√
-5v	-12.0	√	-12.5	√	-12.3	√	-12.3	√
-1v	-2.4	√	-2.43	√	-2.42	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.42	√	2.41	√	2.42	√
5v	12.0	√	12.2	√	12.0	√	12.2	√
7v	16.9	√	17.0	√	17.0	√	17.0	√
10v	24.1	√	24.2	√	24.2	√	24.3	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……T_TOP64P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

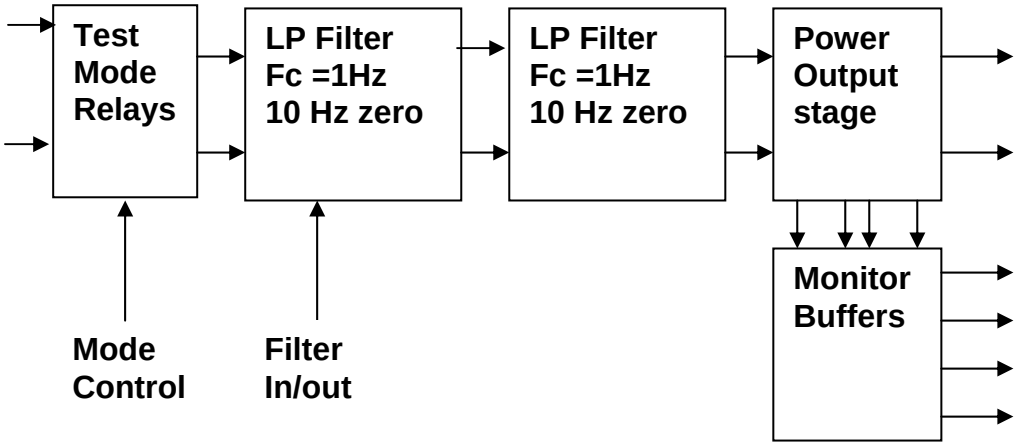
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP65P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP65P……Serial No ……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

U1 has been replaced.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

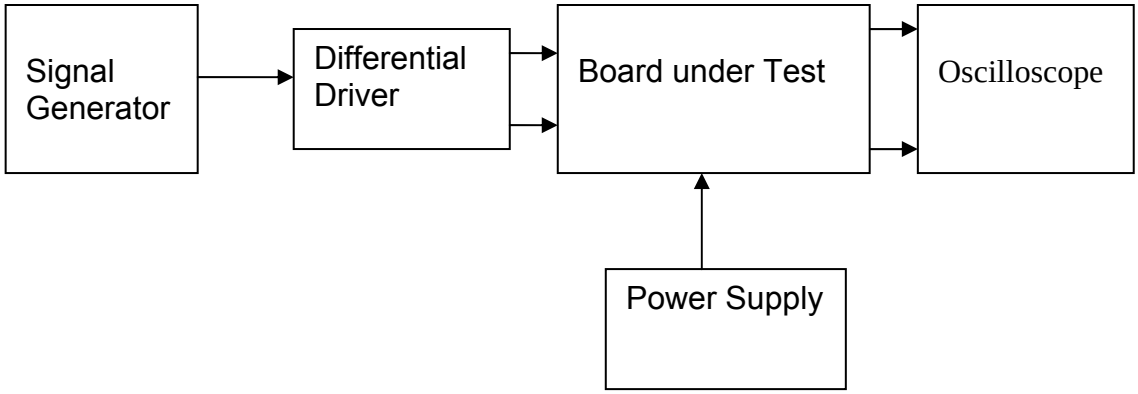
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.05	1mV	√
+15v TP4	14.76	1mV	√
-15v TP6	-15.06	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP65P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.35	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.68	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.46	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.202	√
3	1.15-1.25v	1.202	Pin 9 to Pin 10	1.202	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.477	Pin 11 to Pin 12	0.479	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.481	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP65P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.2	√	-17.2	√	-17.2	√
-5v	-12.3	√	-12.3	√	-12.3	√	-12.3	√
-1v	-2.42	√	-2.42	√	-2.42	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.41	√	2.42	√
5v	12.2	√	12.2	√	12.1	√	12.2	√
7v	17.1	√	17.0	√	17.0	√	17.0	√
10v	24.3	√	24.3	√	24.3	√	24.3	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP65P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.42	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

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LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP66P……Serial No ……
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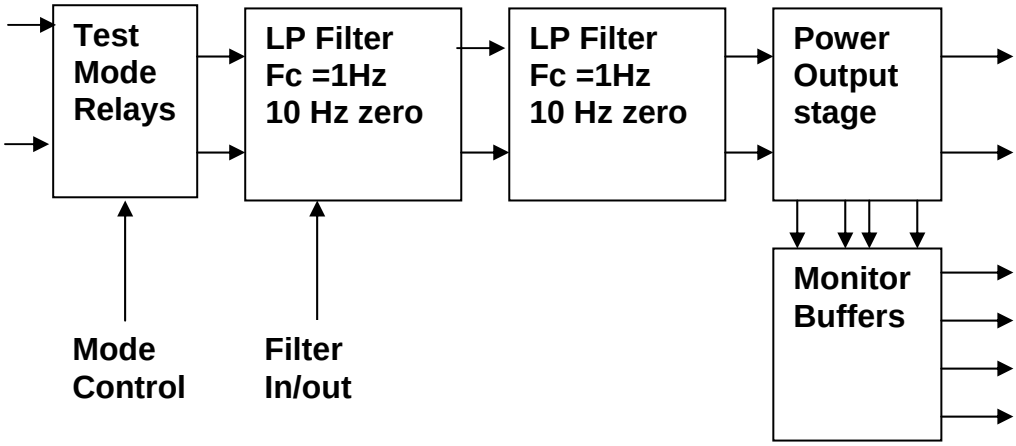
Contents

1. Description

Block diagram



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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP66P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP66P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Replaced U3.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP66P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

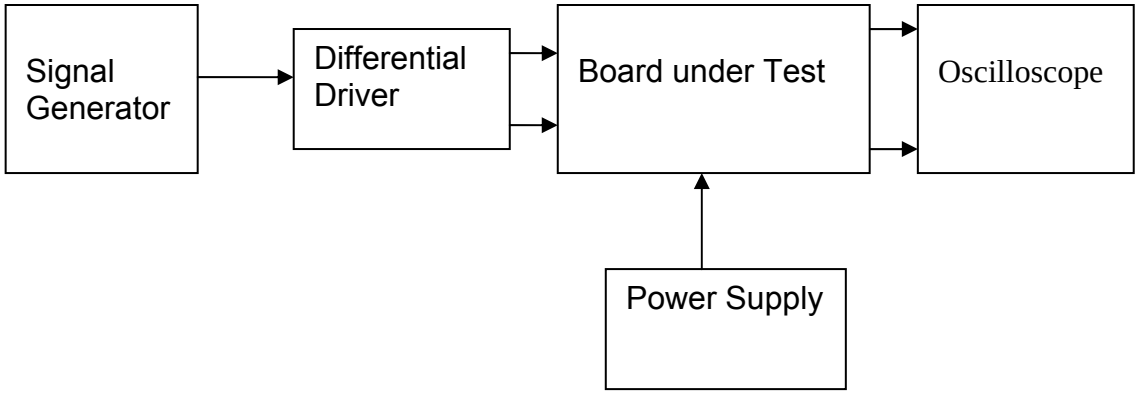
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP66P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.00	1mV	√
+15v TP4	14.80	1mV	√
-15v TP6	-14.98	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP66P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP66P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.35	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP66P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.25	3v to 3.4v	√
Ch3	3.25	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.49	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP66P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.202	Pin 9 to Pin 10	1.202	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.479	√
2	0.47-0.49v	0.481	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.479	√
4	0.47-0.49v	0.480	Pin 15 to Pin 16	0.482	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP66P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.2	√	-17.2	√	-17.2	√	-17.2	√
-5v	-12.3	√	-12.3	√	-12.3	√	-12.3	√
-1v	-2.42	√	-2.42	√	-2.42	√	-2.42	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.1	√	17.0	√	17.0	√
10v	24.4	√	24.4	√	24.4	√	24.5	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP66P……Serial No ……
Test Engineer ….Xen……..……
Date ……12/1/10……..……

13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.45	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.45	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v2 Advanced LIGO UK 26 November 2009

Triple TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

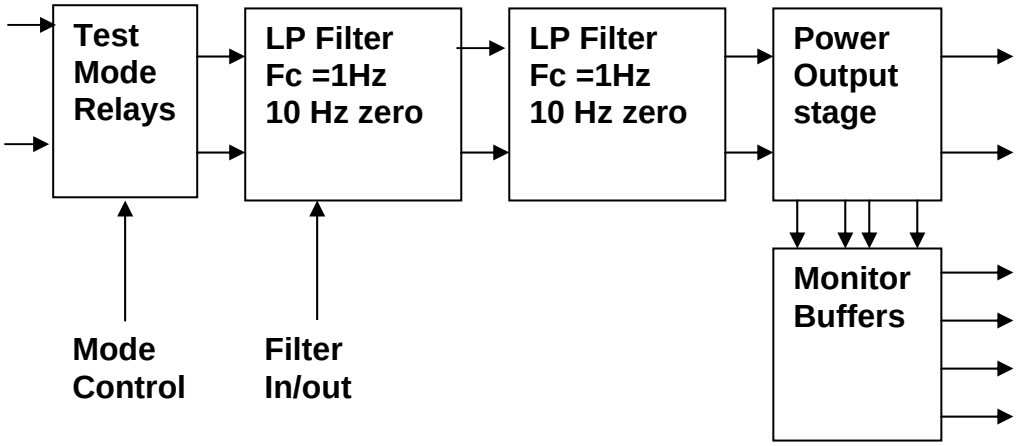
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP67P……Serial No ……
Test Engineer ….Xen……..……
Date ……13/1/10……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……T_TOP67P……Serial No ……
Test Engineer ….Xen……..……
Date ……13/1/10……..……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

Unit……T_TOP67P……Serial No ……
Test Engineer ….Xen……..……
Date ……13/1/10……..……

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Also, U1 has been replaced.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……T_TOP67P……Serial No ……
Test Engineer ….Xen……..……
Date ……13/1/10……..……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

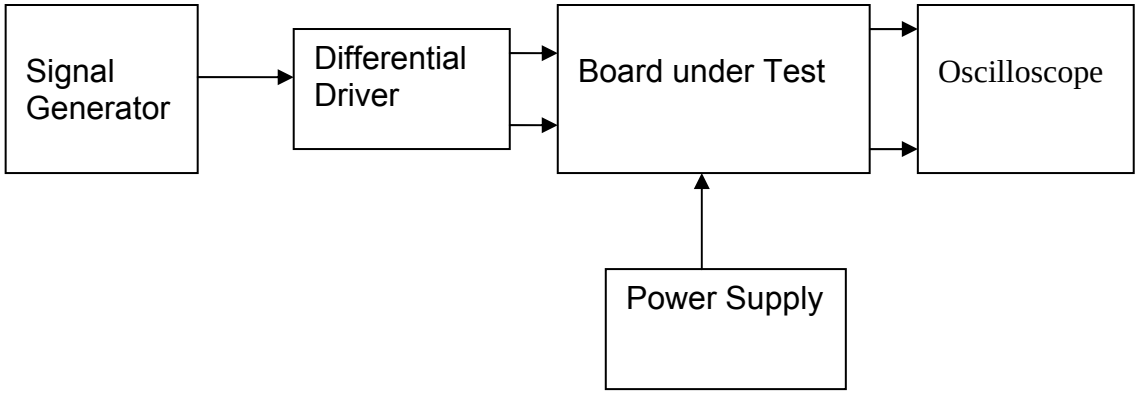
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_TOP67P……Serial No ……
Test Engineer ….Xen……..……
Date ……13/1/10……..……

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.00	1mV	√
+15v TP4	14.91	1mV	√
-15v TP6	-14.95	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_TOP67P……Serial No ……
Test Engineer ….Xen……..……
Date ……13/1/10……..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP67P……Serial No ……
Test Engineer ….Xen……..……
Date ……13/1/10……..……

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.35	**3.3v to 3.7v**	√
Ch3	3.35	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.66	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP67P……Serial No ……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.25	3v to 3.4v	√
Ch2	3.25	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP67P……Serial No ……
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Date ……13/1/10……..……

9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.202	Pin 1 to Pin 2	1.202	√
2	1.15-1.25v	1.202	Pin 5 to Pin 6	1.202	√
3	1.15-1.25v	1.202	Pin 9 to Pin 10	1.202	√
4	1.15-1.25v	1.202	Pin 13 to Pin 14	1.202	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.479	Pin 3 to Pin 4	0.480	√
2	0.47-0.49v	0.479	Pin 7 to Pin 8	0.480	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.478	Pin 15 to Pin 16	0.480	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.4	√
-7v	-17.2	√	-17.2	√	-17.2	√	-17.1	√
-5v	-12.3	√	-12.3	√	-12.3	√	-12.2	√
-1v	-2.42	√	-2.42	√	-2.42	√	-2.41	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.42	√
5v	12.1	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.2	√	24.3	√	24.3	√	24.3	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP67P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.43	√
Ch2	**3.3-3.5v**	3.44	√
Ch3	**3.3-3.5v**	3.43	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.

LIGO Laboratory / LIGO Scientific Collaboration

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Triple TOP Coil Driver Board Test Plan

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

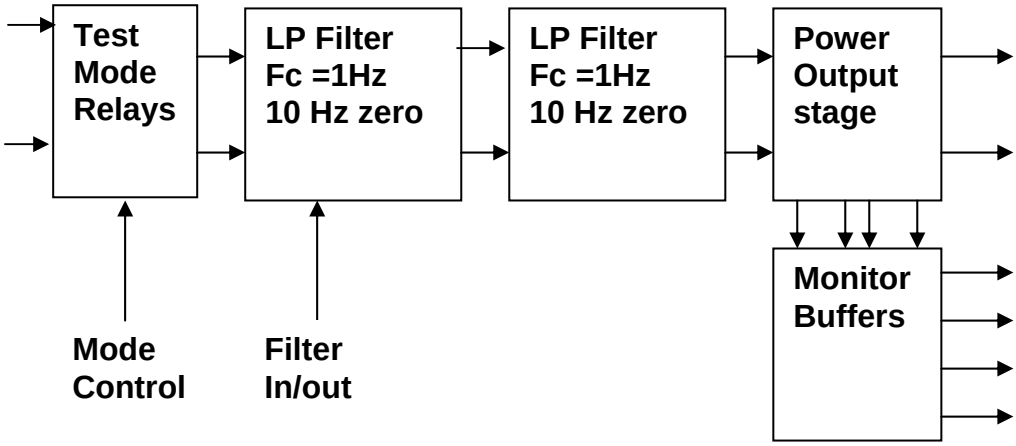
TRIPLE TOP COIL DRIVER BOARD
TEST PLAN

Unit……T_TOP69P……Serial No ……
Test Engineer ….Xen……..……
Date ……14/1/10……..……

Contents

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
V/I calibrator	Time Electronics	1044	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Also replaced C50 and C51 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

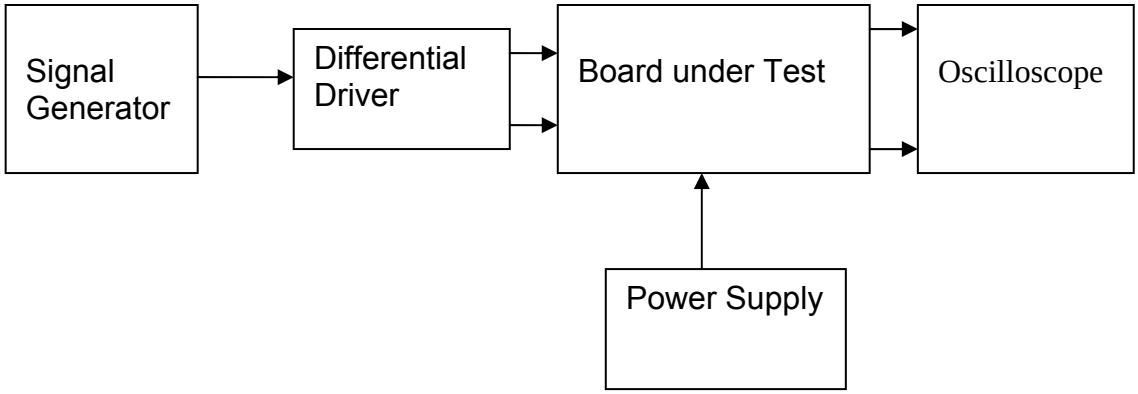
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.99	1mV	√
+15v TP4	14.82	1mV	√
-15v TP6	-15.05	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	400mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_TOP69P……Serial No ……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel.

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.85	5.0	5.0	**4.7v to 5v**	√
Ch2	4.85	5.0	5.0	**4.7v to 5v**	√
Ch3	4.85	5.0	5.0	**4.7v to 5v**	√
Ch4	4.85	5.0	5.0	**4.7v to 5v**	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	**4.7 to 5v**	√
Ch2	4.85	**4.7 to 5v**	√
Ch3	4.85	**4.7 to 5v**	√
Ch4	4.85	**4.7 to 5v**	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	**3.3v to 3.7v**	√
Ch2	3.4	**3.3v to 3.7v**	√
Ch3	3.4	**3.3v to 3.7v**	√
Ch4	3.4	**3.3v to 3.7v**	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	**0.48 to 0.75v**	√
Ch2	0.67	**0.48 to 0.75v**	√
Ch3	0.67	**0.48 to 0.75v**	√
Ch4	0.67	**0.48 to 0.75v**	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	**0.4v to 0.5v**	√
Ch2	0.47	**0.4v to 0.5v**	√
Ch3	0.47	**0.4v to 0.5v**	√
Ch4	0.47	**0.4v to 0.5v**	√

Unit……T_TOP69P……Serial No ……
Test Engineer ….Xen……..……
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1kHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.15	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.46	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……T_TOP69P……Serial No ……
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9. Monitor Outputs

Remove links W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

Ch.	Nominal r.m.s	Output: TP9 to TP13 r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.15-1.25v	1.203	Pin 1 to Pin 2	1.203	√
2	1.15-1.25v	1.203	Pin 5 to Pin 6	1.203	√
3	1.15-1.25v	1.203	Pin 9 to Pin 10	1.203	√
4	1.15-1.25v	1.203	Pin 13 to Pin 14	1.203	√

Current monitors

Ch.	Nominal r.m.s	Output across coil resistor r.m.s	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.47-0.49v	0.478	Pin 3 to Pin 4	0.479	√
2	0.47-0.49v	0.480	Pin 7 to Pin 8	0.481	√
3	0.47-0.49v	0.478	Pin 11 to Pin 12	0.480	√
4	0.47-0.49v	0.479	Pin 15 to Pin 16	0.482	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……T_TOP69P……Serial No ……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.4	√	-24.5	√	-24.5	√	-24.4	√
-7v	-17.2	√	-17.2	√	-17.2	√	-17.1	√
-5v	-12.2	√	-12.3	√	-12.2	√	-12.2	√
-1v	-2.4	√	-2.42	√	-2.42	√	-2.41	√
0v	0	√	0	√	0	√	0	√
1v	2.42	√	2.42	√	2.42	√	2.42	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.1	√	17.2	√	17.0	√
10v	24.3	√	24.3	√	24.5	√	24.3	√

Unit……Serial No ……
Test Engineer …….
Date …….

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it is only necessary to perform the full test on a sample board only.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@Freq
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……T_TOP69P……Serial No ……
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13. Dynamic Range Tests

Remove links W4 and W5. In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W or more load resistor to the output of each channel. Apply a 5v peak signal with respect to ground at 10Hz to the input. Set the voltage between TP10 and TP14 to 7.07V.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

If the waveforms are not clipping, measure the differential r.m.s voltage across each load resistor, and record it in the table below.

	Theoretical o/p r.m.s	Measured	OK?
Ch1	**3.3-3.5v**	3.44	√
Ch2	**3.3-3.5v**	3.43	√
Ch3	**3.3-3.5v**	3.44	√
Ch4	**3.3-3.5v**	3.43	√

Replace links W4 and W5.