LIGO Laboratory / LIGO Scientific Collaboration

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Advanced LIGO UK

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Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P68……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..21/7/10………………

Drive Card ID……T_TOP68P…………………
Monitor Card ID…Mon65………………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

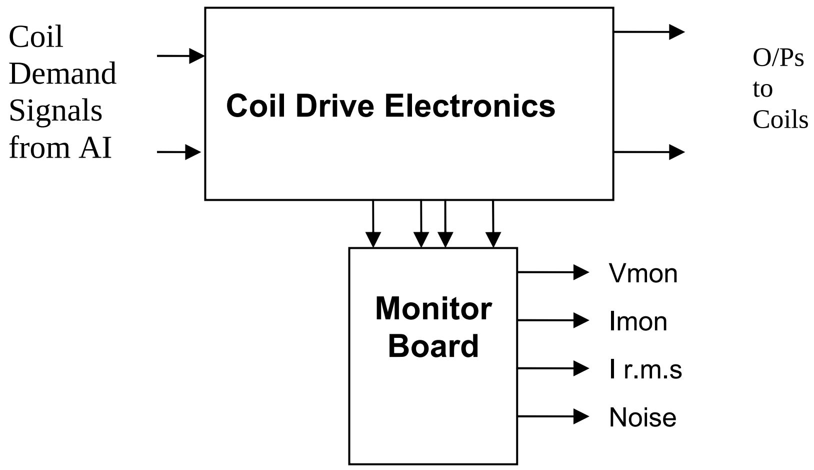

FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P68……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P68……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit.................T_TOP_P68.......................Serial No ....
Test Engineer.....Xen......................
Date................16/3/10.................

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P68……………………Serial No ………………………………
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Date……………..16/3/10………………

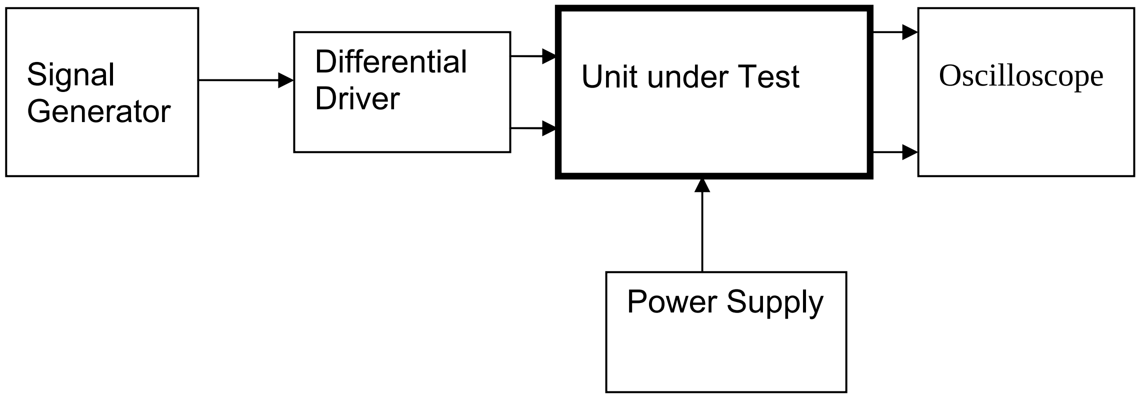
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P68……………………Serial No ………………………………
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6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	**- 16.5 supply current (mA)**
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	**Plus**	**Minus**
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P68……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..16/3/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P68……………………Serial No ………………………………
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8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.753	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.756	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.756	√

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9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.01	2.9μV√Hz	√
2		1.32	2.9μV√Hz	√
3		1.25	2.9μV√Hz	√
4		1.68	2.9μV√Hz	√

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10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………...T_TOP_P68……………………Serial No ………………………………
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11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	**CH1 IC1**	38.4	√
CH1 Negative		**CH1 IC5**	40.4	√
CH2 Positive	12.19	**CH2 IC1**	39.2	√
CH2 Negative		**CH2 IC5**	41.6	√
CH3 Positive	12.18	**CH3 IC1**	39.2	√
CH3 Negative		**CH3 IC5**	40.1	√
CH4 Positive	12.19	**CH4 IC1**	38.4	√
CH4 Negative		**CH4 IC5**	42.1	√

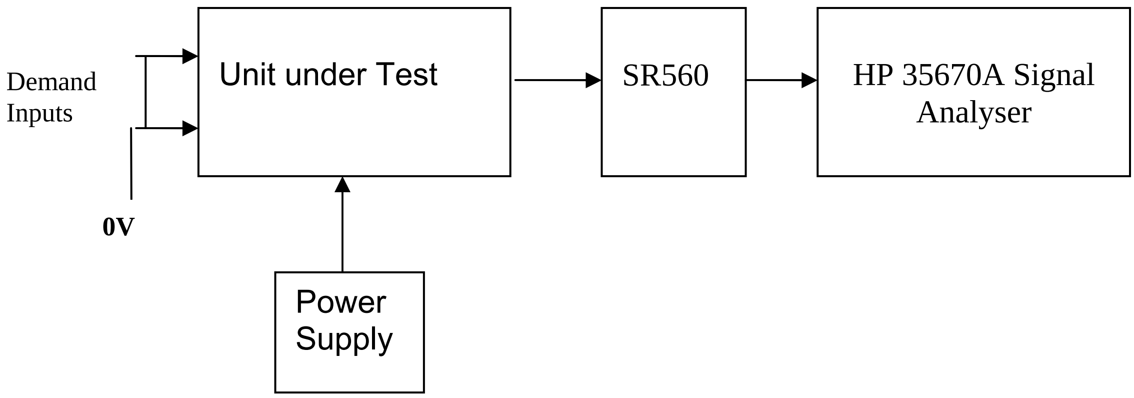
Unit……………….T_TOP_P68……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..21/7/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.1	-160.1
Ch2	-160dB	-100.2	-160.2
Ch3	-160dB	-100.8	-160.8
Ch4	-160dB	-102.3	-162.3

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P68……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..19/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.25	82.7mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP68P……………Serial No ………………………………
Test Engineer…………………RMC
Date……………………………18/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP68P
Driver board ID	TTOP68P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP68P
Monitor board ID	MON65
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON65

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

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11 November 2009

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit..................T_TOP_P1........................Serial No ....
Test Engineer ....Xen..................
Date ....18/11/09............

Drive Card ID......T_TOP1P............
Monitor Card ID...Mon21P...............

Contents

1. Description

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It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

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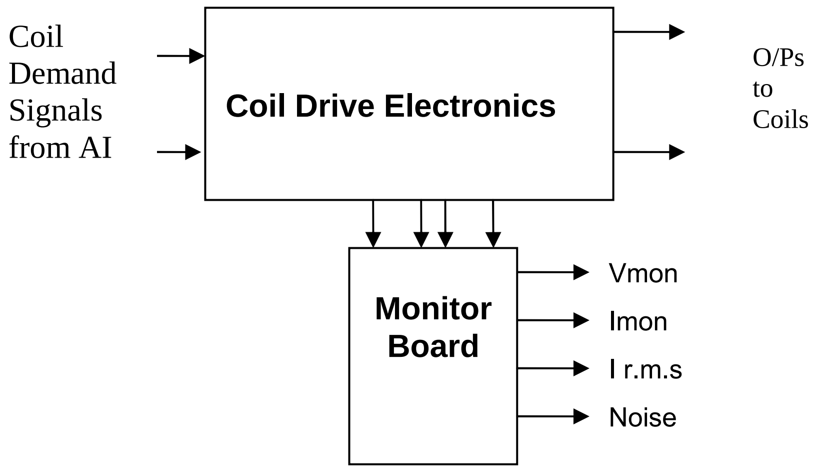

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Test Engineer…...Xen………………
Date ……………18/11/09….….……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

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Oscilloscope	ISO-TECH	ISR622	
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DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………T_TOP_P1……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….18/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Unit………………T_TOP_P1……………………Serial No ………………………………
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4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

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1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	**SIGNAL**	**Monitors:**	**In from Sat**	**OK?**
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	**SIGNAL**	**DESCRIPTION**	**DC in Connector**	**OK?**
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P1……………………Serial No ………………………………
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Date …………….18/11/09……..……

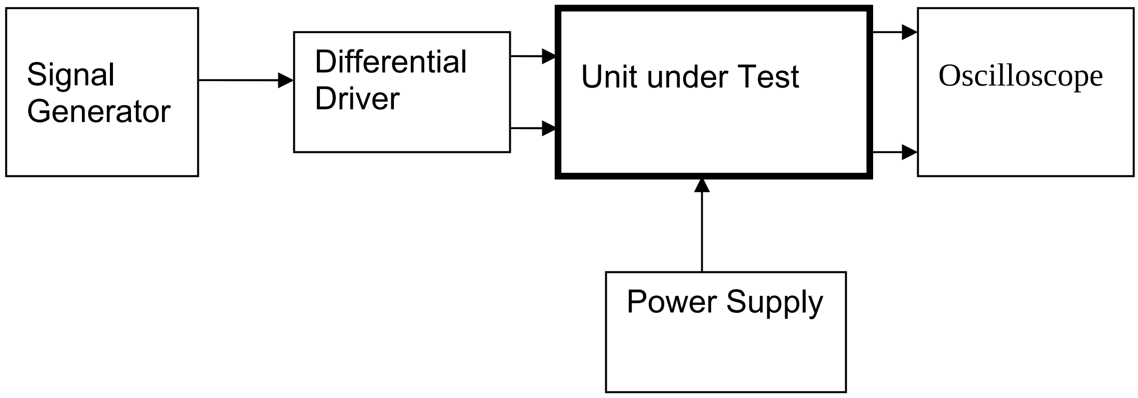
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P1........................Serial No ....
Test Engineer ....Xen...................
Date ....18/11/09.............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P1……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….18/11/09………….

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P1……………………Serial No ………………………………
Test Engineer ….Xen………….……
Date …………….18/11/09……..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	**Monitor Connector**	**Parameter**	**Theoretical Value (+/- .1v)**	**Measured Value**	**Pass/ Fail**
1	Pin 2	Current Monitor	0.75v r.m.s	0.751	√
	Pin 1	RMS Current	0.75v dc	0.752	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.750	√
	Pin 4	RMS Current	0.75v dc	0.755	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.752	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.752	√

Unit………………T_TOP_P1……………………Serial No ………………………………
Test Engineer ….Xen…………
Date ……………18/11/09……

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit……………….T_TOP_P1……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….18/11/09……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….T_TOP_P1……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….18/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

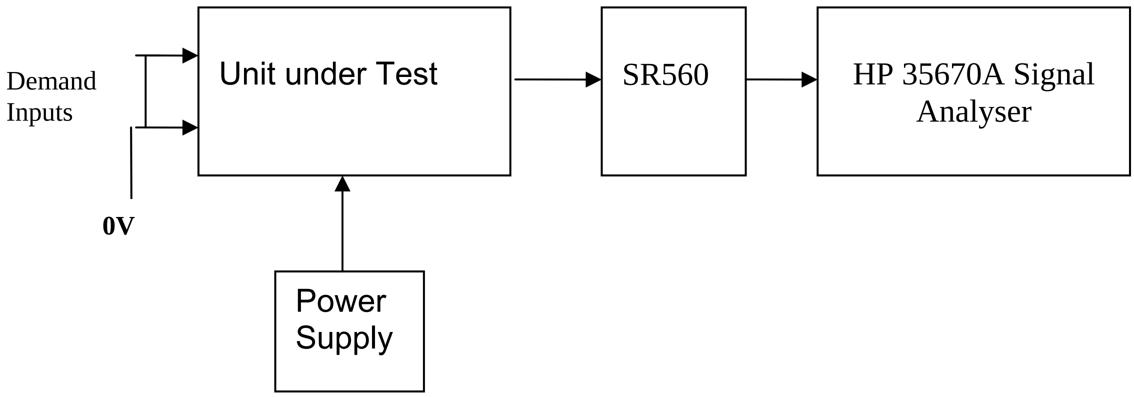
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.19	**CH1 IC1**	42.1	√
CH1 Negative		**CH1 IC5**	44.5	√
CH2 Positive	12.19	**CH2 IC1**	44.3	√
CH2 Negative		**CH2 IC5**	43.1	√
CH3 Positive	12.19	**CH3 IC1**	43.8	√
CH3 Negative		**CH3 IC5**	42.6	√
CH4 Positive	12.19	**CH4 IC1**	41.4	√
CH4 Negative		**CH4 IC5**	44.0	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………9/2/2010

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.5	-160.5
Ch2	-160dB	-101.5	-161.5
Ch3	-160dB	-98.8	-158.8
Ch4	-160dB	-101.0	-161.0

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Channel 3 rather noisy

Unit.................T_TOP_P1.......................Serial No ....
Test Engineer ....Xen...........
Date ....18/11/09......

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	3.35	85.2mA	120mA	84.8mA	√
2	39.4	3.37	85.5mA	120mA	84.8mA	√
3	39.3	3.34	85.0mA	120mA	84.8mA	√
4	39.4	3.35	85.0mA	120mA	84.8mA	√

Unit……………… T_TOP_P1……………………Serial No ………………………………
Test Engineer ………RMC
Date …………………16/12/09

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. √ Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	TTOP1P
Driver board ID	TTOP1P
Driver board Drawing No/Issue No	D0902747 v6
Driver board Serial Number	TTOP1P
Monitor board ID	MON21P
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON21P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………9/2/2010

16. Triple Top Test Plan Addendum

It was found that a problem existed on the Noise Monitor outputs. This was due to the lack of compensating capacitors on the Voltage Monitor AD797 output buffer amplifiers on the Driver Boards.

33pf capacitors need to be added to each channel in the places designated for C102 and C103.

Capacitors Added?

Channel 1 C102	OK
Channel 1 C103	OK
Channel 2 C102	OK
Channel 2 C103	OK
Channel 3 C102	OK
Channel 3 C103	OK
Channel 4 C102	OK
Channel 4 C103	OK

The noise output from each channel then needs to be measured again. For convenience, these results may be added to section 13 ofthis report in place of the previous readings.

Noise monitor tests

Connect the 39 ohm loads, the blanking plug in place on the drive input, and the relay test box.
Switch in all filters.
Connect power, and power up the unit. Measure the noise output on the noise monitor plug in μV/root Hz, on the HP Dynamic signal Analyser, the preamplifier with a gain of 10, and Stuart Aston's noise measurement set up. Check that it is less than 3 μV/root Hz with respect to ground, which may be found on sockets number 5, 6, 7, 8 or 9.

	Noise Monitor socket pin number	**Noise**	**< 3μV/rt Hz?**
Channel 1	1	1.5 μV/root Hz	OK
Channel 2	2	2.12 μV/root Hz	OK
Channel 3	3	1.40 μV/root Hz	OK
Channel 4	4	1.57 μV/root Hz	OK

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P2…………………….Serial No ………………………………
Test Engineer ….Xen………..
Date …………….12/11/09……

Drive Card ID……T_TOP2P…………
Monitor Card ID...Mon22P...…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

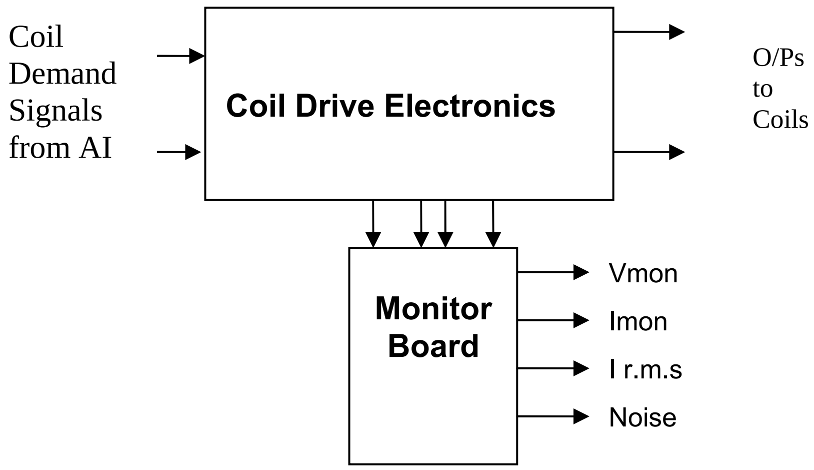


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..T_TOP_P2……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….12/11/09……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P2……………………Serial No ………………………………
Test Engineer ….Xen………..
Date ……………11/11/09…..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Unit………………T_TOP_P2……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….11/11/09……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P2……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….11/11/09……

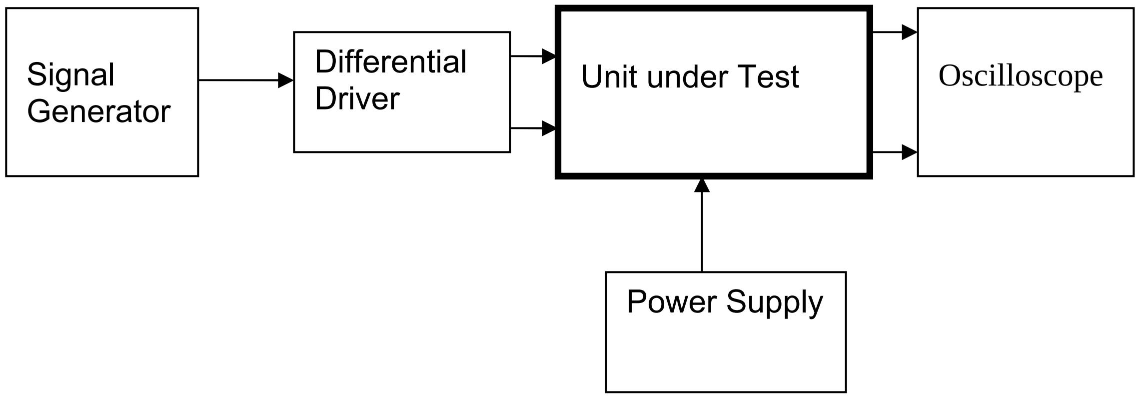
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P2……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….11/11/09……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P2……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….11/11/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit.................T_TOP_P2.......................Serial No ....
Test Engineer ....Xen...........
Date ....12/11/09......

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	**Monitor Connector**	**Parameter**	**Theoretical Value (+/- .1v)**	**Measured Value**	**Pass/ Fail**
1	Pin 2	Current Monitor	0.75v r.m.s	0.755	√
	Pin 1	RMS Current	0.75v dc	0.758	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.755	√
	Pin 4	RMS Current	0.75v dc	0.759	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.755	√
	Pin 7	RMS Current	0.75v dc	0.755	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.754	√
	Pin 10	RMS Current	0.75v dc	0.760	√

Unit……………….T_TOP_P2……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….12/11/09……

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit..................T_TOP_P2........................Serial No ....
Test Engineer ....Xen............
Date ....12/11/09......

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.

Ensure that links W4 and W5 are present.

Using the Dynamic Signal Analyser

With the filter switched in, measure the frequency response of each channel in turn between 0.1 Hz and 1 kHz. If a fast turn around is required, limit the measurement to the frequency range to between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them.

Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
0.1 Hz	7.7		
1Hz	1.0		
10Hz	-30.3		
100Hz	-42.8		
1KHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
0.1 Hz	7.7		
1Hz	1.1		
10Hz	-30.3		
100Hz	-42.9		
1KHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
0.1 Hz	7.6		
1Hz	1.0		
10Hz	-30.3		
100Hz	-42.9		
1KHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
0.1 Hz	7.6		
1Hz	1.1		
10Hz	-30.2		
100Hz	-42.9		
1KHz	-43.3		

Unit.................T_TOP_P2.......................Serial No ....
Test Engineer ....Xen...........
Date ....12/11/09......

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

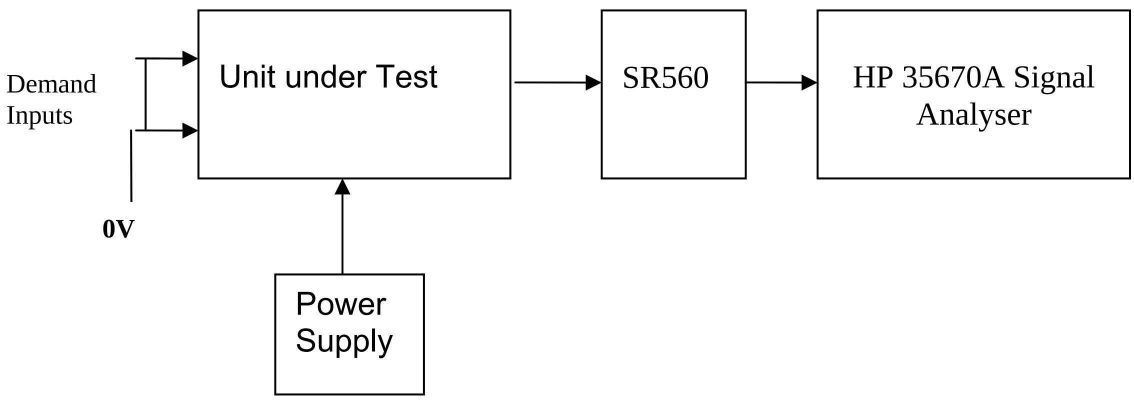
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.22	**CH1 IC1**	40.6	√
CH1 Negative		**CH1 IC5**	43.6	√
CH2 Positive	12.21	**CH2 IC1**	42.1	√
CH2 Negative		**CH2 IC5**	43.6	√
CH3 Positive	12.21	**CH3 IC1**	43.3	√
CH3 Negative		**CH3 IC5**	43.8	√
CH4 Positive	12.21	**CH4 IC1**	43.3	√
CH4 Negative		**CH4 IC5**	42.3	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………30/11/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.0	-159.0
Ch2	-160dB	-101.2	-161.2
Ch3	-160dB	-96.6	-156.6
Ch4	-160dB	-100.1	-160.1

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P2……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….12/11/09……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	3.35	85.2mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.35	85.2mA	120mA	84.8mA	√
4	39.4	3.35	85.0mA	120mA	84.8mA	√

Unit………………… T_TOP_P2………..Serial No ………………………………
Test Engineer ………RMC
Date …………………16/12/09

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. √ Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	TTOP2P
Driver board ID	TTOP2P
Driver board Drawing No/Issue No	D0902747 v6
Driver board Serial Number	TTOP2P
Monitor board ID	MON22P
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON22P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

Unit…………………TTOP P2………Serial No ………………………………
Test Engineer ………RMC
Date …………………24/2/10

FINAL NOISE MEASUREMENTS

Measure the noise output and noise monitor outputs of the completed unit. The extra screening provided by the enclosure protects the unit against extraneous noise, so the results will be more consistent.

If a channel exceeds the limits, replace the noisy ICs, note the work done. Re-measure and record the final result.

Output Noise

Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz (dB)	-60dB =	Measured in nV/√Hz	OK (+/-1dB) ?
Ch1	-160dB	-100.46 dB	-160.4 dB	6.54 nV/√Hz	OK
Ch2	-160dB	-99.9 dB	-159.9 dB	6.97 nV/√Hz	OK
Ch3	-160dB	-99.4 dB	-159.4 dB	7.34 nV/√Hz	OK
Ch4	-160dB	-99.4 dB	-159.4 dB	7.37 nV/√Hz	OK

Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	Output	/(Pre-amplifier gain)	Maximum value	Pass/Fail
1	18.8	1.88 μV/√Hz	2.9 μV/√Hz	OK
2	21.9	2.19 μV/√Hz	2.9 μV/√Hz	OK
3	18.4	1.84 μV/√Hz	2.9 μV/√Hz	OK
4	15.3	1.53 μV/√Hz	2.9 μV/√Hz	OK

Repair work (if any)

Channel 2 Drive Board: IC4 and IC8 replaced
Chanel 1 on Monitor: IC1 and IC6 replaced by LT1128 s

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit..................T_TOP_P3........................Serial No ....
Test Engineer ....Xen..................
Date ....19/11/09............

Drive Card ID......T_TOP3P............
Monitor Card ID...Mon23P...............

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

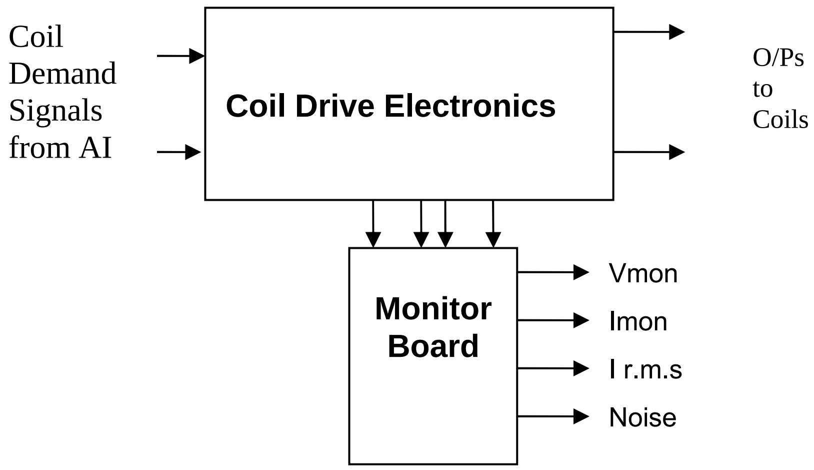


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…….…………
Date …………….19/11/09….….……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_P3……………………..Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….19/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Unit………………T_TOP_P3……………………Serial No ………………………………
Test Engineer ….Xen…………..…..
Date …………….19/11/09………….

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P3……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….19/11/09……..……

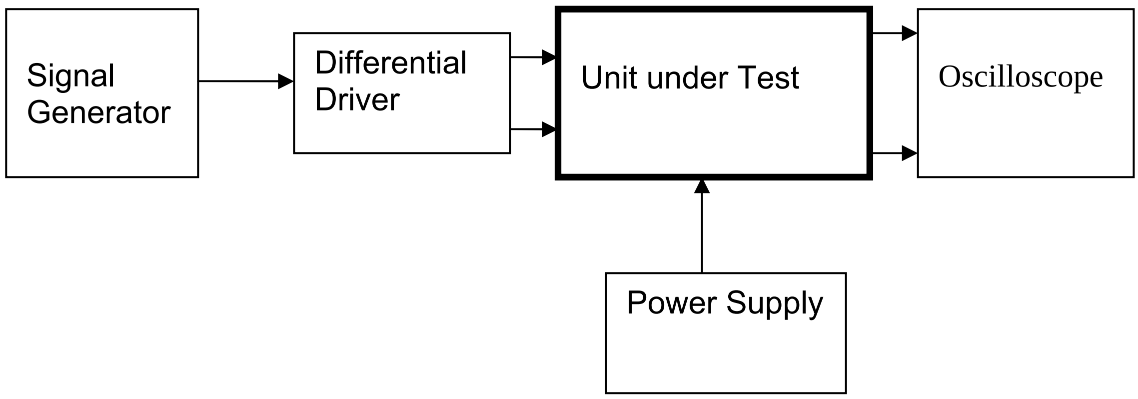
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P3........................Serial No ....
Test Engineer ....Xen...................
Date ....19/11/09.............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P3…………………….Serial No ………………………………
Test Engineer ….Xen……………….
Date …………….19/11/09………….

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit..................T_TOP_P3........................Serial No ....
Test Engineer ....Xen...............……
Date ....19/11/09……...……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.760	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.756	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.752	√

Unit……………….T_TOP_P3……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….19/11/09……

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Unit……………….T_TOP_P3……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….19/11/09……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.9		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………T_TOP_P3……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….19/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

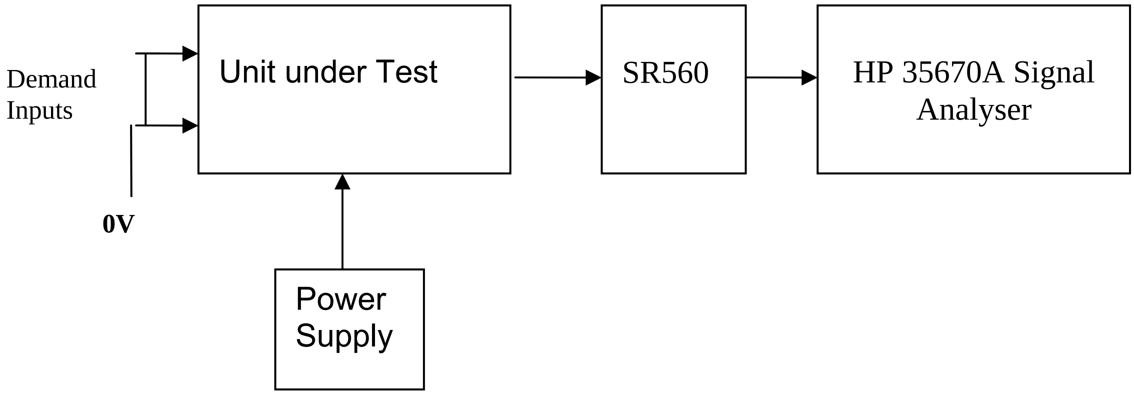
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.29	**CH1 IC1**	43.8	√
CH1 Negative		**CH1 IC5**	45.0	√
CH2 Positive	12.29	**CH2 IC1**	43.8	√
CH2 Negative		**CH2 IC5**	45.7	√
CH3 Positive	12.29	**CH3 IC1**	45.0	√
CH3 Negative		**CH3 IC5**	45.7	√
CH4 Positive	12.29	**CH4 IC1**	43.3	√
CH4 Negative		**CH4 IC5**	44.3	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………24/11/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-102.9	-162.9
Ch2	-160dB	-100.5	-160.5
Ch3	-160dB	-101.27	-161.27
Ch4	-160dB	-98.5	-158.5

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P3……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….19/11/09……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.35	85.2mA	120mA	84.8mA	√
2	39.4	3.35	85.0mA	120mA	84.8mA	√
3	39.3	3.35	85.2mA	120mA	84.8mA	√
4	39.4	3.35	85.0mA	120mA	84.8mA	√

Unit………………TTOP3P…………Serial No ………………………………
Test Engineer ………RMC
Date …………………16/12/09

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. √ Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP3P
Driver board ID	TTOP3P
Driver board Drawing No/Issue No	D0902747 v6
Driver board Serial Number	TTOP3P
Monitor board ID	MON23P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON23P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

Unit……………………………………Serial No ………………………………
Test Engineer ………
Date …………………

16. Triple Top Test Plan Addendum

It was found that a problem existed on the Noise Monitor outputs. This was due to the lack of compensating capacitors on the Voltage Monitor AD797 output buffer amplifiers on the Driver Boards.

33pf capacitors need to be added to each channel in the places designated for C102 and C103.

Capacitors Added?

Channel 1 C102	OK
Channel 1 C103	OK
Channel 2 C102	OK
Channel 2 C103	OK
Channel 3 C102	OK
Channel 3 C103	OK
Channel 4 C102	OK
Channel 4 C103	OK

The noise output from each channel then needs to be measured again. For convenience, these results may be added to section 13 ofthis report in place of the previous readings.

Noise monitor tests

Connect the 39 ohm loads, the blanking plug in place on the drive input, and the relay test box.
Switch in all filters.
Connect power, and power up the unit. Measure the noise output on the noise monitor plug in μV/root Hz, on the HP Dynamic signal Analyser, the preamplifier with a gain of 10, and Stuart Aston's noise measurement set up. Check that it is less than 3 μV/root Hz with respect to ground, which may be found on sockets number 5, 6, 7, 8 or 9.

	Noise Monitor socket pin number	**Noise**	**< 3μV/rt Hz?**
Channel 1	1	1.26 μV/root Hz	OK
Channel 2	2	1.2 μV/root Hz	OK
Channel 3	3	1.45 μV/root Hz	OK
Channel 4	4	1.89 μV/root Hz	OK

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit..................T_TOP_P4........................Serial No ....
Test Engineer ....Xen..................
Date ....18/11/09............

Drive Card ID......T_TOP4P............
Monitor Card ID...Mon24P.....……….

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

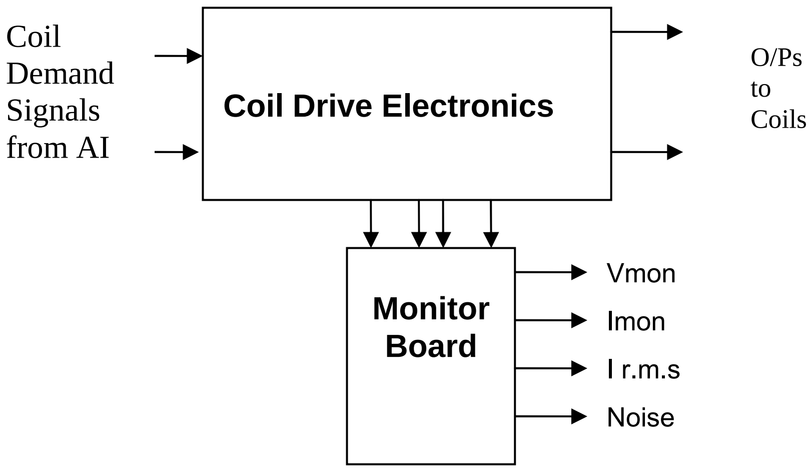


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P4……………………Serial No ………………………………
Test Engineer…..Xen………………
Date ……………18/11/09………….

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P4……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….17/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Unit………………T_TOP_P4……………………Serial No ………………………………
Test Engineer ….Xen……………..…..
Date …………….17/11/09………….

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P4……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….17/11/09……..……

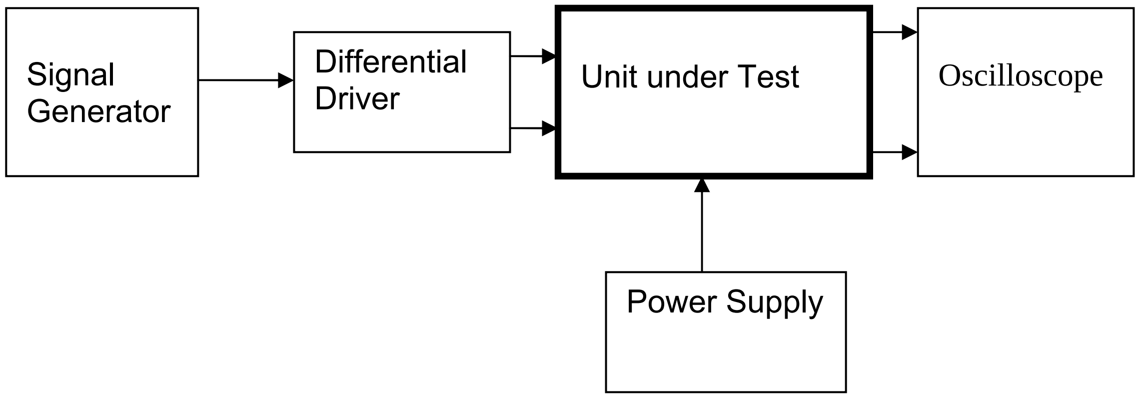
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)
Pd In from Sat pin 9, 10 = +16.5v or DC in A1
Pd In from Sat pin 11, 12 = -16.5 or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v or DC in A2

Coil Drive Outputs
Ch1+ = Coil out to Sat pin 1
Ch2+ = Coil out to Sat pin 3
Ch3+ = Coil out to Sat pin 5
Ch4+ = Coil out to Sat pin 7

Ch1- = Coil out to Sat pin 9
Ch2- = Coil out to Sat pin 11
Ch3- = Coil out to Sat pin 13
Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P4........................Serial No ....
Test Engineer ....Xen...................
Date ....17/11/09.............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P4……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….17/11/09…….……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P4……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….18/11/09……..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.754	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.758	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit………………T_TOP_P4……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….18/11/09……

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit………………T_TOP_P4……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….18/11/09……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.7		
10Hz	-30.9		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.7		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit.................T_TOP_P4.......................Serial No ....
Test Engineer ....Xen...........
Date ....18/11/09......

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

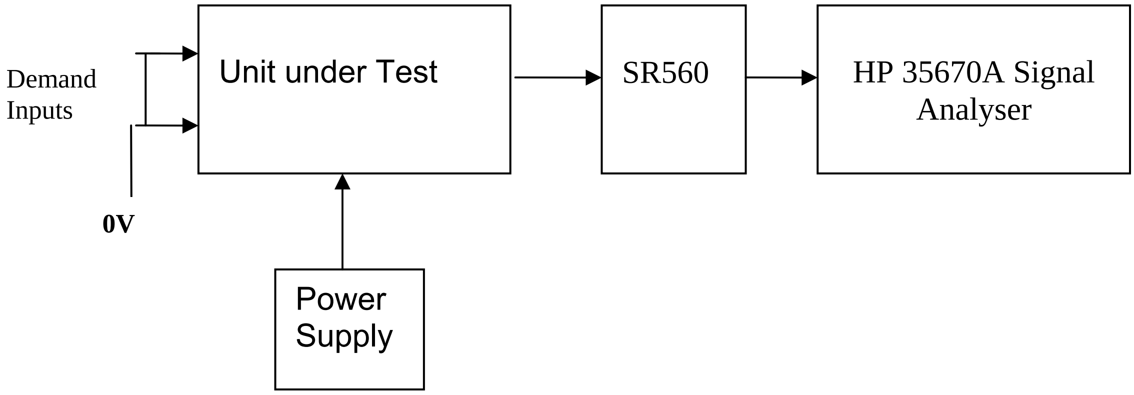
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	**CH1 IC1**	42.6	√
CH1 Negative		**CH1 IC5**	43.6	√
CH2 Positive	12.20	**CH2 IC1**	44.8	√
CH2 Negative		**CH2 IC5**	45.0	√
CH3 Positive	12.20	**CH3 IC1**	44.5	√
CH3 Negative		**CH3 IC5**	45.0	√
CH4 Positive	12.20	**CH4 IC1**	42.3	√
CH4 Negative		**CH4 IC5**	43.3	√

Unit……………………………………Serial No ………………………………
Test Engineer ……RMC…
Date …………………30/11/09 – 10:00 am

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.6	-159.6
Ch2	-160dB	-100.38	-160.38
Ch3	-160dB	-101.6	-161.6
Ch4	-160dB	-100.0	-160.0

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit.................T_TOP_P4.......................Serial No ....
Test Engineer ....Xen...........
Date ....18/11/09......

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	3.35	85.2mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.35	85.2mA	120mA	84.8mA	√
4	39.4	3.35	85.0mA	120mA	84.8mA	√

Unit...............TTOP4P............Serial No ....
Test Engineer ....RMC
Date 16/12/09

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. √ Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	TTOP4P
Driver board ID	TTOP4P
Driver board Drawing No/Issue No	D0902747 v6
Driver board Serial Number	TTOP4P
Monitor board ID	MON24P
Monitor board Drawing No/Issue No	DO70480_4_K
Monitor board Serial Number	MON24P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………10/2/10 – 9:30 am

16. Triple Top Test Plan Addendum

It was found that a problem existed on the Noise Monitor outputs. This was due to the lack of compensating capacitors on the Voltage Monitor AD797 output buffer amplifiers on the Driver Boards.

33pf capacitors need to be added to each channel in the places designated for C102 and C103.

Capacitors Added?

Channel 1 C102	OK
Channel 1 C103	OK
Channel 2 C102	OK
Channel 2 C103	OK
Channel 3 C102	OK
Channel 3 C103	OK
Channel 4 C102	OK
Channel 4 C103	OK

The noise output from each channel then needs to be measured again. For convenience, these results may be added to section 13 ofthis report in place of the previous readings.

Noise monitor tests

Connect the 39 ohm loads, the blanking plug in place on the drive input, and the relay test box.
Switch in all filters.
Connect power, and power up the unit. Measure the noise output on the noise monitor plug in μV/root Hz, on the HP Dynamic signal Analyser, the preamplifier with a gain of 10, and Stuart Aston's noise measurement set up. Check that it is less than 3 μV/root Hz with respect to ground, which may be found on sockets number 5, 6, 7, 8 or 9.

	Noise Monitor socket pin number	**Noise**	**< 3μV/rt Hz?**
Channel 1	1	1.41	OK
Channel 2	2	1.80	OK
Channel 3	3	2.1	OK
Channel 4	4	2.17	OK

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P5……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….19/11/09…………

Drive Card ID……T_TOP5P…………
Monitor Card ID...Mon25P…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

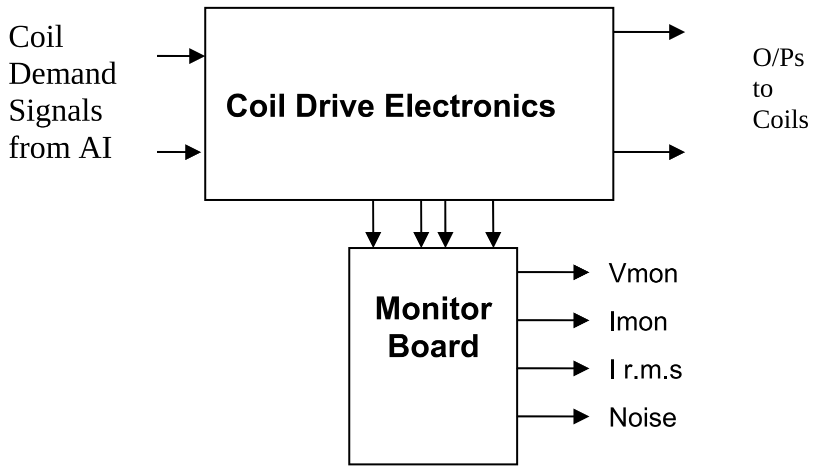

FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P5……………………Serial No ………………………………
Test Engineer…...Xen………………
Date …………….19/11/09…….……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_P5……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….18/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Unit……………….T_TOP_P5……………………Serial No ………………………………
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4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	**SIGNAL**	**DESCRIPTION**	**Pd in from Sat**	**OK?**
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	**SIGNAL**	**Monitors:**	**In from Sat**	**OK?**
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	**SIGNAL**	**DESCRIPTION**	**DC in Connector**	**OK?**
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit…………………T_TOP_P5……………………….Serial No ………………………………….
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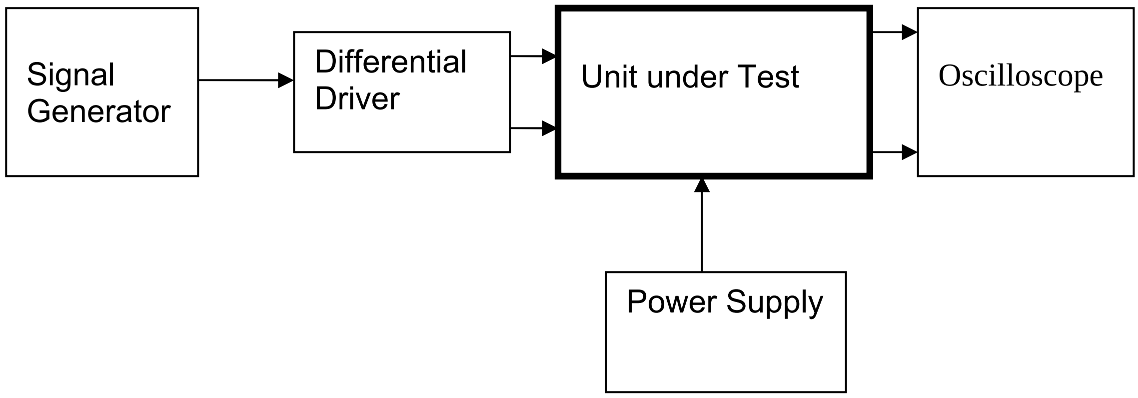
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P5........................Serial No ....
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6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit..................T_TOP_P5........................Serial No ....
Test Engineer ....Xen...................
Date ....18/11/09.............

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit..................T_TOP_P5........................Serial No ....
Test Engineer ....Xen..................
Date ....18/11/09...........

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.761	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.753	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.758	√

Unit………………T_TOP_P5……………………Serial No ………………………………
Test Engineer ….Xen…………
Date ……………18/11/09……

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit……………….T_TOP_P5……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….19/11/09……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.8		
10Hz	-30.8		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P5……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….19/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

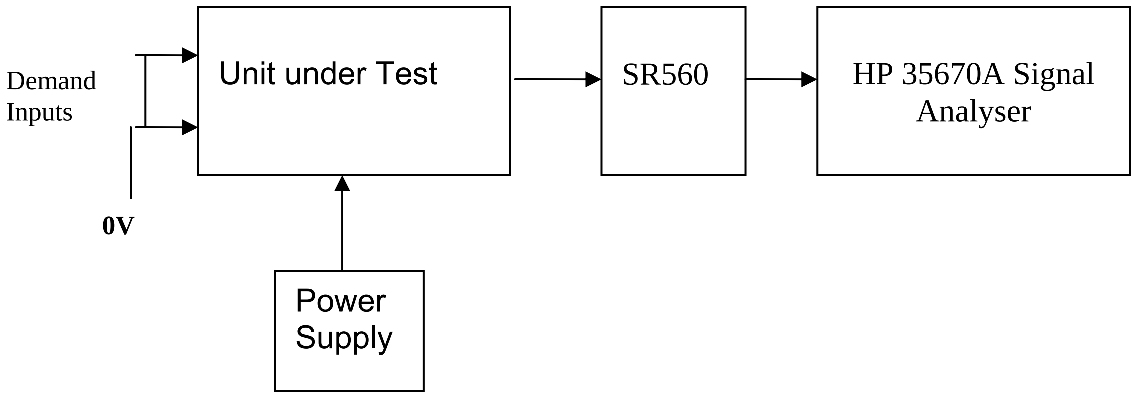
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.19	**CH1 IC1**	41.6	√
CH1 Negative		**CH1 IC5**	44.0	√
CH2 Positive	12.19	**CH2 IC1**	42.8	√
CH2 Negative		**CH2 IC5**	45.7	√
CH3 Positive	12.19	**CH3 IC1**	42.3	√
CH3 Negative		**CH3 IC5**	43.3	√
CH4 Positive	12.19	**CH4 IC1**	41.6	√
CH4 Negative		**CH4 IC5**	42.6	√

Unit.......................................Serial No ....
Test Engineer ....
Date ....

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.4	-160.4
Ch2	-160dB	-100.5	-160.5
Ch3	-160dB	-96	-156
Ch4	-160dB	-99.7	-159.7

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P5……………………Serial No ………………………………
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Date …………….19/11/09……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	3.36	85.5mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.35	85.2mA	120mA	84.8mA	√
4	39.4	3.36	85.3mA	120mA	84.8mA	√

Unit……………………TTOP5……Serial No ………………………………
Test Engineer ………RMC
Date …………………16/12/09

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. √ Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	TTOP5P
Driver board ID	TTOP5P
Driver board Drawing No/Issue No	D0902747 v6
Driver board Serial Number	TTOP5P
Monitor board ID	MON25P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON25P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

Unit……………………TTOP5……Serial No ………………………………
Test Engineer ………RMC
Date …………………24/2/10

FINAL NOISE MEASUREMENTS

Measure the noise output and noise monitor outputs of the completed unit. The extra screening provided by the enclosure protects the unit against extraneous noise, so the results will be more consistent.

If a channel exceeds the limits, replace the noisy ICs, note the work done. Re-measure and record the final result.

Output Noise

Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz (dB)	-60dB =	Measured in nV/√Hz	OK (+/-1dB) ?
Ch1	-160dB	-100.17	-160.17	6.7	OK
Ch2	-160dB	-100.1	-160.1	6.8	OK
Ch3	-160dB	-100.1	-160.1	6.8	OK
Ch4	-160dB	-101.34	-161.37	5.9	OK

Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	Output	/(Pre-amplifier gain)	Maximum value	Pass/Fail
1	14	1.4	2.9 μV/√Hz	OK
2	16.6	1.66	2.9 μV/√Hz	OK
3	20	2.0	2.9 μV/√Hz	OK
4	12	1.2	2.9 μV/√Hz	OK

Repair work (if any)

Channel 3 IC1 and IC4 changed
Channels 1 & 2 monitor ICs IC1 and IC6 changed for LT1128 s

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit..................T_TOP_P6........................Serial No ....
Test Engineer ....Xen..................
Date ....17/11/09............

Drive Card ID......T_TOP6P............
Monitor Card ID...Mon26P...............

Contents

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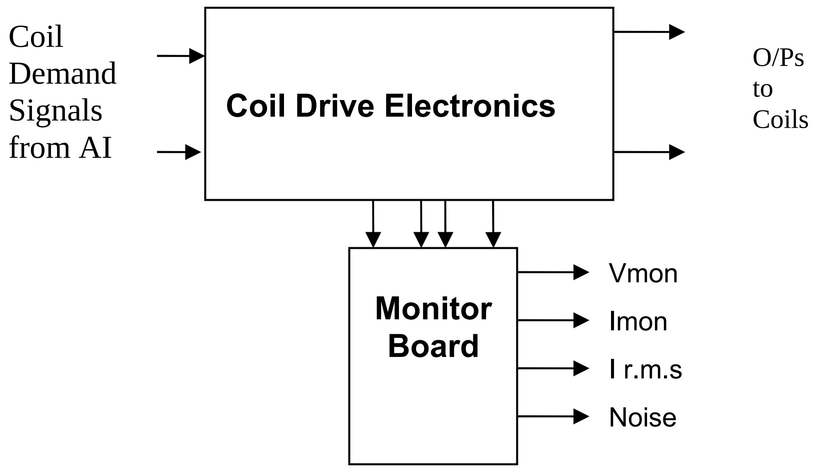

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Unit………………T_TOP_P6……………………Serial No ………………………………
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Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P6……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….17/11/09……..……

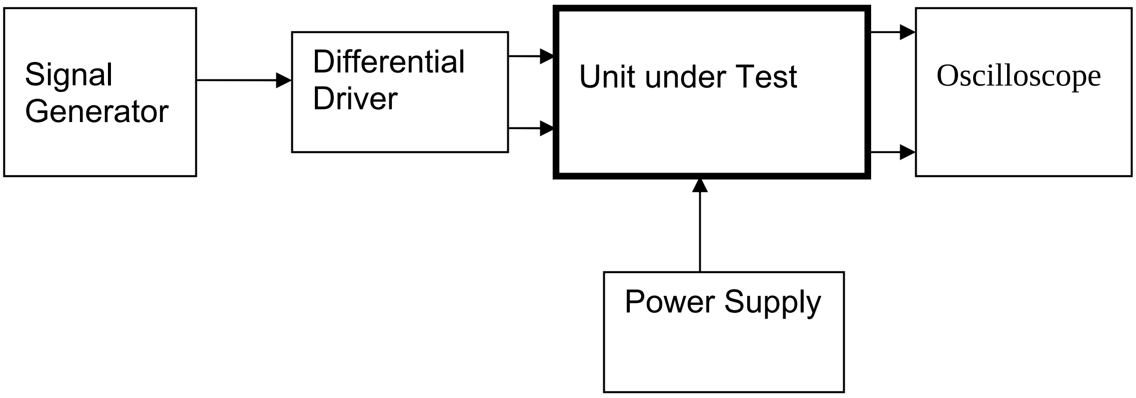
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P6……………………Serial No ………………………………
Test Engineer ….Xen………………
Date ……………17/11/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit..................T_TOP_P6........................Serial No ....
Test Engineer ....Xen..................
Date ....17/11/09.............

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit.................T_TOP_P6.......................Serial No ....
Test Engineer ....Xen...............……
Date ....17/11/09......…….

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.755	√
	Pin 1	RMS Current	0.75v dc	0.758	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.757	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.754	√

Unit..................T_TOP_P6........................Serial No ....
Test Engineer ....Xen...........
Date ....17/11/09......

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit………………T_TOP_P6……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….17/11/09……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….T_TOP_P6……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….17/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.21	**CH1 IC1**	43.3	√
CH1 Negative		**CH1 IC5**	43.1	√
CH2 Positive	12.21	**CH2 IC1**	43.3	√
CH2 Negative		**CH2 IC5**	43.1	√
CH3 Positive	12.21	**CH3 IC1**	41.4	√
CH3 Negative		**CH3 IC5**	44.3	√
CH4 Positive	12.21	**CH4 IC1**	43.1	√
CH4 Negative		**CH4 IC5**	44.5	√

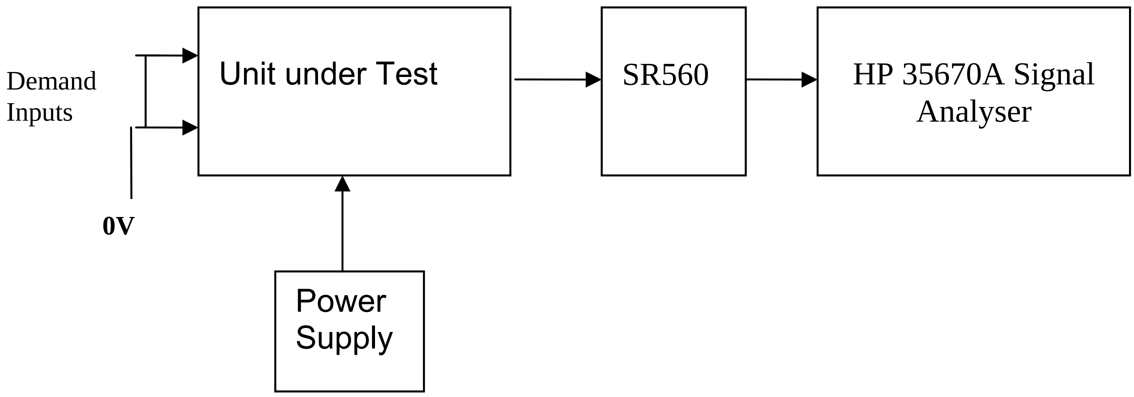
Unit………………T_TOP_P6………………Serial No ………………………………
Test Engineer ….RMC…………..
Date …………….1/12/09 ……….

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.5	-161.5
Ch2	-160dB	-101.8	-161.8
Ch3	-160dB	-98.2	-158.2
Ch4	-160dB	-102	-162

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit………………T_TOP_P6……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….17/11/09……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	3.36	85.5mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.36	85.5mA	120mA	84.8mA	√
4	39.4	3.36	85.3mA	120mA	84.8mA	√

Unit……………………TTOP06P…Serial No ………………………………
Test Engineer ………RMC
Date …………………16/12/09

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. √ Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	TTOP06P
Driver board ID	TTOP06P
Driver board Drawing No/Issue No	D0902747 v6
Driver board Serial Number	TTOP06P
Monitor board ID	MON26P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON26P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

Unit………T Top 6 P……………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………14/1/10

PROBLEM REPORT

Problems
After assembly, a quick test on filter operation was performed. Link W4 on channel 1 was found to be floating.

Cause
The problem was caused by link W4 breaking away at both ends.

Solution
Link W4 was repaired with wire links at both ends, and reinforced with rapid Araldite.

Confirmation
10 Hz filter check performed successfully.

Unit re-assembled and final assembly tests repeated.

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………10/1/10

16. Triple Top Test Plan Addendum

It was found that a problem existed on the Noise Monitor outputs. This was due to the lack of compensating capacitors on the Voltage Monitor AD797 output buffer amplifiers on the Driver Boards.

33pf capacitors need to be added to each channel in the places designated for C102 and C103.

Capacitors Added?

Channel 1 C102	OK
Channel 1 C103	OK
Channel 2 C102	OK
Channel 2 C103	OK
Channel 3 C102	OK
Channel 3 C103	OK
Channel 4 C102	OK
Channel 4 C103	OK

The noise output from each channel then needs to be measured again. For convenience, these results may be added to section 13 ofthis report in place of the previous readings.

Noise monitor tests

Connect the 39 ohm loads, the blanking plug in place on the drive input, and the relay test box.
Switch in all filters.
Connect power, and power up the unit. Measure the noise output on the noise monitor plug in μV/root Hz, on the HP Dynamic signal Analyser, the preamplifier with a gain of 10, and Stuart Aston's noise measurement set up. Check that it is less than 3 μV/root Hz with respect to ground, which may be found on sockets number 5, 6, 7, 8 or 9.

Unit…………………TTOP 6 P………Serial No ………………………………
Test Engineer ………RMC
Date …………………25/2/10

FINAL NOISE MEASUREMENTS

Measure the noise output and noise monitor outputs of the completed unit. The extra screening provided by the enclosure protects the unit against extraneous noise, so the results will be more consistent.

If a channel exceeds the limits, replace the noisy ICs, note the work done. Re-measure and record the final result.

Output Noise

Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz (dB)	-60dB =	Measured in nV/√Hz	OK (+/-1dB) ?
Ch1	-160dB	-101.5	-161.5	6.0 nV/√Hz	OK
Ch2	-160dB	-101.3	-161.3	5.9 nV/√Hz	OK
Ch3	-160dB	-100.03	-160.03	6.9 nV/√Hz	OK
Ch4	-160dB	-101.54	-161.54	5.8 nV/√Hz	OK

Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	Output	/(Pre-amplifier gain)	Maximum value	Pass/Fail
1	16.4 μV/√Hz	1.64 μV/√Hz	2.9 μV/√Hz	OK
2	18.0 μV/√Hz	1.80 μV/√Hz	2.9 μV/√Hz	OK
3	14.9 μV/√Hz	1.49 μV/√Hz	2.9 μV/√Hz	OK
4	15.3 μV/√Hz	1.53 μV/√Hz	2.9 μV/√Hz	OK

Repair work (if any)

Monitor: IC1 Ch 1 replaced
IC6 Ch 4 changed

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………..…T_TOP_P7……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09…………

Drive Card ID……T_TOP7P…………
Monitor Card ID...Mon27P..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

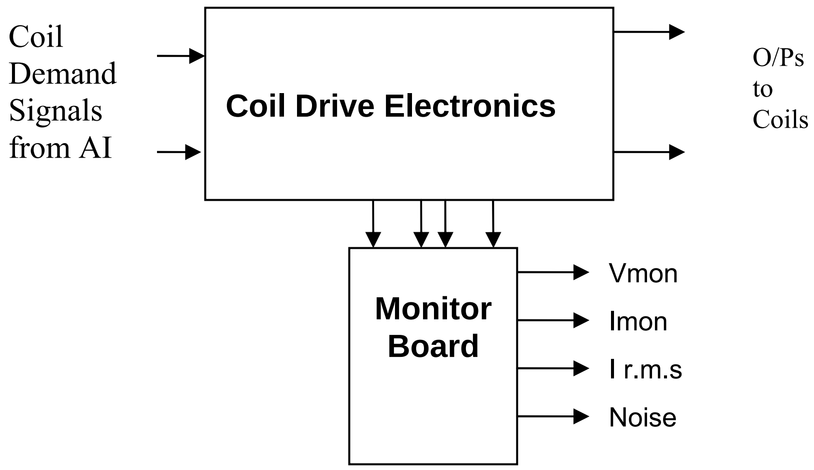


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P7……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P7……………………Serial No ……………………………..
Test Engineer ….Xen……………..
Date …………….23/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Unit..................T_TOP_P7........................Serial No ....
Test Engineer ....Xen..................
Date ....23/11/09............

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	**SIGNAL**	**DESCRIPTION**	**Pd in from Sat**	**OK?**
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	**SIGNAL**	**Monitors:**	**In from Sat**	**OK?**
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	**SIGNAL**	**DESCRIPTION**	**DC in Connector**	**OK?**
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P7……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09…………

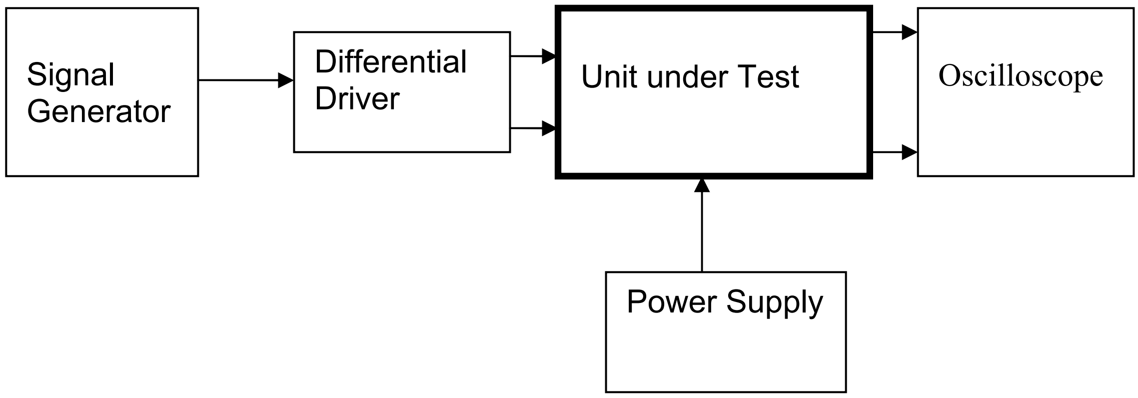
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P7........................Serial No ....
Test Engineer ....Xen..................
Date ....23/11/09.............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P7……………………Serial No ………………………………
Test Engineer ….Xen………………
Date ……………23/11/09………….

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P7……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date ……………23/11/09……..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.753	√
	Pin 1	RMS Current	0.75v dc	0.759	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.755	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.749	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit………………T_TOP_P7……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….23/11/09……

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit..................T_TOP_P7........................Serial No ....
Test Engineer ....Xen............
Date ....23/11/09......

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………T_TOP_P7……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….23/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

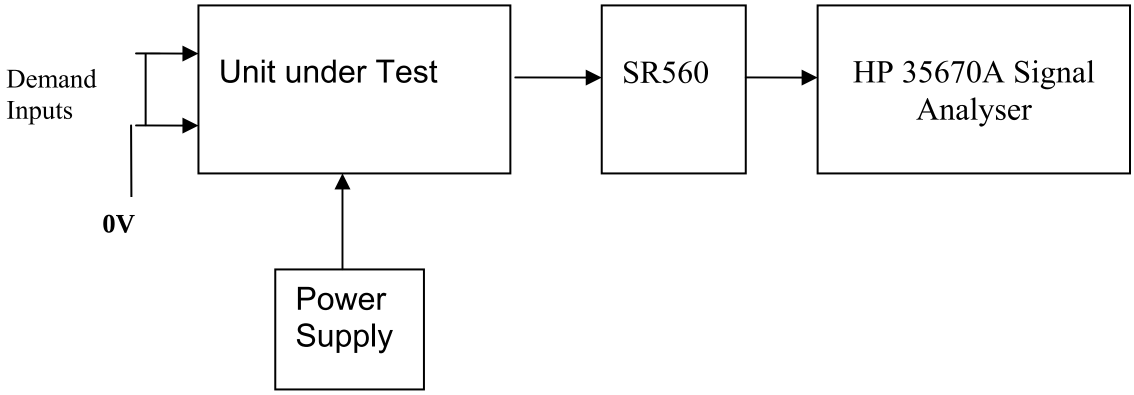
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.23	CH1 IC1	41.6	√
CH1 Negative		CH1 IC5	42.8	√
CH2 Positive	12.23	CH2 IC1	42.3	√
CH2 Negative		CH2 IC5	42.3	√
CH3 Positive	12.23	CH3 IC1	41.6	√
CH3 Negative		CH3 IC5	43.1	√
CH4 Positive	12.23	CH4 IC1	42.8	√
CH4 Negative		CH4 IC5	43.6	√

Unit......................................Serial No ....
Test Engineer ....RMC
Date 15/2/10

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.0	-159,0
Ch2	-160dB	-103.1	-163.1
Ch3	-160dB	-96.0	-156.0
Ch4	-160dB	-101.5	-101.5

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P7……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….23/11/09……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	3.36	85.5mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.36	85.5mA	120mA	84.8mA	√
4	39.4	3.36	85.3mA	120mA	84.8mA	√

Unit…………………… T_TOP_P7………………Serial No ………………………………
Test Engineer ………
Date …………………

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. √ Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	TTOPP7
Driver board ID	TTOPP7
Driver board Drawing No/Issue No	D0902747 V6
Driver board Serial Number	TTOPP7
Monitor board ID	MON27P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON27P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

Unit………T Top 7 P……………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………14/1/10

PROBLEM REPORT

Problems
After assembly, a quick test on filter operation was performed. Link W4 on channel 4 was found to be disconnected from the capacitor.

Cause
The problem was caused by link W4 breaking away at one end.

Solution
Link W4 was repaired with a wire links top the capacitor, and reinforced with rapid Araldite.

Confirmation
10 Hz filter check performed successfully.

Unit re-assembled and final assembly tests repeated.

Unit……………………………………Serial No ………………………………
Test Engineer ………
Date …………………10/2/10

16. Triple Top Test Plan Addendum

It was found that a problem existed on the Noise Monitor outputs. This was due to the lack of compensating capacitors on the Voltage Monitor AD797 output buffer amplifiers on the Driver Boards.

33pf capacitors need to be added to each channel in the places designated for C102 and C103.

Capacitors Added?

Channel 1 C102	OK
Channel 1 C103	OK
Channel 2 C102	OK
Channel 2 C103	OK
Channel 3 C102	OK
Channel 3 C103	OK
Channel 4 C102	OK
Channel 4 C103	OK

The noise output from each channel then needs to be measured again. For convenience, these results may be added to section 13 ofthis report in place of the previous readings.

15. Noise monitor tests

Connect the 39 ohm loads, the blanking plug in place on the drive input, and the relay test box.
Switch in all filters.
Connect power, and power up the unit. Measure the noise output on the noise monitor plug in μV/root Hz, on the HP Dynamic signal Analyser, the preamplifier with a gain of 10, and Stuart Aston's noise measurement set up. Check that it is less than 3 μV/root Hz with respect to ground, which may be found on sockets number 5, 6, 7, 8 or 9.

	Noise Monitor socket pin number	**Noise**	**< 3μV/rt Hz?**
Channel 1	1	4.6	
Channel 2	2	5.1	
Channel 3	3	2.47	
Channel 4	4	1.37	

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P8……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09…………

Drive Card ID……T_TOP8P…………
Monitor Card ID...Mon28P…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

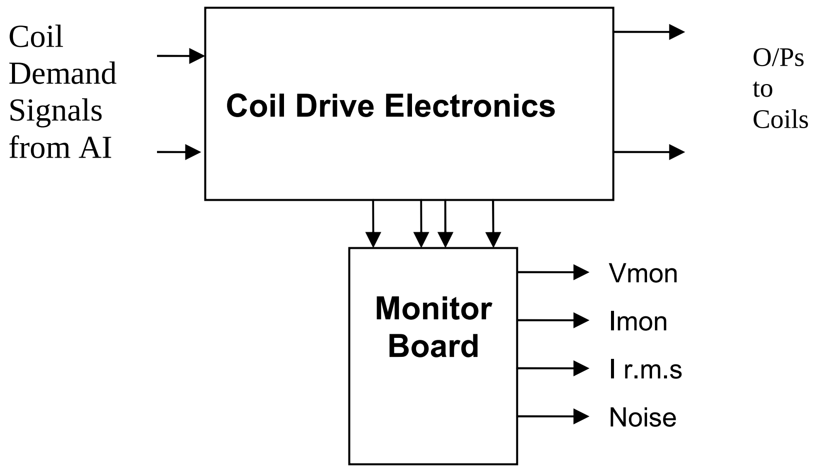


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit..................T_TOP_P8........................Serial No ....
Test Engineer ....Xen..................
Date ....23/11/09............

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	**Manufacturer**	**Model**	**Serial Number**
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P8……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………23/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Unit………………T_TOP_P8……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit..................T_TOP_P8........................Serial No ....
Test Engineer ....Xen..................
Date ....23/11/09............

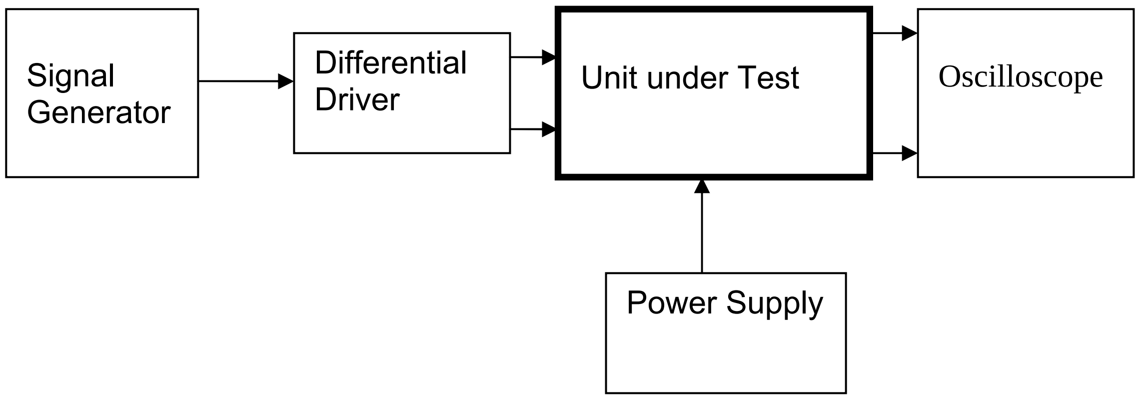
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P8........................Serial No ....
Test Engineer ....Xen..................
Date ....23/11/09............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P8……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………23/11/09………..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P8……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.759	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.749	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.758	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit……………..T_TOP_P8……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….23/11/09………..

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit..................T_TOP_P8.........................Serial No ....
Test Engineer ....Xen..................
Date ....23/11/09............

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….T_TOP_P8……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

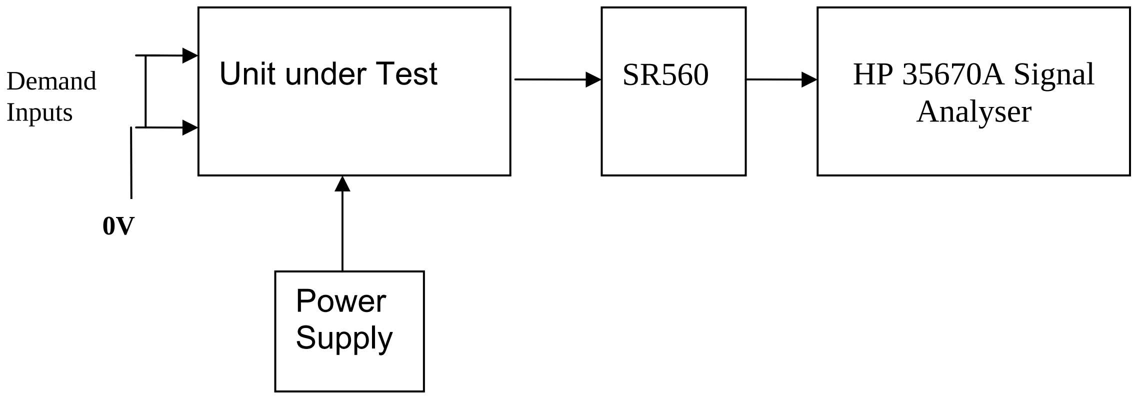
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	41.8	√
CH1 Negative		CH1 IC5	43.1	√
CH2 Positive	12.20	CH2 IC1	40.6	√
CH2 Negative		CH2 IC5	41.4	√
CH3 Positive	12.20	CH3 IC1	40.1	√
CH3 Negative		CH3 IC5	41.8	√
CH4 Positive	12.20	CH4 IC1	40.1	√
CH4 Negative		CH4 IC5	42.8	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………1/12/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-102.4	-162.4
Ch2	-160dB	-102.7	-162.7
Ch3	-160dB	-104.3	-164.3
Ch4	-160dB	-101.7	-161.7

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P8……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….23/11/09………..

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.36	85.5mA	120mA	84.8mA	√
2	39.4	3.37	85.5mA	120mA	84.8mA	√
3	39.3	3.36	85.5mA	120mA	84.8mA	√
4	39.4	3.36	85.3mA	120mA	84.8mA	√

Unit………………… T_TOP_P8…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………16/12/09

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary √ . Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	TTOPP8
Driver board ID	TTOPP8
Driver board Drawing No/Issue No	D0902747 v 6
Driver board Serial Number	TTOPP8
Monitor board ID	MON28
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON28

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

Unit………………… ………Serial No ………………………………
Test Engineer ………
Date …………………

FINAL NOISE MEASUREMENTS

Measure the noise output and noise monitor outputs of the completed unit. The extra screening provided by the enclosure protects the unit against extraneous noise, so the results will be more consistent.

If a channel exceeds the limits, replace the noisy ICs, note the work done. Re-measure and record the final result.

Output Noise

Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz (dB)	-60dB =	Measured in nV/√Hz	OK (+/-1dB) ?
Ch1	**-160 dB**	-99.3	-159.3		OK
Ch2	**-160 dB**	-97.2	-157.2		poor
Ch3	**-160 dB**	-100.5	-160.5		OK
Ch4	**-160 dB**	-100.0	-160.0		OK

Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	Output	/(Pre-amplifier gain)	Maximum value	Pass/Fail
1	20.1	2.01	**2.9 μV/√Hz**	OK
2	17.2	1.72	**2.9 μV/√Hz**	OK
3	13.3	1.33	**2.9 μV/√Hz**	OK
4	13.9	1.39	**2.9 μV/√Hz**	OK

Repair work (if any)

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P9……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….24/11/09…………

Drive Card ID……T_TOP9P…………
Monitor Card ID...Mon29P..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

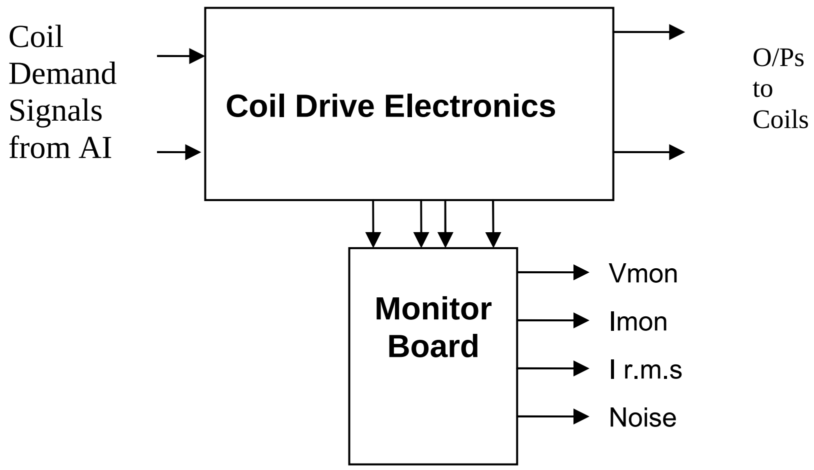


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….T_TOP_P9……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….24/11/09…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P9……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….24/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Unit………………T_TOP_P9……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….24/11/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit..................T_TOP_P9........................Serial No ....
Test Engineer ....Xen..................
Date ....24/11/09............

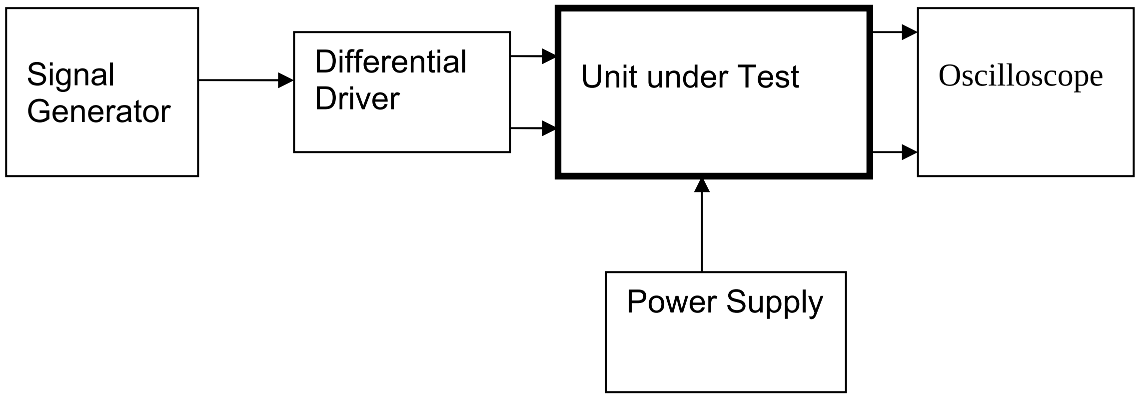
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P9........................Serial No ....
Test Engineer ....Xen..................
Date ....24/11/09............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P9……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….24/11/09………..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit..................T_TOP_P9........................Serial No ....
Test Engineer ....Xen.................
Date ....24/11/09...........

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.753	√
	Pin 1	RMS Current	0.75v dc	0.754	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.759	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit………………T_TOP_P9……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….24/11/09…………

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit.................T_TOP_P9.......................Serial No ....
Test Engineer ....Xen.................
Date ....24/11/09...........

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.7		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit…………….…T_TOP_P9……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….24/11/09………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

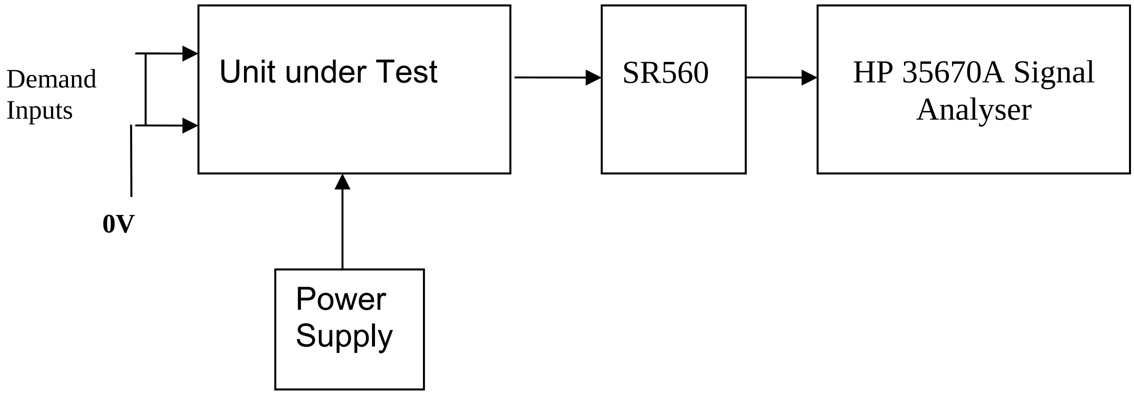
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	CH1 IC1	42.8	√
CH1 Negative		CH1 IC5	45.0	√
CH2 Positive	12.19	CH2 IC1	41.6	√
CH2 Negative		CH2 IC5	42.8	√
CH3 Positive	12.19	CH3 IC1	42.3	√
CH3 Negative		CH3 IC5	42.3	√
CH4 Positive	12.19	CH4 IC1	42.1	√
CH4 Negative		CH4 IC5	43.8	√

Unit..Serial No ....
Test Engineer ....RMC
Date 10/2/10

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.2	-159.2
Ch2	-160dB	-96.6	-156.6
Ch3	-160dB	-100.0	-160.0
Ch4	-160dB	-100.9	-160.9

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P9……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….24/11/09………..

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.36	85.5mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.35	85.2mA	120mA	84.8mA	√
4	39.4	3.35	85.0mA	120mA	84.8mA	√

Unit…………………… T_TOP_P9……………..Serial No ………………………………
Test Engineer ………RMC
Date …………………16/12/09

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. √ Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	TTOPP9
Driver board ID	TTOPP9
Driver board Drawing No/Issue No	D0903747 v6
Driver board Serial Number	TTOPP9
Monitor board ID	MON28P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON28P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

Unit……………………………………Serial No ………………………………
Test Engineer ………
Date …………………

16. Triple Top Test Plan Addendum

It was found that a problem existed on the Noise Monitor outputs. This was due to the lack of compensating capacitors on the Voltage Monitor AD797 output buffer amplifiers on the Driver Boards.

33pf capacitors need to be added to each channel in the places designated for C102 and C103.

Capacitors Added?

Channel 1 C102	OK
Channel 1 C103	OK
Channel 2 C102	OK
Channel 2 C103	OK
Channel 3 C102	OK
Channel 3 C103	OK
Channel 4 C102	OK
Channel 4 C103	OK

The noise output from each channel then needs to be measured again. For convenience, these results may be added to section 13 ofthis report in place of the previous readings.

Noise monitor tests

Connect the 39 ohm loads, the blanking plug in place on the drive input, and the relay test box.
Switch in all filters.
Connect power, and power up the unit. Measure the noise output on the noise monitor plug in µV/root Hz, on the HP Dynamic signal Analyser, the preamplifier with a gain of 10, and Stuart Aston's noise measurement set up. Check that it is less than 3 µV/root Hz with respect to ground, which may be found on sockets number 5, 6, 7, 8 or 9.

	Noise Monitor socket pin number	**Noise**	**< 3µV/rt Hz?**
Channel 1	1	2.34	OK
Channel 2	2	1.87	OK
Channel 3	3	2.29	OK
Channel 4	4	1.4	OK

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P10……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….24/11/09…………

Drive Card ID……T_TOP10P…………
Monitor Card ID...Mon30P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

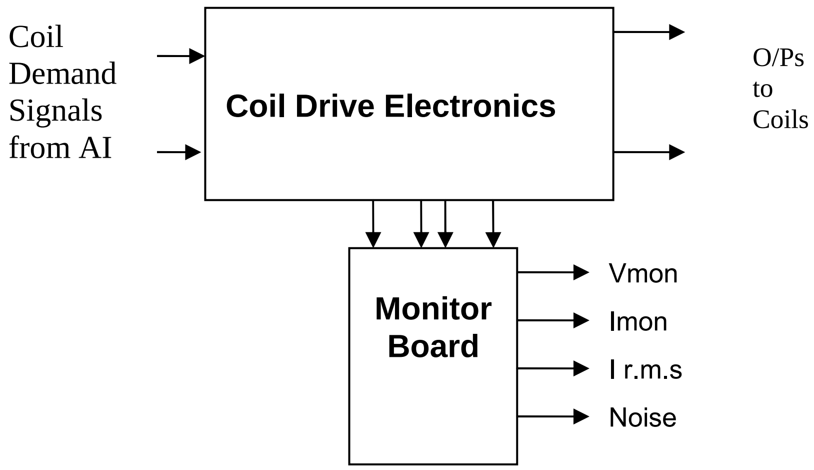


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P10……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….24/11/09…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P10……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….23/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Unit..................T_TOP_P10........................Serial No ....
Test Engineer ....Xen..................
Date ....23/11/09............

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P10……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09…………

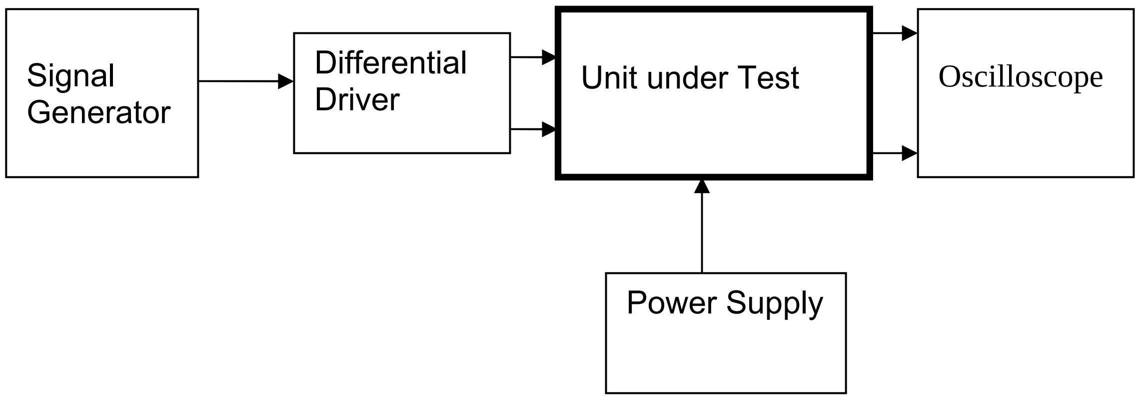
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P10........................Serial No ....
Test Engineer ....Xen.................
Date ....23/11/09...........

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit..................T_TOP_P10........................Serial No ....
Test Engineer ....Xen..................
Date ....23/11/09............

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P10……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.756	√
	Pin 1	RMS Current	0.75v dc	0.765	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.755	√
	Pin 4	RMS Current	0.75v dc	0.764	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.756	√
	Pin 7	RMS Current	0.75v dc	0.759	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.755	√
	Pin 10	RMS Current	0.75v dc	0.761	√

Unit………………T_TOP_P10……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09…………

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit……………….T_TOP_P10……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….23/11/09………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit..................T_TOP_P10...........................Serial No ....
Test Engineer ....Xen...........
Date ....24/11/09......

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.21	CH1 IC1	40.4	√
CH1 Negative		CH1 IC5	42.3	√
CH2 Positive	12.21	CH2 IC1	40.6	√
CH2 Negative		CH2 IC5	41.6	√
CH3 Positive	12.21	CH3 IC1	42.3	√
CH3 Negative		CH3 IC5	42.3	√
CH4 Positive	12.21	CH4 IC1	41.1	√
CH4 Negative		CH4 IC5	42.6	√

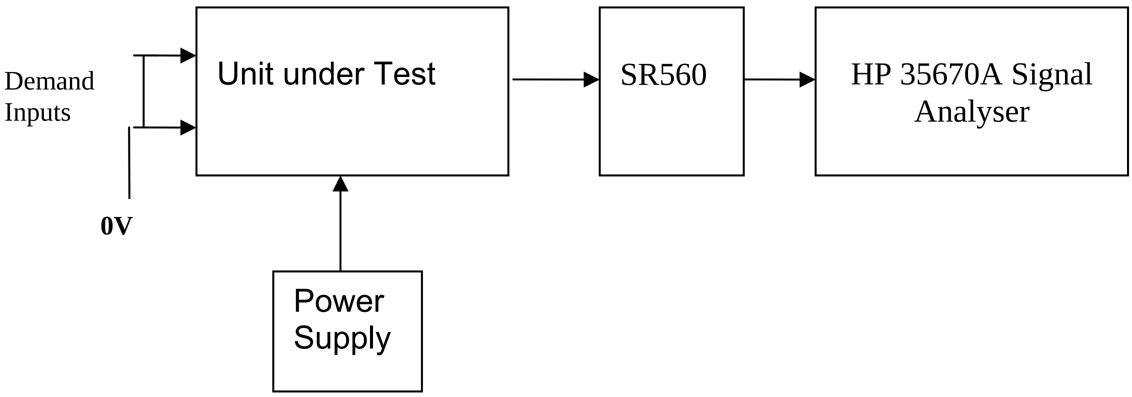
Unit.........TTOP10P................................Serial No ....
Test Engineer ....RMC
Date 10/2/10

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.2	-161.2dB
Ch2	-160dB	-96.4	-156.4dB
Ch3	-160dB	-99.5	-159.5dB
Ch4	-160dB	-99.9	-159.9dB

Note : Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Channel 2 initially noisy, so IC4 and iC8 changed (797s)

Unit……………..T_TOP_P10……………………..Serial No ………………………………
Test Engineer ….Xen………..
Date …………….24/11/09……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.35	85.2mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.35	85.2mA	120mA	84.8mA	√
4	39.4	3.35	85.0mA	120mA	84.8mA	√

Unit…………………TTOP10P……………Serial No ………………………………
Test Engineer ………RMC
Date …………………17/12/09

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. √Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	TTOP10P
Driver board ID	TTOP10P
Driver board Drawing No/Issue No	D0902747 V6
Driver board Serial Number	TTOP10P
Monitor board ID	MON30P
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON30P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………10/2/10

16. Triple Top Test Plan Addendum

It was found that a problem existed on the Noise Monitor outputs. This was due to the lack of compensating capacitors on the Voltage Monitor AD797 output buffer amplifiers on the Driver Boards.

33pf capacitors need to be added to each channel in the places designated for C102 and C103.

Capacitors Added?

Channel 1 C102	OK
Channel 1 C103	OK
Channel 2 C102	OK
Channel 2 C103	OK
Channel 3 C102	OK
Channel 3 C103	OK
Channel 4 C102	OK
Channel 4 C103	OK

The noise output from each channel then needs to be measured again. For convenience, these results may be added to section 13 ofthis report in place of the previous readings.

Noise monitor tests

Connect the 39 ohm loads, the blanking plug in place on the drive input, and the relay test box.
Switch in all filters.
Connect power, and power up the unit. Measure the noise output on the noise monitor plug in μV/root Hz, on the HP Dynamic signal Analyser, the preamplifier with a gain of 10, and Stuart Aston's noise measurement set up. Check that it is less than 3 μV/root Hz with respect to ground, which may be found on sockets number 5, 6, 7, 8 or 9.

	Noise Monitor socket pin number	**Noise** μV/√Hz	**< 3μV/rt Hz?**
Channel 1	1	1.4	OK
Channel 2	2	1.8	OK
Channel 3	3	1.825	OK
Channel 4	4	1.23	OK

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P11……………………Serial No ………………………………
Test Engineer ….Xen…..…..……..
Date …………….9/8/10…..…………

Drive Card ID……T_TOP11P…………
Monitor Card ID...Mon31P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

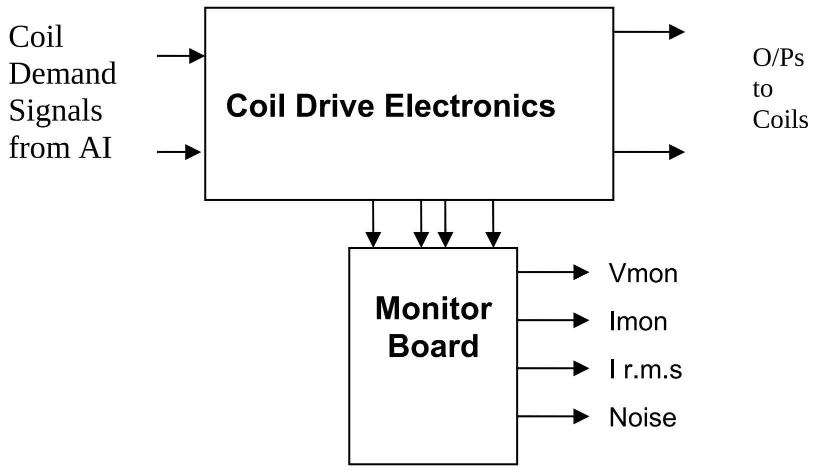


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P11……………………Serial No ………………………………
Test Engineer ….Xen…..…..………
Date …………….9/8/10…..…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_P11……………………..Serial No ……………………………….
Test Engineer ….Xen………………
Date …………….24/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH2.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………….T_TOP_P11…………………….Serial No ……………………………….
Test Engineer ….Xen……………...
Date …………….24/11/09………..

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P11……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….24/11/09…………

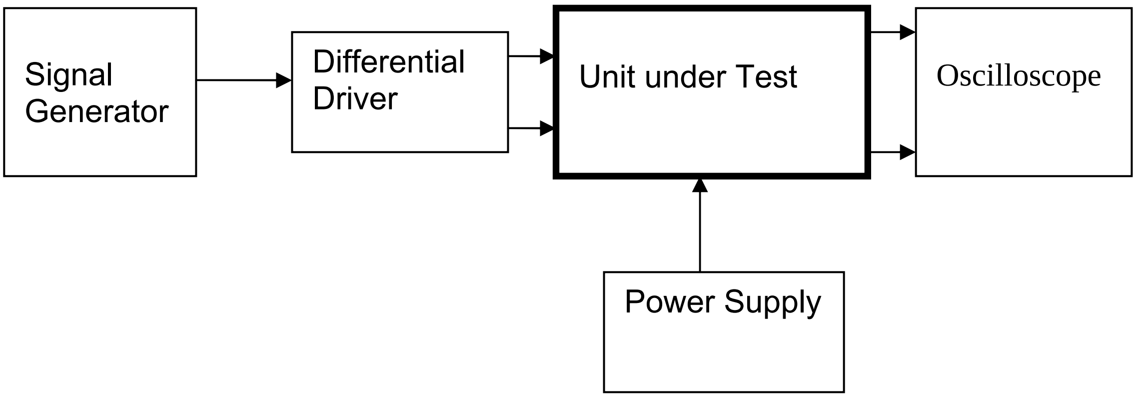
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P11……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….24/11/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P11…………………….Serial No ……………………………….
Test Engineer ….Xen……………….
Date …………….24/11/09………..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P11……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….24/11/09………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.753	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.753	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.753	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit……………..T_TOP_P11……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………24/11/09………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors
- Monitor coil inputs to board were grounded for all channels.
Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.16	2.9μV√Hz	√
2		1.05	2.9μV√Hz	√
3		0.95	2.9μV√Hz	√
4		1.74	2.9μV√Hz	√

Unit……………..T_TOP_P11……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….24/11/09………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………T_TOP_P11……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….24/11/09………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

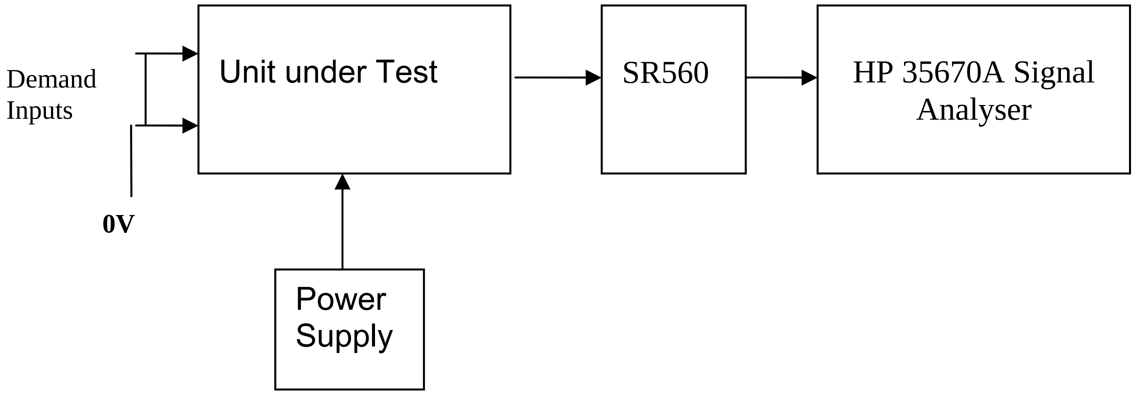
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.19	**CH1 IC1**	43.6	√
CH1 Negative		**CH1 IC5**	44.0	√
CH2 Positive	12.19	**CH2 IC1**	44.3	√
CH2 Negative		**CH2 IC5**	43.8	√
CH3 Positive	12.19	**CH3 IC1**	43.6	√
CH3 Negative		**CH3 IC5**	44.8	√
CH4 Positive	12.19	**CH4 IC1**	43.6	√
CH4 Negative		**CH4 IC5**	44.8	√

Unit.......................T_TOP_P11..................Serial No ....
Test Engineer ....RMC (1, 3 & 4) / Xen (2)
Date ....1/12/09 / 28/7/10

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.8	-161.8
Ch2	-160dB	-100.1	-160.1
Ch3	-160dB	-100.1	-160.1
Ch4	-160dB	-100.5	-160.5

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………….T_TOP_P11……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/7/10..…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.25	82.7mA	120mA	84.8mA	√
2	39.4			120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP11P…………Serial No ………………………………
Test Engineer ………RMC
Date …………………25/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP11P
Driver board ID	TTOP11P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP11P
Monitor board ID	MON31P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON31P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P12……………………Serial No ………………………………
Test Engineer ….Xen….…..……..
Date …………….9/8/10….…………

Drive Card ID……T_TOP12P…………
Monitor Card ID...Mon32P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

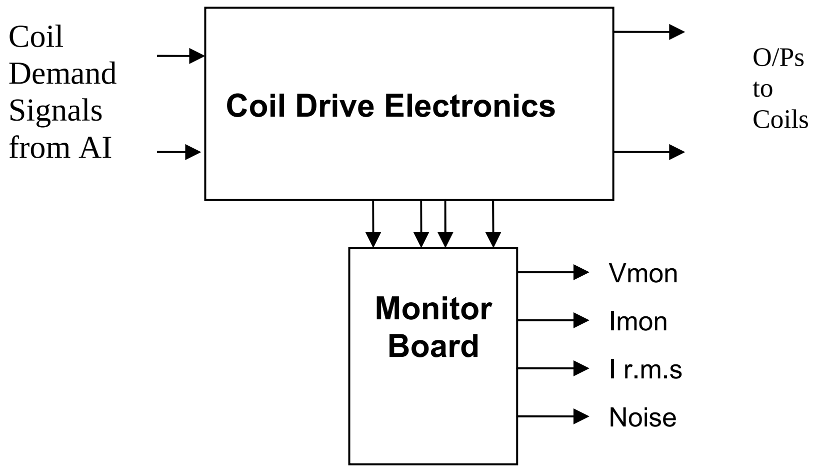


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..T_TOP_P12……………………Serial No ………………………………
Test Engineer ….Xen…..…………
Date …………….9/8/10…..……….

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P12……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………25/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P12……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….25/11/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P12……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….25/11/09…………

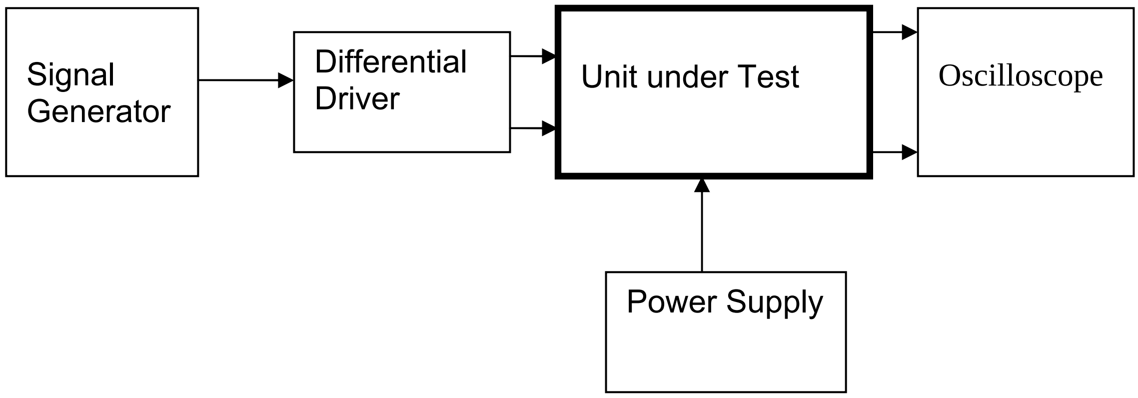
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P12........................Serial No ....
Test Engineer ....Xen..................
Date ....25/11/09............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P12……………………Serial No ………………………………
Test Engineer ….Xen……………….
Date …………….25/11/09………..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P12……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….25/11/09………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.757	√
	Pin 1	RMS Current	0.75v dc	0.758	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.755	√
	Pin 4	RMS Current	0.75v dc	0.763	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.755	√
	Pin 7	RMS Current	0.75v dc	0.752	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.754	√
	Pin 10	RMS Current	0.75v dc	0.757	√

Unit………………T_TOP_P12……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….25/11/09…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.04	2.9μV√Hz	√
2		1.76	2.9μV√Hz	√
3		1.01	2.9μV√Hz	√
4		1.14	2.9μV√Hz	√

Unit……………..T_TOP_P12…………………..Serial No ……………………………..
Test Engineer ….Xen……………..
Date …………….25/11/09………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	3.6		
10Hz	-24.2		
100Hz	-41.9		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.9		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P12……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….25/11/09………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

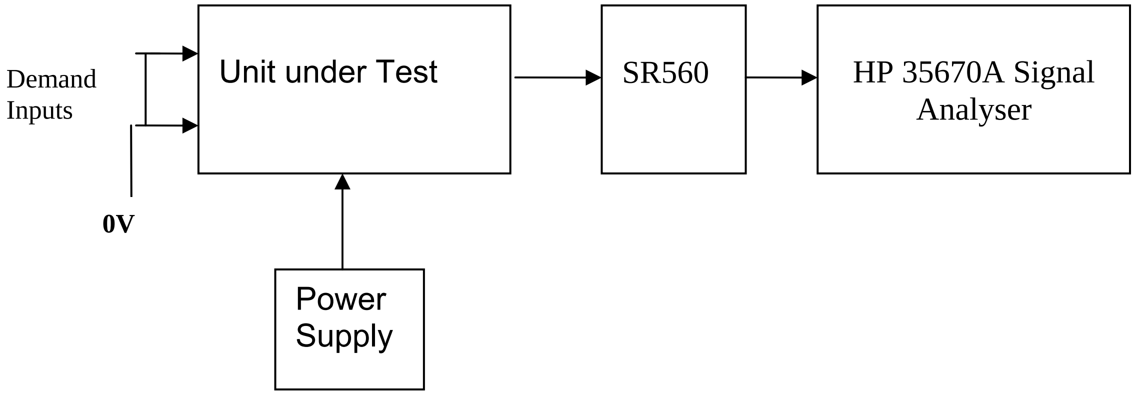
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	42.6	√
CH1 Negative		CH1 IC5	44.5	√
CH2 Positive	12.20	CH2 IC1	44.0	√
CH2 Negative		CH2 IC5	42.8	√
CH3 Positive	12.20	CH3 IC1	43.6	√
CH3 Negative		CH3 IC5	43.1	√
CH4 Positive	12.20	CH4 IC1	43.3	√
CH4 Negative		CH4 IC5	45.0	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………30/11/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-96.8	-156.8
Ch2	-160dB	-100.7	-160.7
Ch3	-160dB	-99.0	-159.0
Ch4	-160dB	-98.0	-158.0

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit..................T_TOP_P12........................Serial No ....
Test Engineer ....Xen..................
Date ....22/7/10..............

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.25	82.7mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7Ma	120mA	84.8mA	√

Unit…………………TTOP12P……………Serial No ………………………………
Test Engineer ………RMC
Date …………………25/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP12P
Driver board ID	TTOP12P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP12P
Monitor board ID	MON32P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON32P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P13……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….10/8/10…………

Drive Card ID……T_TOP13P…………
Monitor Card ID...Mon33P……………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

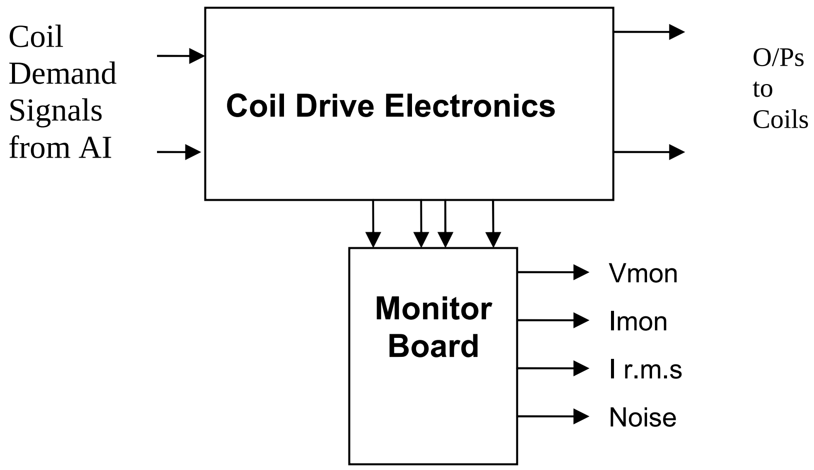


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P13……………………Serial No ………………………………
Test Engineer ….Xen………………
Date ……………10/8/10…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit.................T_TOP_P13.......................Serial No ....
Test Engineer ....Xen.................
Date ....26/11/09...........

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………….T_TOP_P13…………………….Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….26/11/09………..

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P13……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….26/11/09………..

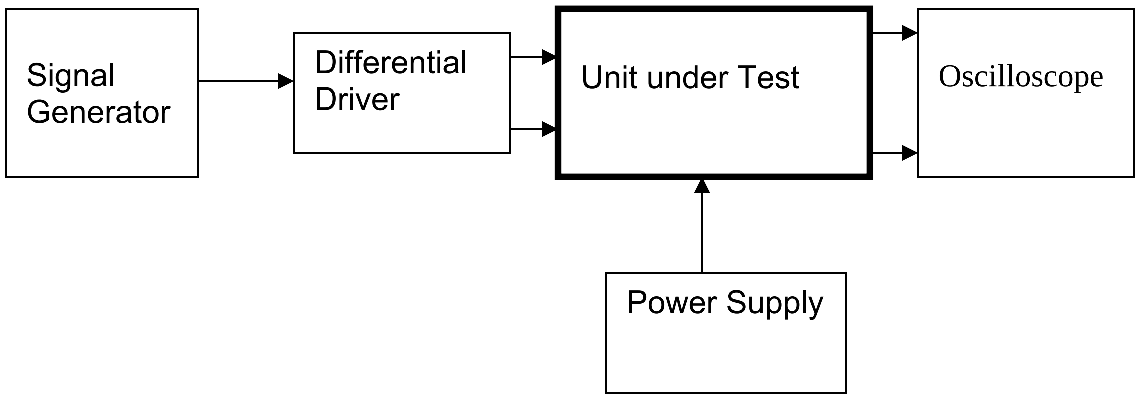
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….T_TOP_P13……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P13……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P13……………………Serial No ………………………………
Test Engineer ….Xen………………
Date ……………26/11/09…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.756	√
	Pin 1	RMS Current	0.75v dc	0.756	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.757	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.754	√
	Pin 7	RMS Current	0.75v dc	0.759	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.753	√
	Pin 10	RMS Current	0.75v dc	0.749	√

Unit……………….T_TOP_P13……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….26/11/09………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors
- Monitor coil inputs to board were grounded for all channels.
Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.43	2.9μV√Hz	√
2		1.46	2.9μV√Hz	√
3		0.92	2.9μV√Hz	√
4		1.52	2.9μV√Hz	√

Unit.................T_TOP_P13.......................Serial No ....
Test Engineer ....Xen.................
Date ....26/11/09...........

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.8		
10Hz	-30.7		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.8		
10Hz	-30.8		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.8		
10Hz	-30.8		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P13…………………..Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….26/11/09………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

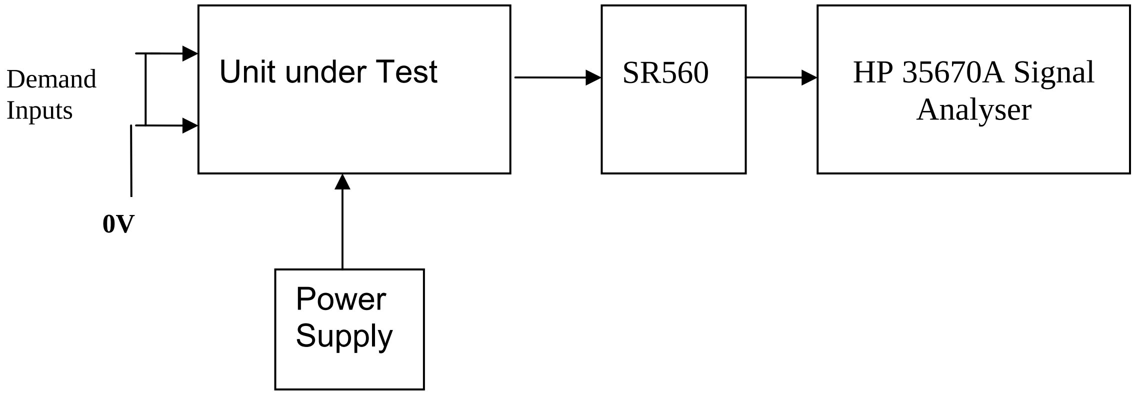
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.19	**CH1 IC1**	40.6	√
CH1 Negative		**CH1 IC5**	42.6	√
CH2 Positive	12.19	**CH2 IC1**	42.6	√
CH2 Negative		**CH2 IC5**	43.8	√
CH3 Positive	12.19	**CH3 IC1**	43.6	√
CH3 Negative		**CH3 IC5**	44.0	√
CH4 Positive	12.19	**CH4 IC1**	42.6	√
CH4 Negative		**CH4 IC5**	43.6	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………30/11/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-104.3	-164.3
Ch2	-160dB	-102.7	-162.7
Ch3	-160dB	-103.3	-163.3
Ch4	-160dB	-104.5	-164.5

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P13…………………..Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………22/7/10..…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP13P…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………25/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP13P
Driver board ID	TTOP13P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP13P
Monitor board ID	MON33P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON33P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx Advanced LIGO UK 11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P14……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….10/8/10………..

Drive Card ID……T_TOP14P…………
Monitor Card ID...Mon34P….…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

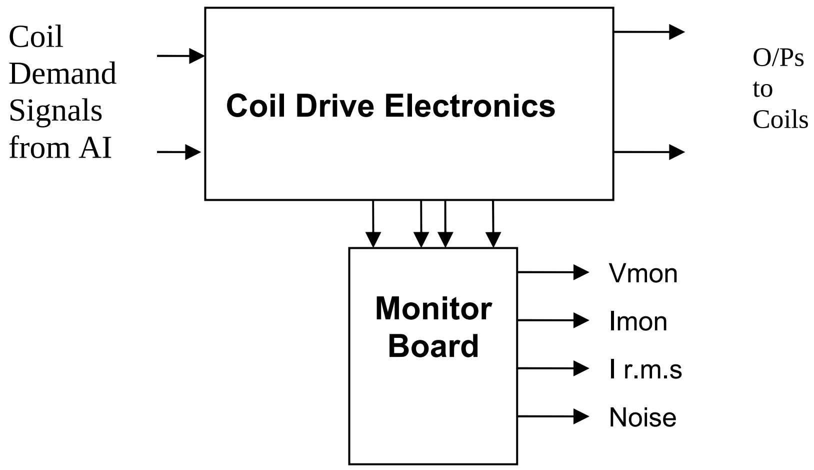


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P14……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….10/8/10…………..

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P14……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………26/11/09…………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH1.

Four 0.39uF filter capacitors have been added to the driver board (C200).
Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………….T_TOP_P14…………………….Serial No ……………………………….
Test Engineer ….Xen……………..
Date …………….26/11/09………..

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P14……………………Serial No ……………………………….
Test Engineer ….Xen……………….
Date …………….26/11/09…………

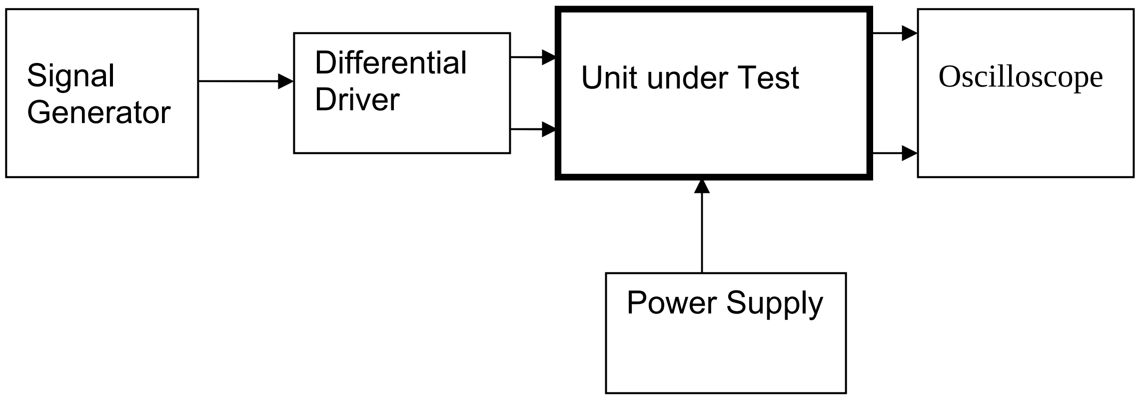
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….T_TOP_P14…………………….Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….26/11/09………..

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P14……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit.................T_TOP_P14.......................Serial No ....
Test Engineer ....Xen.................
Date ....26/11/09...........

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.755	√
	Pin 1	RMS Current	0.75v dc	0.758	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.757	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.754	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.758	√

Unit………………T_TOP_P14……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.39	2.9μV√Hz	√
2		0.95	2.9μV√Hz	√
3		1.01	2.9μV√Hz	√
4		1.37	2.9μV√Hz	√

Unit……………..T_TOP_P14…………………..Serial No ……………………………..
Test Engineer ….Xen……………..
Date ……………26/11/09………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.
With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.7		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P14……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….26/11/09………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

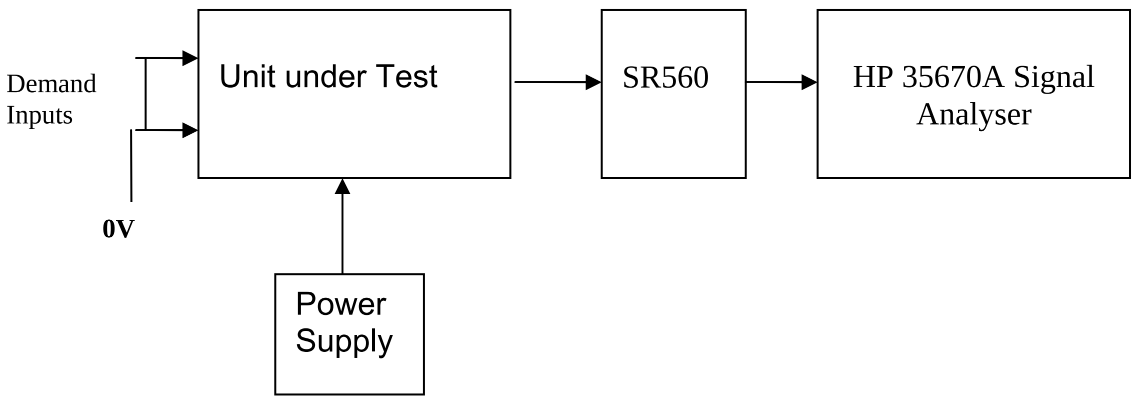
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	42.6	√
CH1 Negative		CH1 IC5	43.3	√
CH2 Positive	12.20	CH2 IC1	42.8	√
CH2 Negative		CH2 IC5	43.6	√
CH3 Positive	12.20	CH3 IC1	43.3	√
CH3 Negative		CH3 IC5	44.5	√
CH4 Positive	12.20	CH4 IC1	42.3	√
CH4 Negative		CH4 IC5	43.3	√

Unit.......................T_TOP_P14..................Serial No ....
Test Engineer ....RMC (2, 3 & 4) / Xen (1)........
Date ....30/11/09 / 28/7/10................

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-102.4	-162.4
Ch2	-160dB	-100.3	-160.3
Ch3	-160dB	-100.1	-160.1
Ch4	-160dB	-100.5	-160.5

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P14……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………26/7/10..…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification.

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.25	82.7mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………………TTOP14P………………Serial No ………………………………
Test Engineer ………RMC
Date …………………25/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP14P
Driver board ID	TTOP14P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP14P
Monitor board ID	MON34P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON34P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P15……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….22/7/10……………

Drive Card ID……T_TOP15P…………
Monitor Card ID...Mon35P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

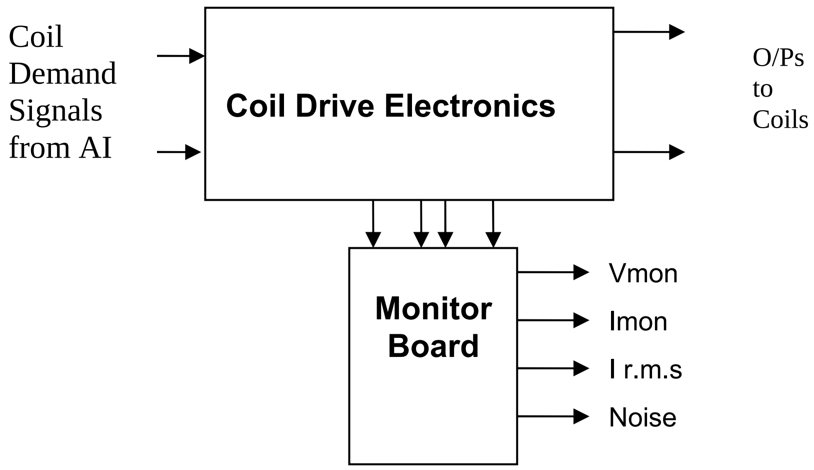


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..T_TOP_P15……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….22/7/10……………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit.................T_TOP_P15.......................Serial No ....
Test Engineer ....Xen.................
Date ....26/11/09...........

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit………………T_TOP_P15……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P15……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09…………

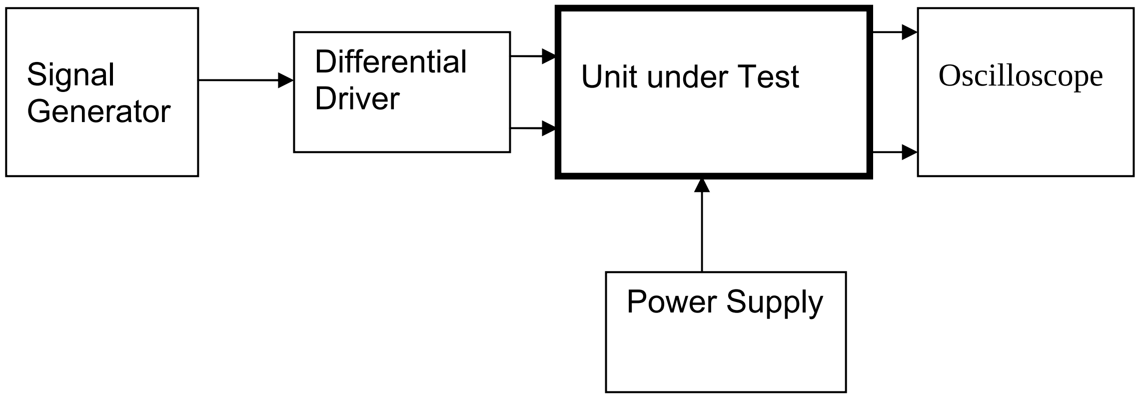
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P15……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	**- 16.5 supply current (mA)**
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	**Plus**	**Minus**
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P15……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit.................T_TOP_P15.......................Serial No ....
Test Engineer ....Xen.................
Date ....26/11/09...........

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.757	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.757	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.755	√
	Pin 7	RMS Current	0.75v dc	0.762	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit……………..T_TOP_P15…………………..Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….26/11/09………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.29	2.9μV√Hz	√
2		1.27	2.9μV√Hz	√
3		0.85	2.9μV√Hz	√
4		0.99	2.9μV√Hz	√

Unit……………..T_TOP_P15…………………..Serial No ……………………………..
Test Engineer ….Xen……………..
Date …………….26/11/09………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….T_TOP_P15…………………….Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….26/11/09…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

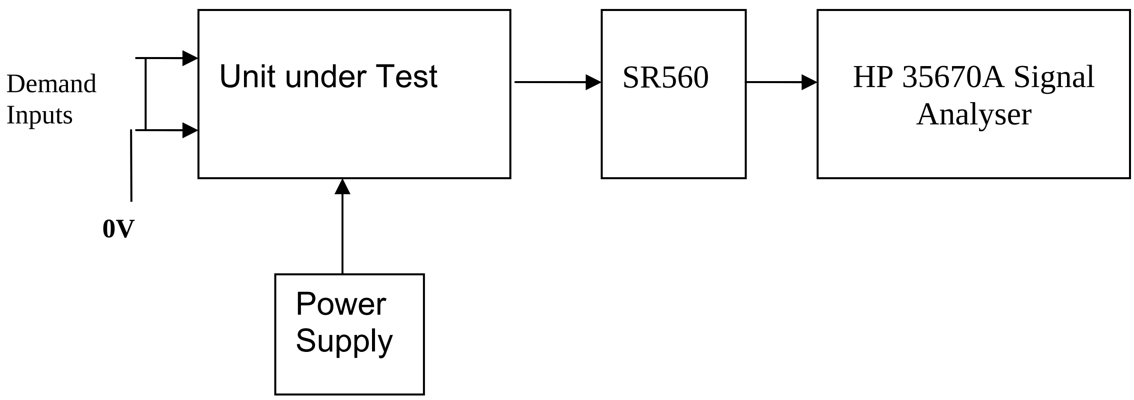
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	40.6	√
CH1 Negative		CH1 IC5	44.5	√
CH2 Positive	12.20	CH2 IC1	43.6	√
CH2 Negative		CH2 IC5	42.6	√
CH3 Positive	12.20	CH3 IC1	43.6	√
CH3 Negative		CH3 IC5	43.8	√
CH4 Positive	12.20	CH4 IC1	42.6	√
CH4 Negative		CH4 IC5	42.6	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………1/12/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.0	-160
Ch2	-160dB	-98.0	-158
Ch3	-160dB	-100.3	-160.3
Ch4	-160dB	-100.7	-160.7

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P15……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….22/7/10..…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s) +/- 2.5mA**	**Pass?**
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.27	83.0mA	120mA	84.8mA	√

Unit……………………………………Serial No ………………………………
Test Engineer ………
Date …………………

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below: √

UoB box ID	TTOP15P
Driver board ID	TTOP15P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP15P
Monitor board ID	MON35P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON35P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P16……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09…………

Drive Card ID……T_TOP16P…………
Monitor Card ID...Mon36P….…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

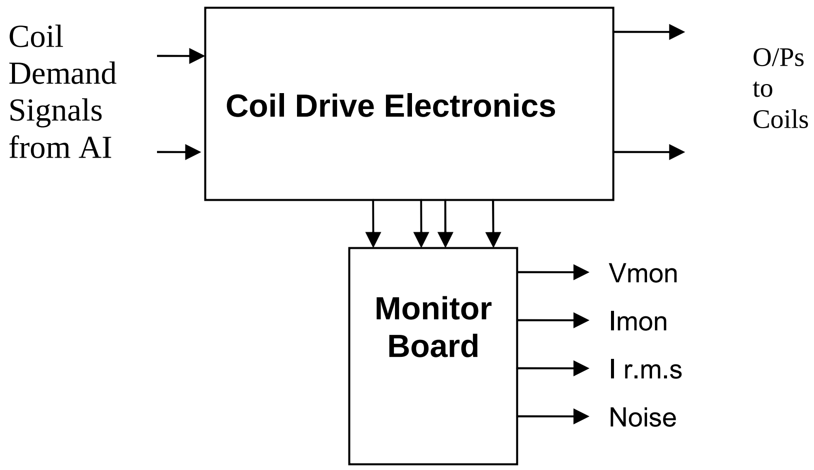


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P16……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P16……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….26/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Removed capacitors C102, C103, C104, and C105 on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Unit..................T_TOP_P16........................Serial No ....
Test Engineer ....Xen..................
Date ....26/11/09............

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P16……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09………..

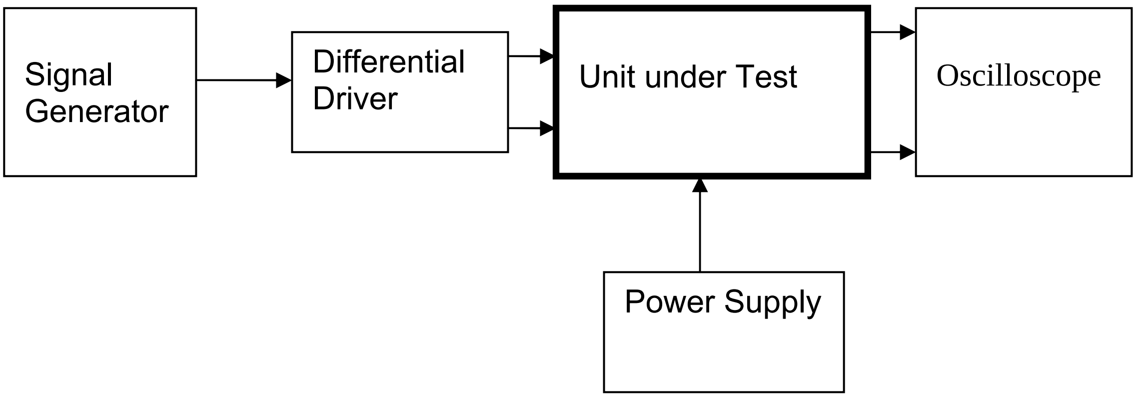
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P16……………………Serial No ………………………………
Test Engineer ….Xen………………
Date ……………26/11/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit..................T_TOP_P16........................Serial No ....
Test Engineer ....Xen..................
Date ....26/11/09............

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit.................T_TOP_P16.......................Serial No ....
Test Engineer ....Xen.................
Date ....26/11/09...........

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.751	√
	Pin 1	RMS Current	0.75v dc	0.749	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.748	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.757	√

Unit………………T_TOP_P16……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….26/11/09………..

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	**Output**	**/(Pre-amplifier gain)**	**Maximum value**	**Pass/Fail**
1	17.1	1.71	2.9	Pass
2	19.0	1.90	2.9	Pass
3	14.5	1.45	2.9	Pass
4	14.9	1.49	2.9	Pass

Unit…………………T_TOP_P16………………………Serial No ……………………………………
Test Engineer ….Xen………………
Date …………….26/11/09………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.7		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.7		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit..................T_TOP_P16........................Serial No ....
Test Engineer ....Xen..................
Date ....26/11/09............

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

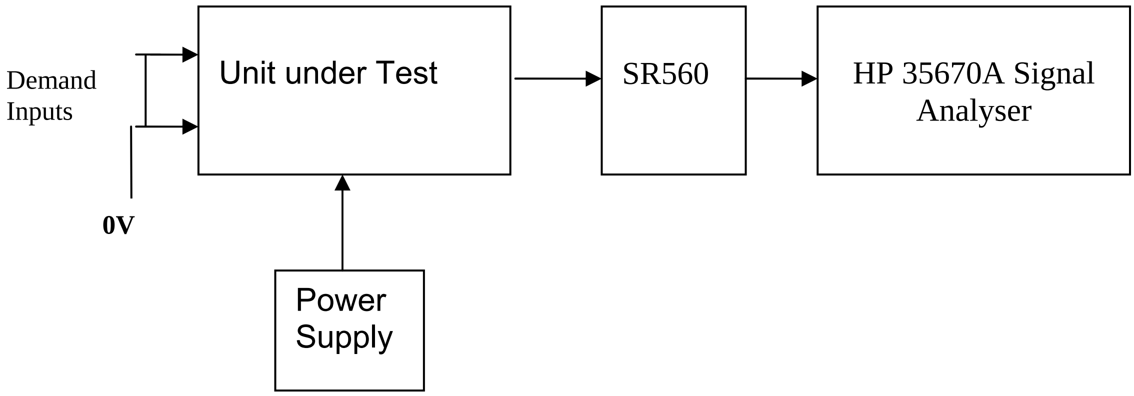
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.20	**CH1 IC1**	41.1	√
CH1 Negative		**CH1 IC5**	41.6	√
CH2 Positive	12.20	**CH2 IC1**	41.8	√
CH2 Negative		**CH2 IC5**	43.1	√
CH3 Positive	12.20	**CH3 IC1**	41.8	√
CH3 Negative		**CH3 IC5**	41.8	√
CH4 Positive	12.20	**CH4 IC1**	42.1	√
CH4 Negative		**CH4 IC5**	42.8	√

Unit………… TTOP16P ………………………….Serial No ……………………………….
Test Engineer ………RMC
Date …………………30/11/9

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.2	-160.2
Ch2	-160dB	-100.0	-160.0
Ch3	-160dB	-100.5	-160.5
Ch4	-160dB	-99.7	-159.7

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit.................T_TOP_P16.......................Serial No ....
Test Engineer ....Xen.................
Date ....26/11/09...........

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.36	85.5mA	120mA	84.8mA	√
2	39.4	3.37	85.5mA	120mA	84.8mA	√
3	39.3	3.36	85.5mA	120mA	84.8mA	√
4	39.4	3.36	85.3mA	120mA	84.8mA	√

Unit………… TTOP16P …………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………9/4/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP16P
Driver board ID	TTOP16P
Driver board Drawing No/Issue No	D0902747 V 6
Driver board Serial Number	TTOP16P
Monitor board ID	MON36(P)
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON36(P)

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P17……………………Serial No ………………………………
Test Engineer ….Xen…..……….
Date …………….9/8/10….…………

Drive Card ID……T_TOP17P…………
Monitor Card ID...Mon37P….…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

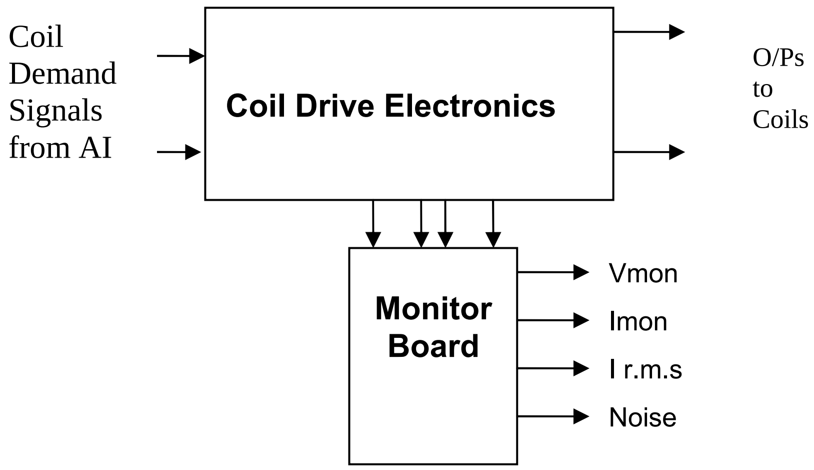


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P17……………………Serial No ………………………………
Test Engineer ….Xen…..……….
Date …………….9/8/10……………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P17……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….27/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 3 & 4.

Four 0.39uF filter capacitors have been added to the driver board (C200).
Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………..T_TOP_P17……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….27/11/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit..................T_TOP_P17........................Serial No ....
Test Engineer ....Xen..................
Date ....27/11/09............

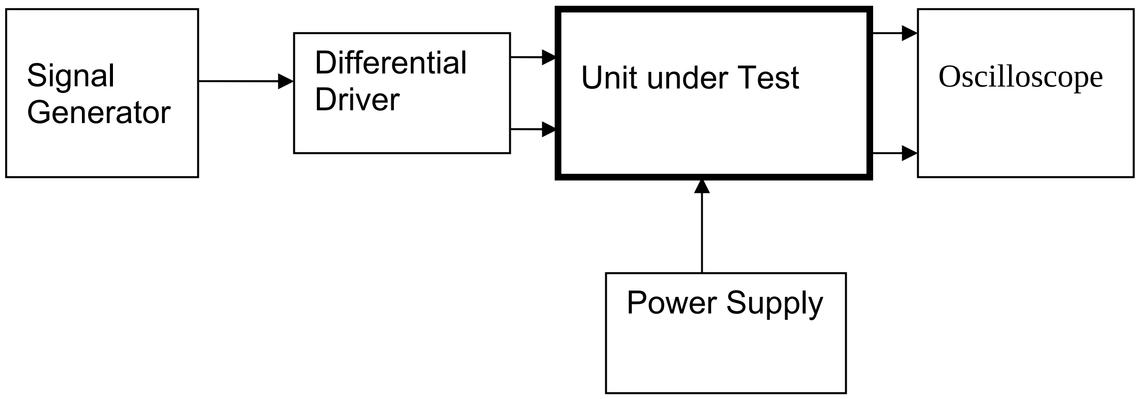
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)
Pd In from Sat pin 9, 10 = +16.5v or DC in A1
Pd In from Sat pin 11, 12 = -16.5 or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v or DC in A2

Coil Drive Outputs
Ch1+ = Coil out to Sat pin 1 Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3 Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5 Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7 Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P17……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….27/11/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P17……………………Serial No ………………………………
Test Engineer ….Xen………………
Date ……………27/11/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P17……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………27/11/09………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.757	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.754	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit……………..T_TOP_P17……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….27/11/09…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in µV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9µV√Hz out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		0.85	2.9µV√Hz	√
2		1.66	2.9µV√Hz	√
3		1.97	2.9µV√Hz	√
4		0.98	2.9µV√Hz	√

Unit……………..T_TOP_P17……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………27/11/09……….

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.
With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.7		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………...T_TOP_P17……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………27/11/09………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

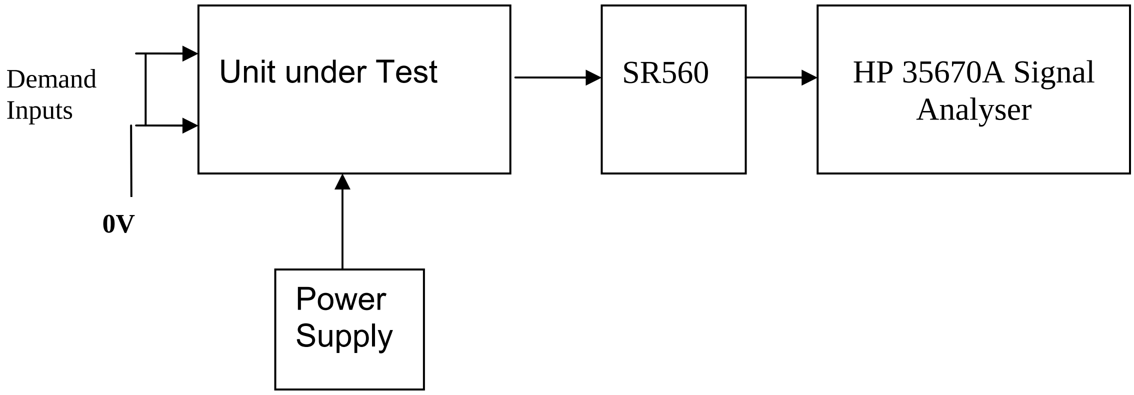
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	40.6	√
CH1 Negative		CH1 IC5	43.8	√
CH2 Positive	12.20	CH2 IC1	42.6	√
CH2 Negative		CH2 IC5	43.3	√
CH3 Positive	12.20	CH3 IC1	43.8	√
CH3 Negative		CH3 IC5	45.7	√
CH4 Positive	12.20	CH4 IC1	42.1	√
CH4 Negative		CH4 IC5	44.8	√

Unit.................T_TOP_P17........................Serial No ....
Test Engineer ....Xen..................
Date ....29/7/10..............

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.7	-159.7
Ch2	-160dB	-100.6	-160.6
Ch3	-160dB	-102.6	-162.6
Ch4	-160dB	-102.9	-162.9

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………….T_TOP_P17……………………..Serial No ……………………………….
Test Engineer ….Xen………………
Date …………….26/7/10..…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP17P…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………24/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP17P
Driver board ID	TTOP17P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP17P
Monitor board ID	MON37P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON37P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx Advanced LIGO UK 11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..…..………
Date …………….9/8/10….…………

Drive Card ID……T_TOP18P…………
Monitor Card ID...Mon38P….…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

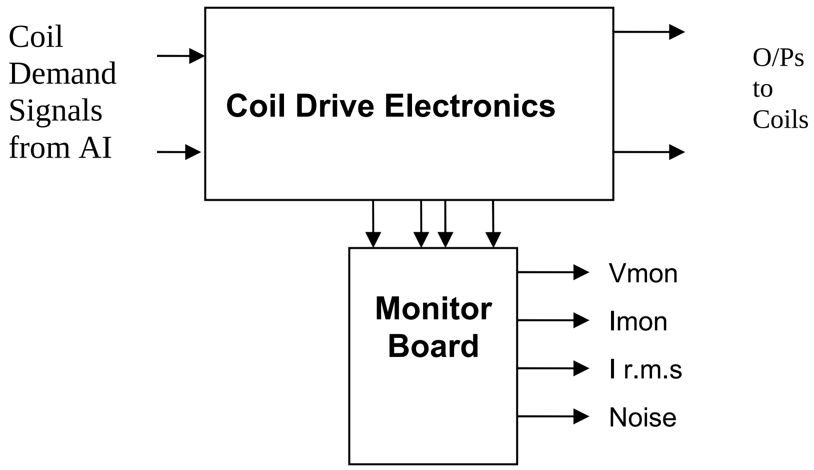


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..…..………
Date …………….9/8/10…..…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..….………
Date …………….30/11/09…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH1.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..……………
Date …………….30/11/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..…………
Date …………….30/11/09…………

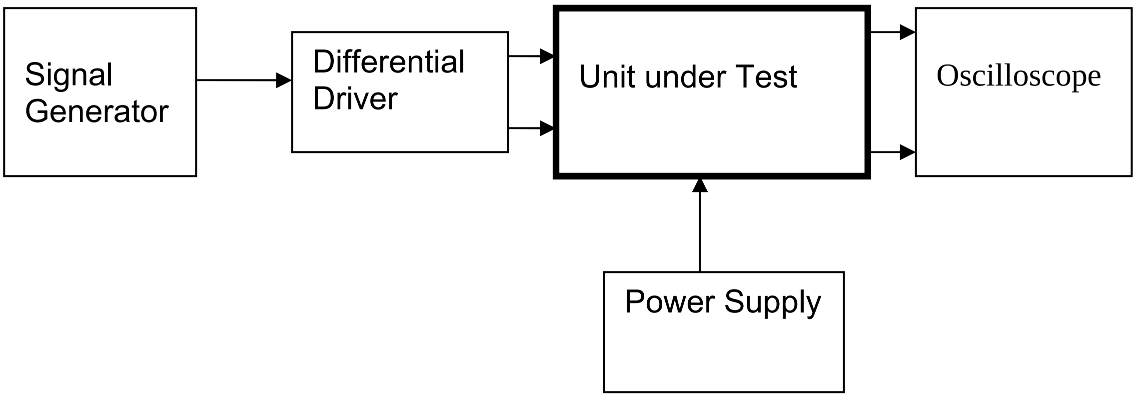
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..……………
Date …………….30/11/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen……………….
Date …………….30/11/09………..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..…………
Date …………….1/12/09…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.755	√
	Pin 1	RMS Current	0.75v dc	0.759	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.754	√
	Pin 4	RMS Current	0.75v dc	0.760	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.755	√
	Pin 7	RMS Current	0.75v dc	0.758	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit……………..T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..…………
Date …………….1/12/09…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.31	2.9μV√Hz	√
2		1.33	2.9μV√Hz	√
3		1.22	2.9μV√Hz	√
4		1.06	2.9μV√Hz	√

Unit……………..T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..…………
Date …………….1/12/09…………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..…………
Date …………….1/12/09…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	CH1 IC1	41.1	√
CH1 Negative		CH1 IC5	42.3	√
CH2 Positive	12.19	CH2 IC1	43.3	√
CH2 Negative		CH2 IC5	41.8	√
CH3 Positive	12.19	CH3 IC1	42.1	√
CH3 Negative		CH3 IC5	42.6	√
CH4 Positive	12.19	CH4 IC1	41.6	√
CH4 Negative		CH4 IC5	42.8	√

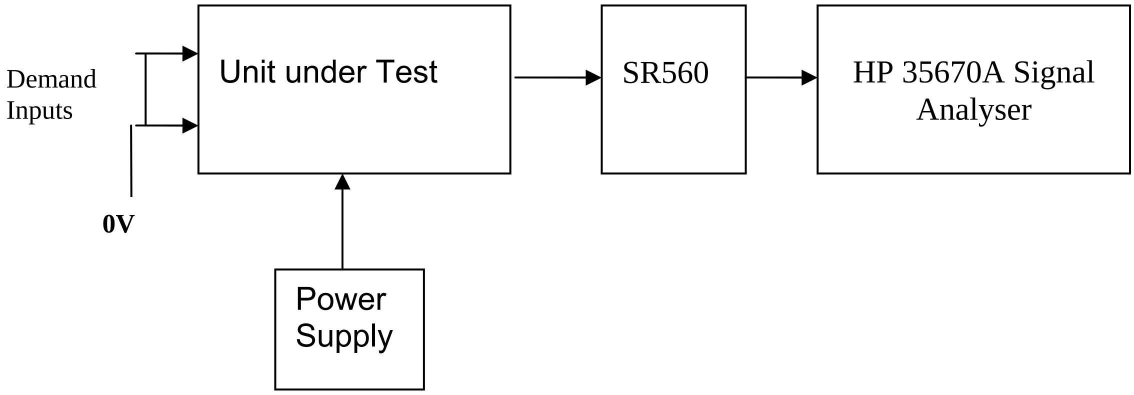
Unit……………….T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….28/7/10…………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-160dB	-101.1	-161.1
Ch2	-160dB	-101.2	-161.2
Ch3	-160dB	-99.2	-159.2
Ch4	-160dB	-98.7	-158.7

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P18……………………Serial No ………………………………
Test Engineer ….Xen…..……………
Date …………….26/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit………………… TTOP18P …………………Serial No ………………………………
Test Engineer ………RMC
Date …………………24/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP18P
Driver board ID	TTOP18P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP18P
Monitor board ID	MON38P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON38P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen…..….………
Date …………….9/8/10…..…………

Drive Card ID……T_TOP19P…………
Monitor Card ID...Mon39P….…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

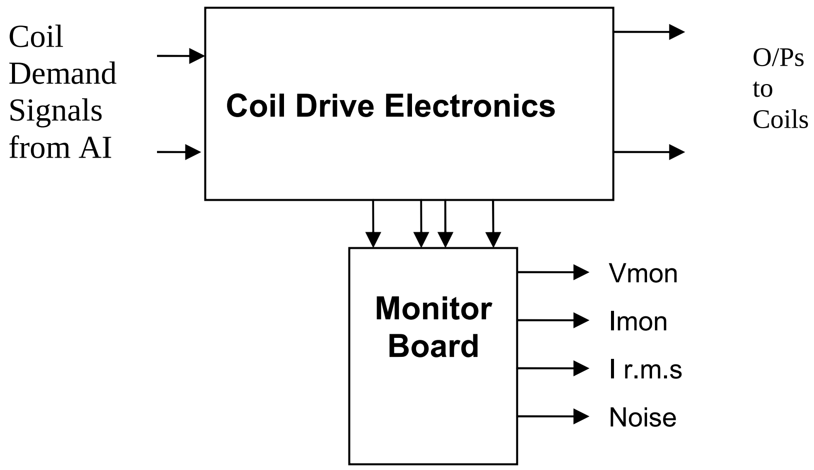


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen…..…………
Date …………….9/8/10…..………..

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….2/12/09…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………..T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/12/09………..

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/12/09…………

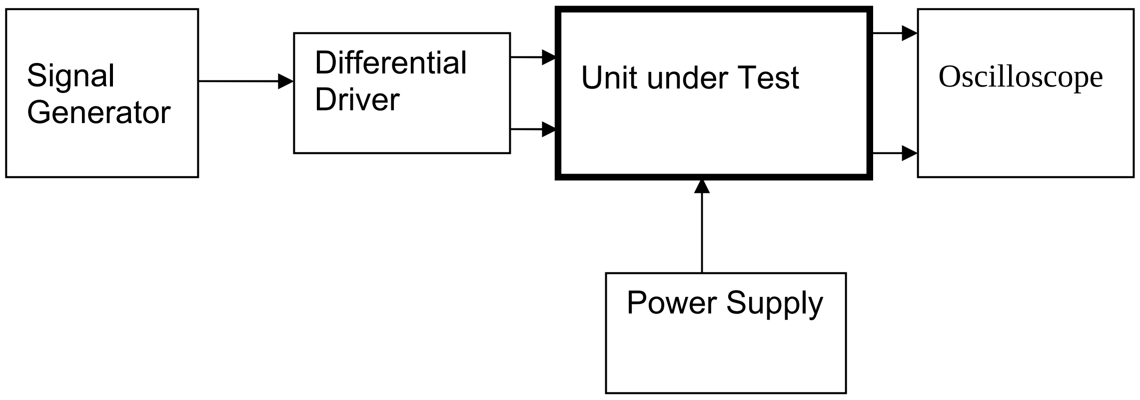
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….2/12/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date …………….2/12/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/12/09………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.753	√
	Pin 1	RMS Current	0.75v dc	0.753	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.750	√
	Pin 4	RMS Current	0.75v dc	0.752	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.755	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.756	√

Unit……………..T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/12/09………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.41	2.9μV√Hz	√
2		0.86	2.9μV√Hz	√
3		1.05	2.9μV√Hz	√
4		1.37	2.9μV√Hz	√

Unit.................T_TOP_P19.......................Serial No ....
Test Engineer ....Xen................
Date ....2/12/09...........

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.7		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/12/09…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	CH1 IC1	41.8	√
CH1 Negative		CH1 IC5	44.5	√
CH2 Positive	12.19	CH2 IC1	43.1	√
CH2 Negative		CH2 IC5	43.1	√
CH3 Positive	12.19	CH3 IC1	43.8	√
CH3 Negative		CH3 IC5	46.7	√
CH4 Positive	12.19	CH4 IC1	43.1	√
CH4 Negative		CH4 IC5	42.8	√

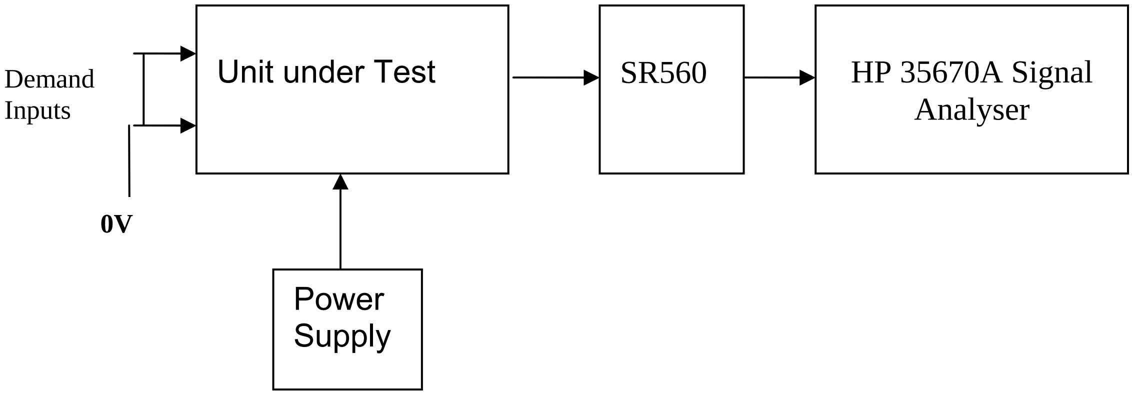
Unit..................T_TOP_P19........................Serial No ....
Test Engineer ....Xen................
Date ....23/7/10............

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.9	-161.9
Ch2	-160dB	-100.0	-160.0
Ch3	-160dB	-101.3	-161.3
Ch4	-160dB	-101.6	-161.6

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P19……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….23/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.28	83.2mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit………T Top 19 P……………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………12/1/10

PROBLEM REPORT

Problems
During the noise tests, the unit had excess noise on Channel 4.

Cause
The problem was expected to be due to noisy AD797s, IC4 and IC8

Solution
These ICs needed to be replaced.

Action
These ICs were replaced.

Confirmation
A frequency response test, and a noise test were performed.
Noise levels and frequency response were both nominal. The results of the noise test were recorded on page 16 of this report.

Unit……………………TTOP19P………………Serial No ………………………………
Test Engineer ………RMC
Date …………………24/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP19P
Driver board ID	TTOP19P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP19P
Monitor board ID	MON39P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON39P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P20……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….10/8/10…………

Drive Card ID……T_TOP20P…………
Monitor Card ID...Mon40P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

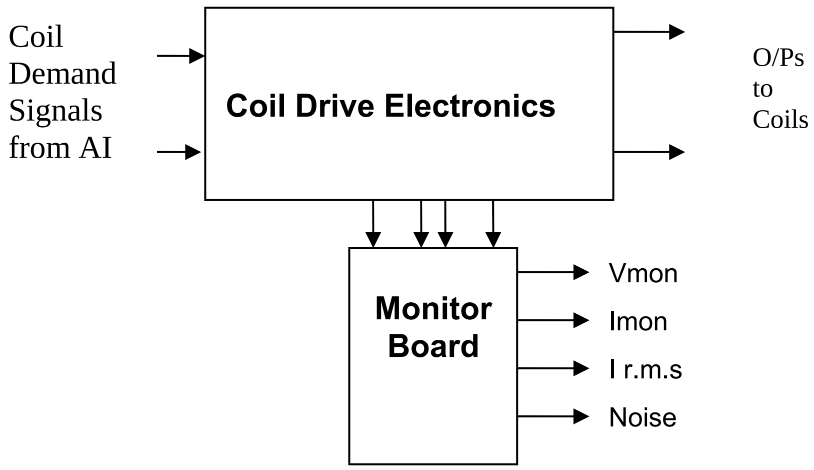


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit..................T_TOP_P20........................Serial No ....
Test Engineer ....Xen.................
Date ....10/8/10............

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P20……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date ……………2/12/09………..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 1 & 4.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………….T_TOP_P20…………………….Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/12/09………..

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………..T_TOP_P20……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/12/09…………

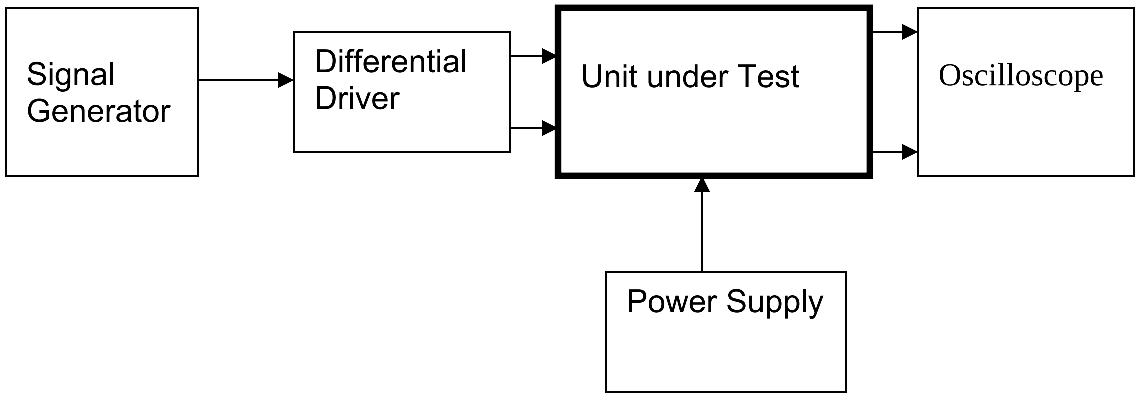
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….T_TOP_P20……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….2/12/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P20……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….2/12/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P20……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/12/09…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.755	√
	Pin 1	RMS Current	0.75v dc	0.758	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.754	√
	Pin 4	RMS Current	0.75v dc	0.754	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.754	√
	Pin 7	RMS Current	0.75v dc	0.760	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit……………..T_TOP_P20……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….2/12/09…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors
- Monitor coil inputs to board were grounded for all channels.
Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		0.88	2.9μV√Hz	√
2		1.50	2.9μV√Hz	√
3		1.60	2.9μV√Hz	√
4		0.93	2.9μV√Hz	√

Unit……………..T_TOP_P20……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….2/12/09………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	3.4		
10Hz	-25.0		
100Hz	-42.0		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.9		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P20……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/12/09…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

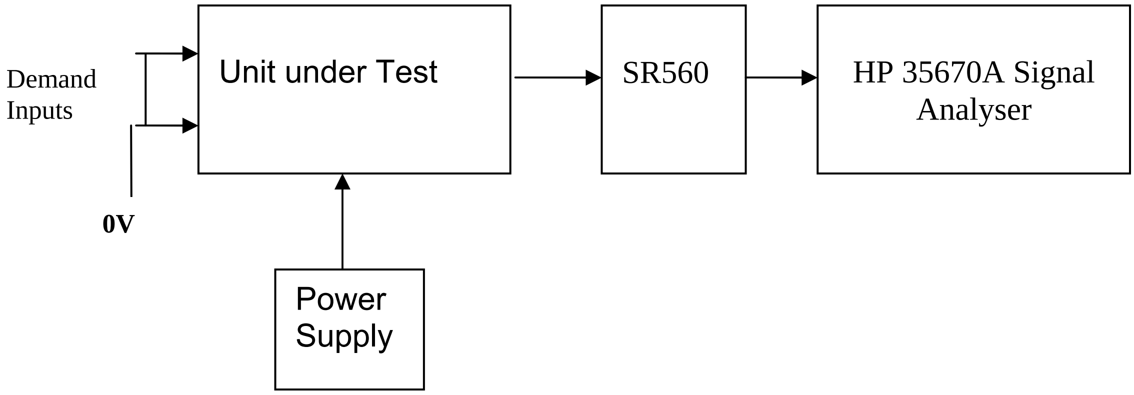
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.17	CH1 IC1	41.4	√
CH1 Negative		CH1 IC5	43.6	√
CH2 Positive	12.17	CH2 IC1	43.3	√
CH2 Negative		CH2 IC5	42.8	√
CH3 Positive	12.17	CH3 IC1	44.3	√
CH3 Negative		CH3 IC5	45.5	√
CH4 Positive	12.17	CH4 IC1	42.8	√
CH4 Negative		CH4 IC5	44.3	√

Unit.................T_TOP_P20.......................Serial No ....
Test Engineer ....Xen................
Date ....29/7/10...........

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.1	-161.1
Ch2	-160dB	-99.8	-159.8
Ch3	-160dB	-100.0	-160.0
Ch4	-160dB	-102.4	-162.4

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P20……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….27/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

-

Unit…………………TTOP20P……………Serial No ………………………………
Test Engineer ………RMC
Date …………………24/8/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP20P
Driver board ID	TTOP20P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP20P
Monitor board ID	MON40P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON40P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P21……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….10/9/10…………

Drive Card ID……T_TOP21P…………
Monitor Card ID...Mon41P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

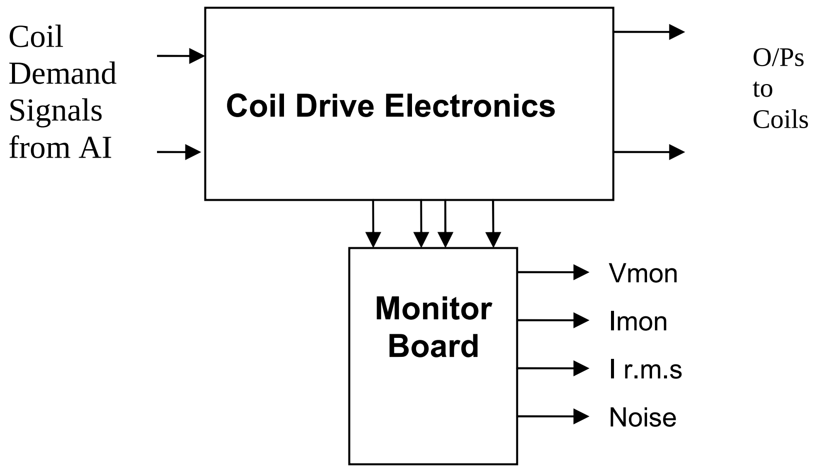


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P21……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….10/9/10…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit.................T_TOP_P21........................Serial No ....
Test Engineer ....Xen.................
Date ....1/12/09............

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P21……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….1/12/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit..................T_TOP_P21........................Serial No ....
Test Engineer ....Xen.................
Date ....1/12/09............

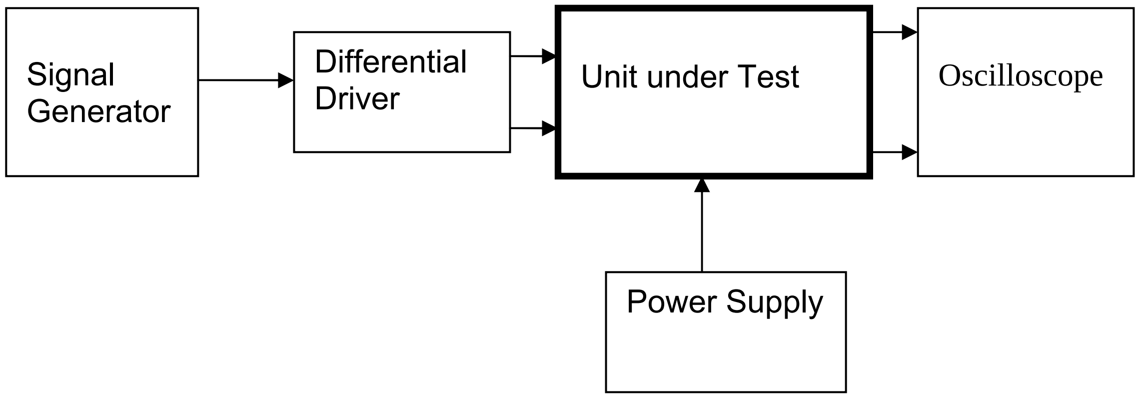
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit…………………T_TOP_P21………………………Serial No ………………………………….
Test Engineer ….Xen…………….
Date ………………1/12/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit..................T_TOP_P21........................Serial No ....
Test Engineer ....Xen.................
Date ....1/12/09............

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit.................T_TOP_P21.......................Serial No ....
Test Engineer ....Xen................
Date ....1/12/09...........

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.758	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.750	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.752	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit..................T_TOP_P21........................Serial No ....
Test Engineer ....Xen................
Date ....22/7/10............

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.74	2.9μV√Hz	√
2		0.96	2.9μV√Hz	√
3		1.57	2.9μV√Hz	√
4		0.77	2.9μV√Hz	√

Unit……………..T_TOP_P21……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….1/12/09…………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit.................T_TOP_P21.......................Serial No ....
Test Engineer ....Xen................
Date ....1/12/09...........

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

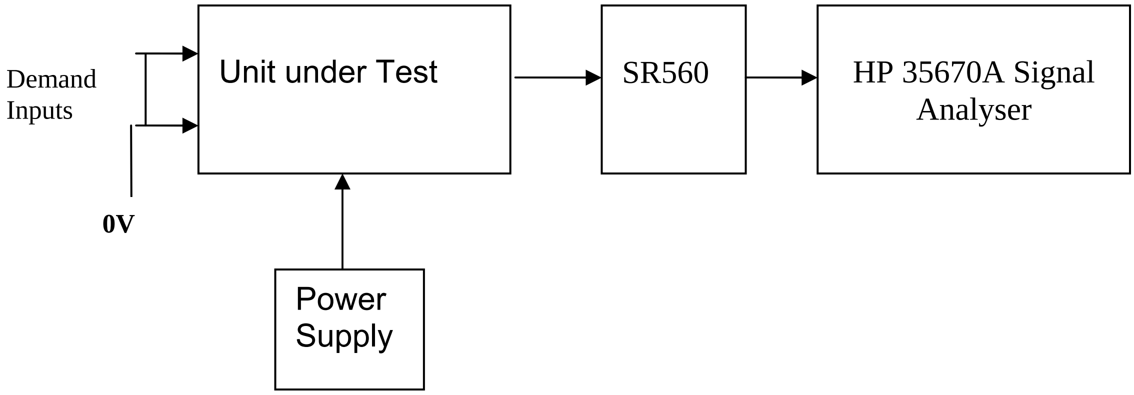
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.17	CH1 IC1	41.1	√
CH1 Negative		CH1 IC5	42.6	√
CH2 Positive	12.17	CH2 IC1	41.6	√
CH2 Negative		CH2 IC5	42.3	√
CH3 Positive	12.17	CH3 IC1	43.6	√
CH3 Negative		CH3 IC5	44.0	√
CH4 Positive	12.17	CH4 IC1	41.8	√
CH4 Negative		CH4 IC5	42.3	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………8/12/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-98.2	-158.2
Ch2	-160dB	-97.1	-157.1
Ch3	-160dB	-101.5	-161.5
Ch4	-160dB	-99.27	-159.2

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P21……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….22/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………………TTOP21P……………..Serial No ……………………………
Test Engineer ………RMC
Date …………………24/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP21P
Driver board ID	TTOP21P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP21P
Monitor board ID	MON41P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON41P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P22……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….28/7/10…..………

Drive Card ID……T_TOP22P…………
Monitor Card ID...Mon42P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

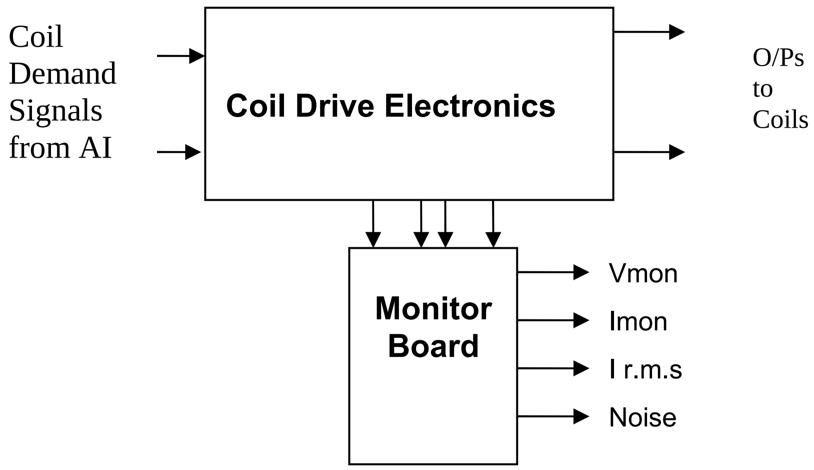


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P22……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….28/7/10…..………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P22……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………1/12/09…..………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 1 & 2.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit..................T_TOP_P22........................Serial No ....
Test Engineer ....Xen..................
Date ....1/12/09.............

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………..T_TOP_P22……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….1/12/09…..………

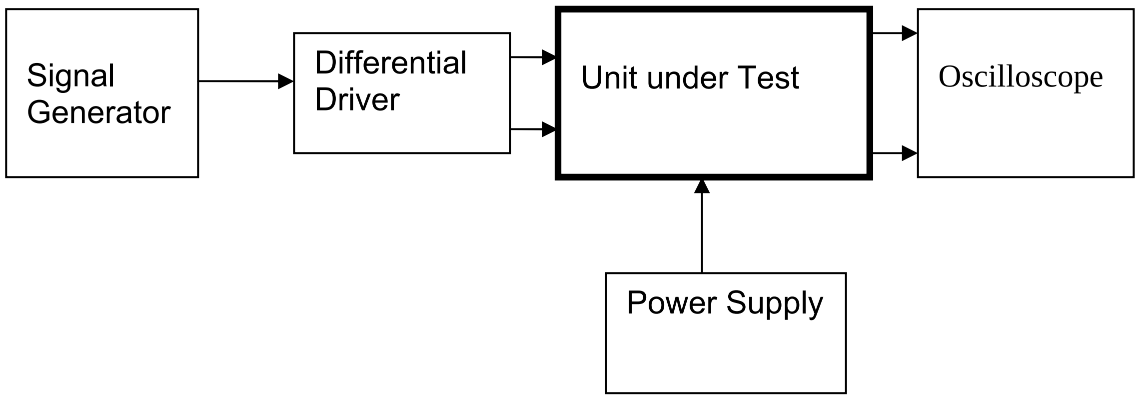
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….T_TOP_P22……………………Serial No ………………………………
Test Engineer ….Xen……………….
Date …………….1/12/09…..………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P22……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….1/12/09…...……..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P22……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….1/12/09…..………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.757	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.758	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.754	√
	Pin 7	RMS Current	0.75v dc	0.753	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit……………….T_TOP_P22……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….1/12/09…..………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		0.92	2.9μV√Hz	√
2		1.42	2.9μV√Hz	√
3		0.94	2.9μV√Hz	√
4		0.88	2.9μV√Hz	√

Unit……………..T_TOP_P22…………………..Serial No ……………………………..
Test Engineer ….Xen……………..
Date …………….1/12/09….……..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P22……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….1/12/09…..………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

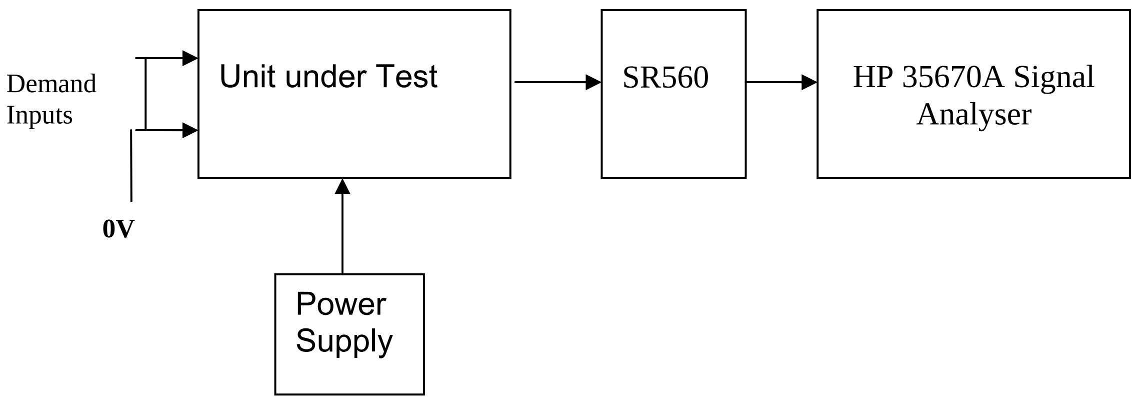
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.17	CH1 IC1	41.1	√
CH1 Negative		CH1 IC5	44.8	√
CH2 Positive	12.17	CH2 IC1	42.3	√
CH2 Negative		CH2 IC5	43.1	√
CH3 Positive	12.17	CH3 IC1	43.8	√
CH3 Negative		CH3 IC5	44.8	√
CH4 Positive	12.17	CH4 IC1	43.1	√
CH4 Negative		CH4 IC5	42.3	√

Unit……………...T_TOP_P22……………………Serial No ………………………………
Test Engineer …RMC (3 & 4) / Xen (1 & 2)………
Date ……………28/7/10…………………………..……

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.5	-160.5
Ch2	-160dB	-100.4	-160.4
Ch3	-160dB	-98	-158
Ch4	-160dB	-98.2	-158.2

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P22……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….27/7/10…..………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………………TTOP22P………Serial No ………………………………
Test Engineer ………RMC
Date …………………24/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP22P
Driver board ID	TTOP22P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP22P
Monitor board ID	MON42P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON42P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P23……………………Serial No ………………………………
Test Engineer ….Xen………..……
Date …………….10/8/10…………

Drive Card ID……T_TOP23P…………
Monitor Card ID...Mon43P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

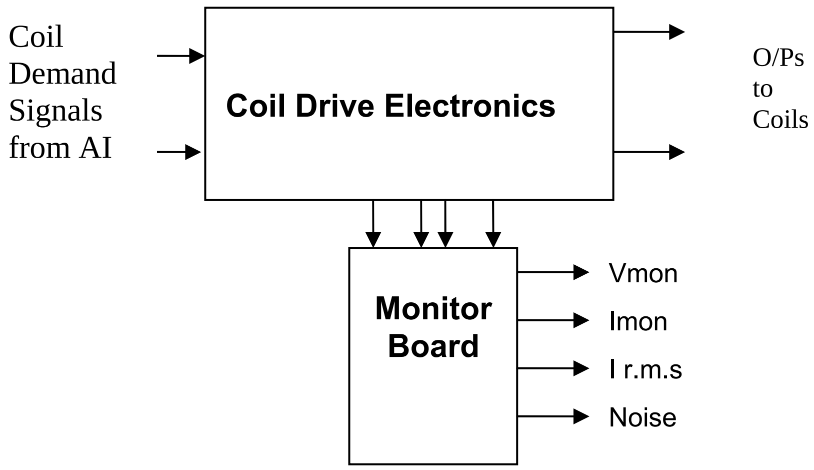


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P23……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….10/8/10…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P23……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date ……………2/11/09…………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit.................T_TOP_P23.......................Serial No ....
Test Engineer ....Xen................
Date ....2/11/09...........

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P23……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/11/09………..

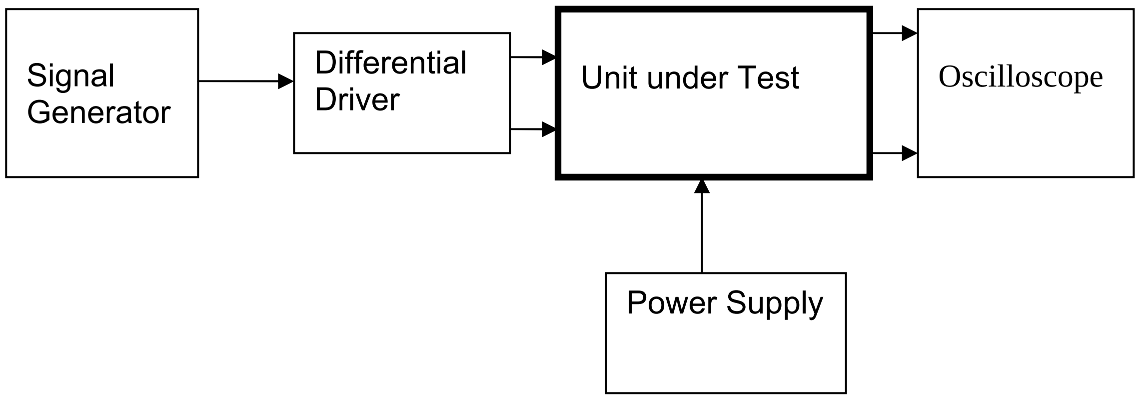
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit.................T_TOP_P23.......................Serial No ....
Test Engineer ....Xen................
Date ....2/11/09............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P23……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….2/11/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P23……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….2/11/09…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.756	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.753	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.755	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.754	√

Unit………………T_TOP_P23……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….2/11/09…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.27	2.9μV√Hz	√
2		0.84	2.9μV√Hz	√
3		1.22	2.9μV√Hz	√
4		1.36	2.9μV√Hz	√

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	3.4		
10Hz	-25.1		
100Hz	-42.0		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Test Engineer ….Xen……..………
Date …………….2/11/09…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

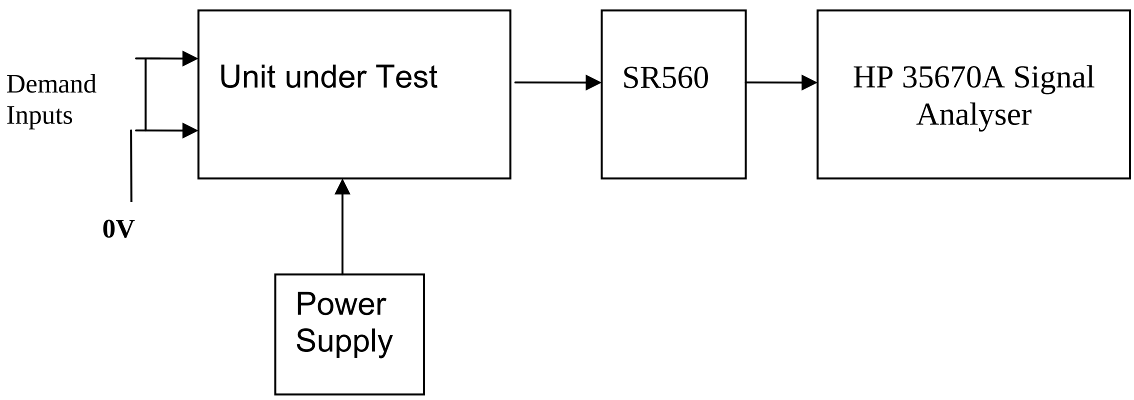
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.19	**CH1 IC1**	38.7	√
CH1 Negative		**CH1 IC5**	41.1	√
CH2 Positive	12.19	**CH2 IC1**	41.1	√
CH2 Negative		**CH2 IC5**	42.3	√
CH3 Positive	12.19	**CH3 IC1**	41.6	√
CH3 Negative		**CH3 IC5**	42.1	√
CH4 Positive	12.19	**CH4 IC1**	41.8	√
CH4 Negative		**CH4 IC5**	42.6	√

Unit……………………..T_TOP_P23………………Serial No ………………………………
Test Engineer ………RMC (1, 2 & 3) / Xen (4)
Date …………………8/12/09 / 22/7/10

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-98.8	-158.8
Ch2	-160dB	-101.2	-161.2
Ch3	-160dB	-98.7	-158.7
Ch4	-160dB	-102.5	-162.5

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P23……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date …………….22/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………………TTOP23P………Serial No ………………………………
Test Engineer ………RMC
Date …………………24/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP23P
Driver board ID	TTOP23P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP23P
Monitor board ID	MON43P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON43P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P24……………………Serial No ………………………………
Test Engineer ….Xen………..……
Date …………….9/8/10..…………

Drive Card ID……T_TOP24P…………
Monitor Card ID...Mon44P….…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

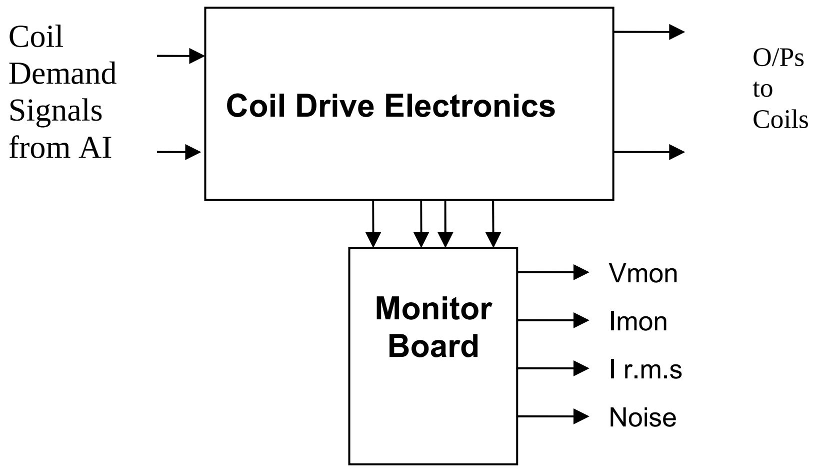


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P24……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….9/8/10..…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_P24……………………..Serial No ……………………………….
Test Engineer ….Xen……..………
Date …………….2/12/09…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P24……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….2/12/09………..

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit.................T_TOP_P24.......................Serial No ....
Test Engineer ....Xen................
Date ....2/12/09...........

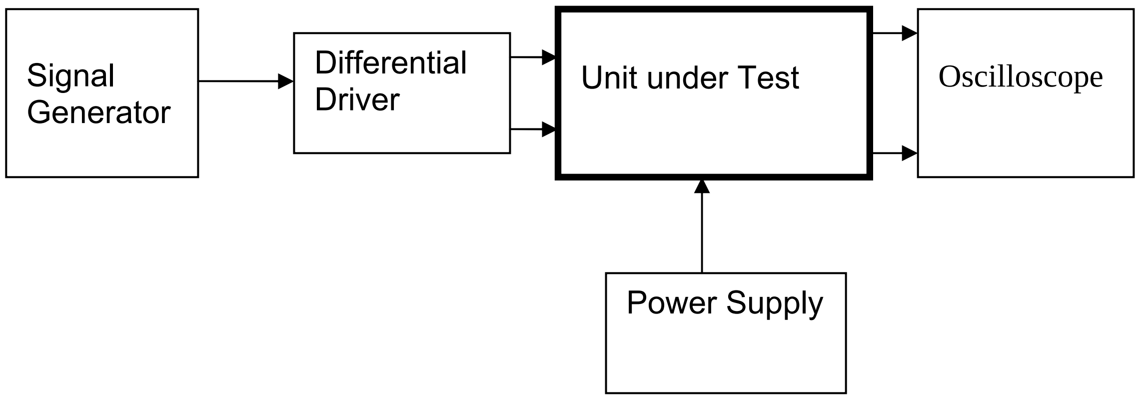
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)
Pd In from Sat pin 9, 10 = +16.5v or DC in A1
Pd In from Sat pin 11, 12 = -16.5 or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v or DC in A2

Coil Drive Outputs
Ch1+ = Coil out to Sat pin 1
Ch2+ = Coil out to Sat pin 3
Ch3+ = Coil out to Sat pin 5
Ch4+ = Coil out to Sat pin 7

Ch1- = Coil out to Sat pin 9
Ch2- = Coil out to Sat pin 11
Ch3- = Coil out to Sat pin 13
Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P24........................Serial No ....
Test Engineer ....Xen..................
Date ....2/12/09............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P24……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….2/12/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P24……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….2/12/09………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.751	√
	Pin 1	RMS Current	0.75v dc	0.756	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.760	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.754	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit……………….T_TOP_P24……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….2/12/09…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in µV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9µV√Hz out.

Ch.	**Output (µV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.01	2.9µV√Hz	√
2		1.54	2.9µV√Hz	√
3		0.90	2.9µV√Hz	√
4		1.27	2.9µV√Hz	√

Unit.................T_TOP_P24.......................Serial No ....
Test Engineer ....Xen................
Date ....2/12/09...........

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	3.3		
10Hz	-25.2		
100Hz	-42.0		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.9		

Unit.................T_TOP_P24.......................Serial No ....
Test Engineer ....Xen................
Date ....2/12/09...........

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

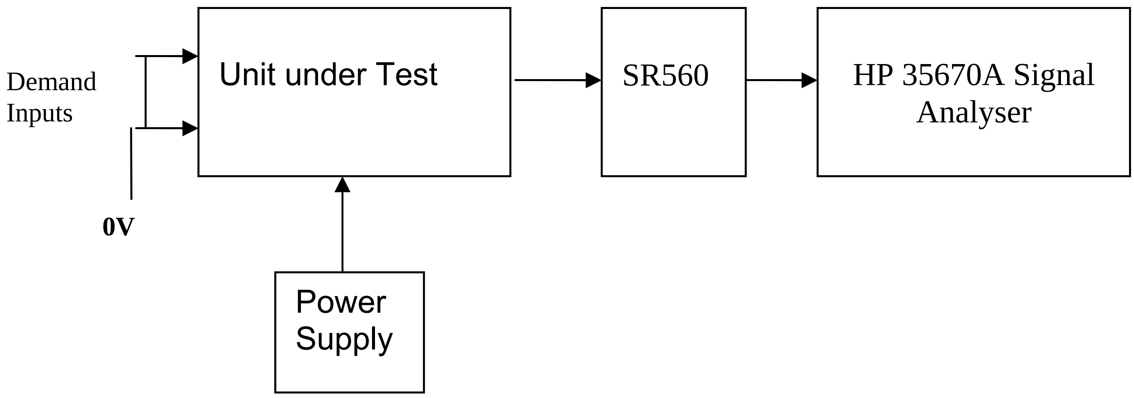
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	**CH1 IC1**	41.1	√
CH1 Negative		**CH1 IC5**	41.6	√
CH2 Positive	12.19	**CH2 IC1**	43.3	√
CH2 Negative		**CH2 IC5**	43.3	√
CH3 Positive	12.19	**CH3 IC1**	43.1	√
CH3 Negative		**CH3 IC5**	43.1	√
CH4 Positive	12.19	**CH4 IC1**	42.1	√
CH4 Negative		**CH4 IC5**	41.6	√

Unit…………………TTOP 24 P…………Serial No ………………………………
Test Engineer ………RMC
Date …………………20/1/10

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.4 dB	-160.4 dB
Ch2	-160dB	-101.7 dB	-161.7dB
Ch3	-160dB	-101.6 dB	-161.6 dB
Ch4	-160dB	-100.26 dB	-160.26 dB

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit.................T_TOP_P24.......................Serial No ....
Test Engineer ....Xen................
Date ....20/7/10............

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.27	83.2mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit.................TTOP24P.......................Serial No ....
Test Engineer ....RMC
Date 24/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP24P
Driver board ID	TTOP24P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP24P
Monitor board ID	MON44P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON44P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

Unit………T Top 24 P……………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………20/1/10

PROBLEM REPORT

Problems
During noise tests, channel 4 was found to be excessively noisy.

Cause
IC4 and IC8 on channel 4

Solution
The noisy ICs were replaced, then the noise tests were performed.

Confirmation
Noise dropped to -160dB

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P25……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….11/11/09……

Drive Card ID……T_TOP25P………
Monitor Card ID...Mon46P…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

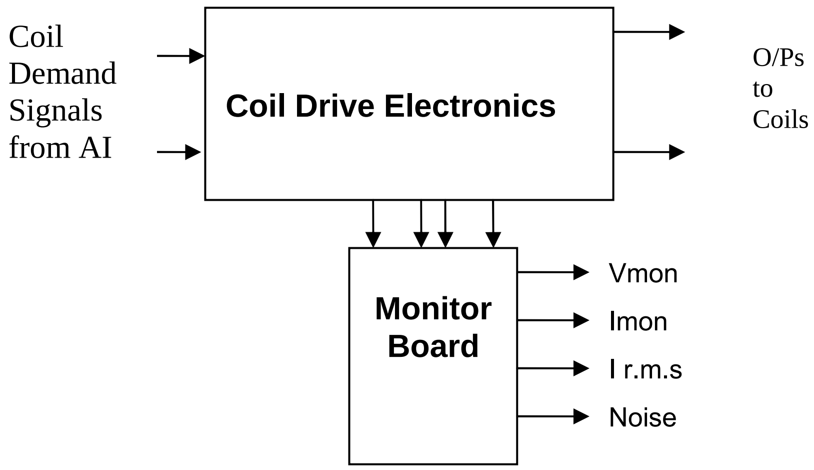


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit..................T_TOP_P25........................Serial No ....
Test Engineer ....Xen............
Date ....11/11/09......

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit…………….T_TOP_P25……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….11/11/09……

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………T_TOP_P25……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….11/11/09……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P25……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….11/11/09……

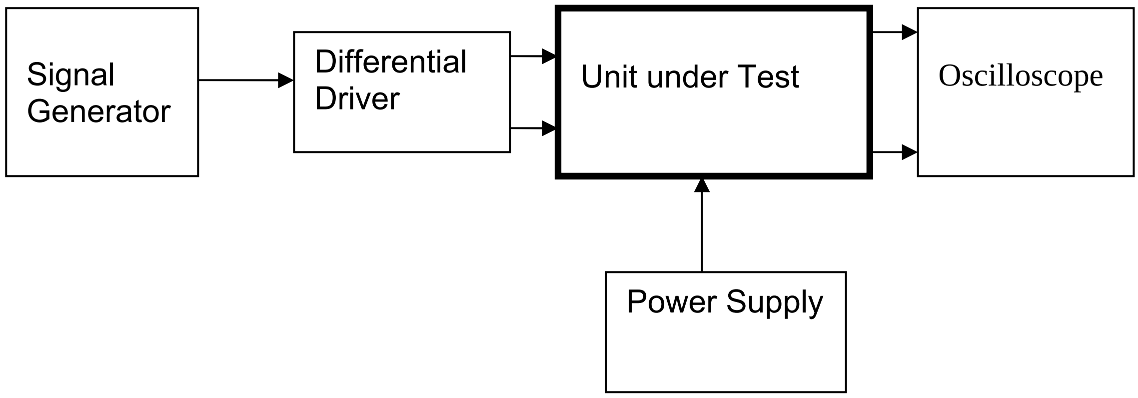
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P25……………………Serial No ………………………………
Test Engineer ….Xen…………
Date ……………11/11/09……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P25……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….11/11/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit..................T_TOP_P25........................Serial No ....
Test Engineer ....Xen............
Date ....11/11/09......

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.750	√
	Pin 1	RMS Current	0.75v dc	0.754	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.755	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.750	√
	Pin 7	RMS Current	0.75v dc	0.753	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.748	√
	Pin 10	RMS Current	0.75v dc	0.751	√

Unit……………..T_TOP_P25……………………Serial No ……………………………..
Test Engineer ….Xen………..
Date …………….11/11/09……

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.6	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.6	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.6	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.6	1.6v to 1.7v	√

Noise monitor tests

Connect the 39 ohm loads, the blanking plug in place on the drive input, and the relay test box.
Switch in all filters.
Connect power, and power up the unit. Measure the noise output on the noise monitor plug in μV/root Hz, on the HP Dynamic signal Analyser, the preamplifier with a gain of 10, and Stuart Aston's noise measurement set up.
Check that it is less than 3 μV/root Hz with respect to ground, which may be found on sockets number 5, 6, 7, 8 or 9.

	Noise Monitor socket pin number	**Noise**	**< 3μV/rt Hz?**
Channel 1	1	2.34	OK
Channel 2	2	1.87	OK
Channel 3	3	2.29	OK
Channel 4	4	1.4	OK

Unit………………T_TOP_P25……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….11/11/09……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.

Ensure that links W4 and W5 are present.

Using the Dynamic Signal Analyser

With the filter switched in, measure the frequency response of each channel in turn between 0.1 Hz and 1 kHz. If a fast turn around is required, limit the measurement to the frequency range to between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them.

Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
0.1 Hz	7.5		
1Hz	1.1		
10Hz	-30.0		
100Hz	-42.8		
1KHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
0.1 Hz	7.8		
1Hz	1.1		
10Hz	-30.1		
100Hz	-42.8		
1KHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
0.1 Hz	7.6		
1Hz	1.0		
10Hz	-30.4		
100Hz	-42.8		
1KHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
0.1 Hz	7.6		
1Hz	1.1		
10Hz	-30.1		
100Hz	-42.8		
1KHz	-43.3		

Unit………………T_TOP_P25……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….11/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1KHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

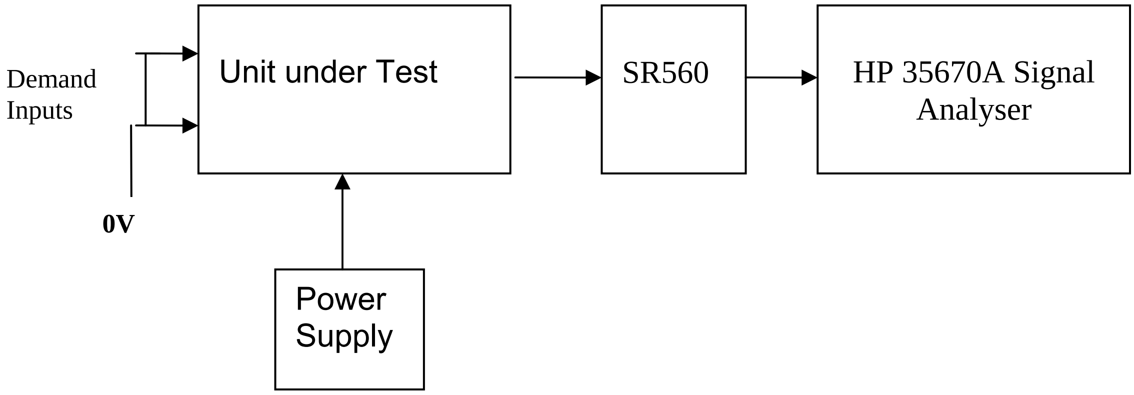
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.23	**CH1 IC1**	40.6	√
CH1 Negative		**CH1 IC5**	42.8	√
CH2 Positive	12.23	**CH2 IC1**	43.1	√
CH2 Negative		**CH2 IC5**	43.6	√
CH3 Positive	12.23	**CH3 IC1**	41.6	√
CH3 Negative		**CH3 IC5**	44.0	√
CH4 Positive	12.23	**CH4 IC1**	44.3	√
CH4 Negative		**CH4 IC5**	46.0	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………1/12/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.2	-160.2
Ch2	-160dB	-100.3	-160.3
Ch3	-160dB	-100.7	-160.7
Ch4	-160dB	-101.9	-161.9

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit.................T_TOP_P25.......................Serial No ....
Test Engineer ....Xen...........
Date ....11/11/09......

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.36	85.5mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.35	85.2mA	120mA	84.8mA	√
4	39.4	3.35	85.0mA	120mA	84.8mA	√

Unit……… TTOP25P …………………Serial No ………………………………
Test Engineer ………RMC
Date …………………

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP25P
Driver board ID	TTOP25P
Driver board Drawing No/Issue No	D0902747
Driver board Serial Number	TTOP25P
Monitor board ID	MON46P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON46P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,

    Check all external screws for tightness.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P26……………………Serial No ………………………………
Test Engineer ….Xen………….……
Date …………….16/11/09…………

Drive Card ID……T_TOP26P…………
Monitor Card ID...Mon47P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

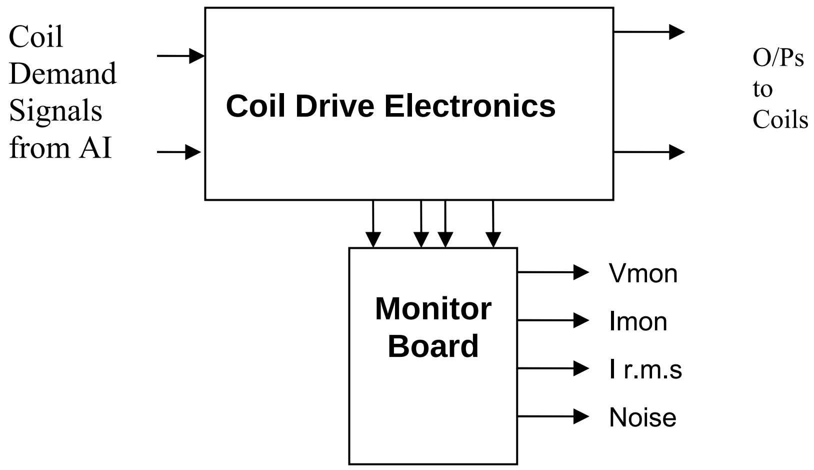


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P26……………………Serial No ………………………………
Test Engineer.….Xen………………
Date ……………16/11/09…….……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P26…………………..Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………16/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………T_TOP_P26……………………Serial No ………………………………
Test Engineer ….Xen…………..…..
Date …………….16/11/09………….

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	**SIGNAL**	**DESCRIPTION**	**Pd in from Sat**	**OK?**
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	**SIGNAL**	**Monitors:**	**In from Sat**	**OK?**
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	**SIGNAL**	**DESCRIPTION**	**DC in Connector**	**OK?**
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P26……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….16/11/09……..……

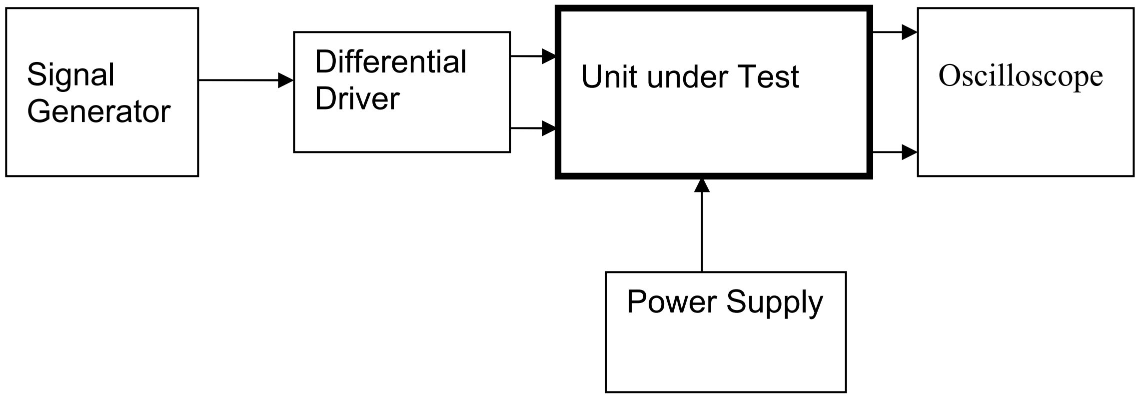
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	7MΩ	
IC12 Channel 1	7MΩ	
IC11 Channel 2	7MΩ	
IC12 Channel 2	7MΩ	
IC11 Channel 3	7MΩ	
IC12 Channel 3	7MΩ	
IC11 Channel 4	7MΩ	
IC12 Channel 4	7MΩ	

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P26........................Serial No ....
Test Engineer ....Xen..................
Date ....16/11/09.............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	**- 16.5 supply current (mA)**
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	**Plus**	**Minus**
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P26……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….16/11/09………….

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit.................T_TOP_P26.......................Serial No ....
Test Engineer ....Xen..................
Date ....16/11/09..........

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.751	√
	Pin 1	RMS Current	0.75v dc	0.754	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.751	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.749	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit………………T_TOP_P26……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….16/11/09……

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise monitor tests

Connect the 39 ohm loads, the blanking plug in place on the drive input, and the relay test box.
Switch in all filters.
Connect power, and power up the unit. Measure the noise output on the noise monitor plug in μV/root Hz, on the HP Dynamic signal Analyser, the preamplifier with a gain of 10, and Stuart Aston's noise measurement set up. Check that it is less than 3 μV/root Hz with respect to ground, which may be found on sockets number 5, 6, 7, 8 or 9.

	Noise Monitor socket pin number	**Noise**	**< 3μV/rt Hz?**
Channel 1	1	1.56	OK
Channel 2	2	1.67	OK
Channel 3	3	1.25	OK
Channel 4	4	1.45	OK

Unit……………..T_TOP_P26……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….16/11/09……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.3		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P26……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….16/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

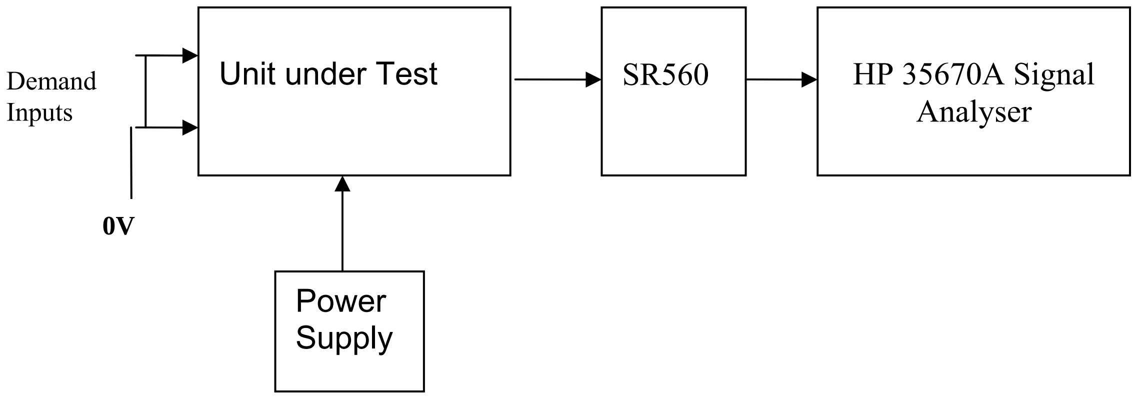
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.21	CH1 IC1	41.4	√
CH1 Negative		CH1 IC5	43.1	√
CH2 Positive	12.21	CH2 IC1	42.6	√
CH2 Negative		CH2 IC5	42.6	√
CH3 Positive	12.21	CH3 IC1	43.1	√
CH3 Negative		CH3 IC5	42.8	√
CH4 Positive	12.21	CH4 IC1	42.1	√
CH4 Negative		CH4 IC5	43.8	√

Unit.......................................Serial No ....
Test Engineer ....RMC
Date 3/12/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.35	-160.35
Ch2	-160dB	-101.0	-161.0
Ch3	-160dB	-103.0	-163.0
Ch4	-160dB	-96.8	-156.8

IC8 ch 4 and IC4 ch 4 changed.

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit.................T_TOP_P26.......................Serial No ....
Test Engineer ....Xen...........
Date ....16/11/09......

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	3.37	85.8mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.36	85.5mA	120mA	84.8mA	√
4	39.4	3.36	85.3mA	120mA	84.8mA	√

Unit……………………………………Serial No ………………………………
Test Engineer ………
Date …………………

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP26P
Driver board ID	TTOP26P
Driver board Drawing No/Issue No	D0902747
Driver board Serial Number	TTOP26P
Monitor board ID	MON47P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON47P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,

Check all external screws for tightness.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P27……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….28/7/10 …………

Drive Card ID……T_TOP27P…………
Monitor Card ID...Mon48P….…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

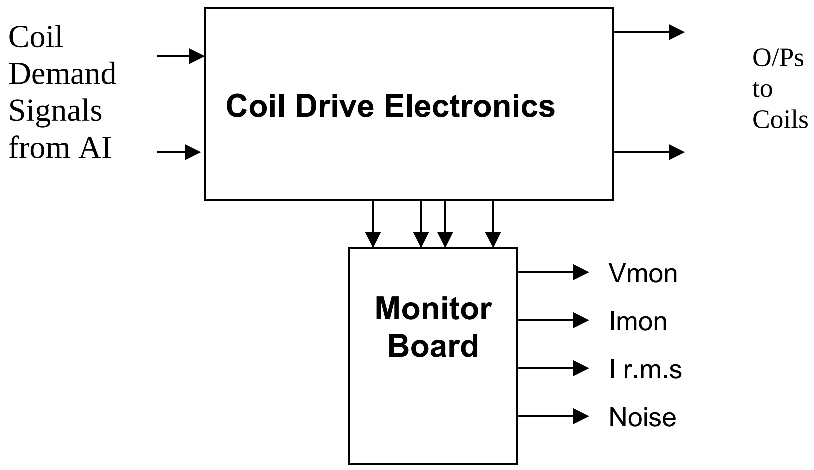


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….T_TOP_P27……………………Serial No ………………………………
Test Engineer…..Xen……………..…
Date …………….28/7/10 ……..……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P27……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….12/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 3 & 4.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P27……………………Serial No ………………………………
Test Engineer ….Xen……………..…..
Date …………….12/11/09….….……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P26……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….12/11/09……..……

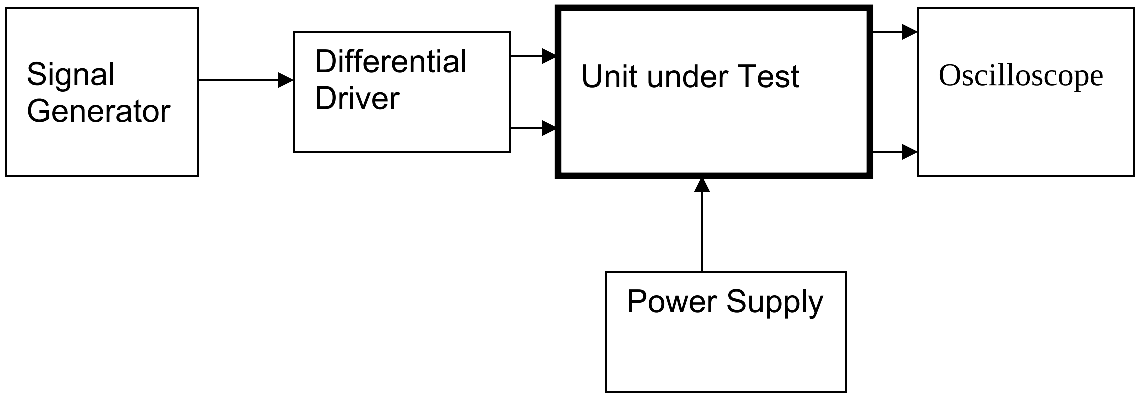
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P27……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….12/11/09……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P27……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….12/11/09……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P27……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….12/11/09……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.762	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.754	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit……………..T_TOP_P27……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….12/11/09……

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.80	2.9μV√Hz	√
2		1.44	2.9μV√Hz	√
3		1.25	2.9μV√Hz	√
4		1.09	2.9μV√Hz	√

Unit……………..T_TOP_P27……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….12/11/09……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Using the Dynamic Signal Analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1KHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1KHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1KHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1KHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P27……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….12/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.21	**CH1 IC1**	38.4	√
CH1 Negative		**CH1 IC5**	39.4	√
CH2 Positive	12.21	**CH2 IC1**	41.1	√
CH2 Negative		**CH2 IC5**	41.8	√
CH3 Positive	12.21	**CH3 IC1**	42.6	√
CH3 Negative		**CH3 IC5**	40.4	√
CH4 Positive	12.21	**CH4 IC1**	38.9	√
CH4 Negative		**CH4 IC5**	42.6	√

Unit…………………..T_TOP_P27……………..Serial No ……………………………..
Test Engineer ………RMC (1&2) / Xen (3&4)
Date …………………1/12/09/28/7/10

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.

Replace the lid of the box, and replace screws.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode

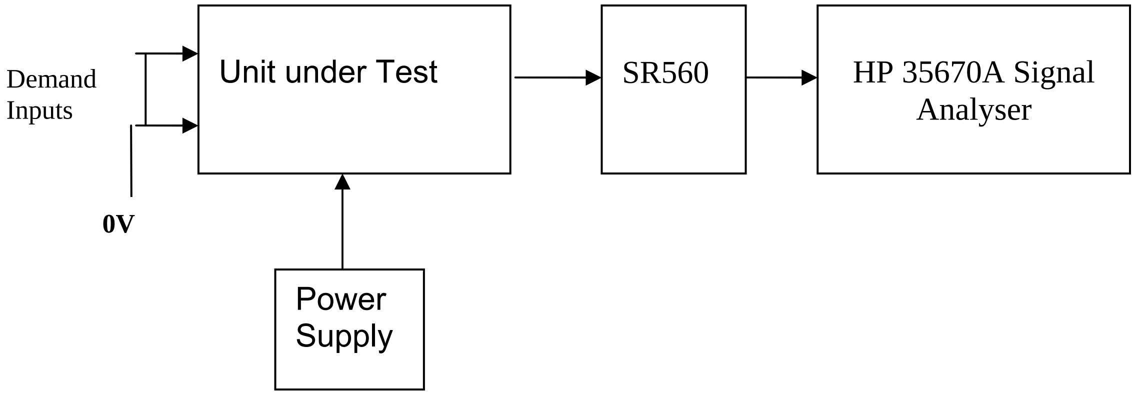
Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.

Switch the filters in.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.9	-161.9
Ch2	-160dB	-101.0	-161.0
Ch3	-160dB	-101.4	-161.4
Ch4	-160dB	-101.0	-161.0

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P27……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….26/7/10..……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s) +/- 2.5mA**	**Pass?**
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP27P…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………30/9/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP27P
Driver board ID	TTOP27P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP27P
Monitor board ID	MON48P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON48P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P28……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….13/8/10..……

Drive Card ID……T_TOP28P…………
Monitor Card ID...Mon49P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

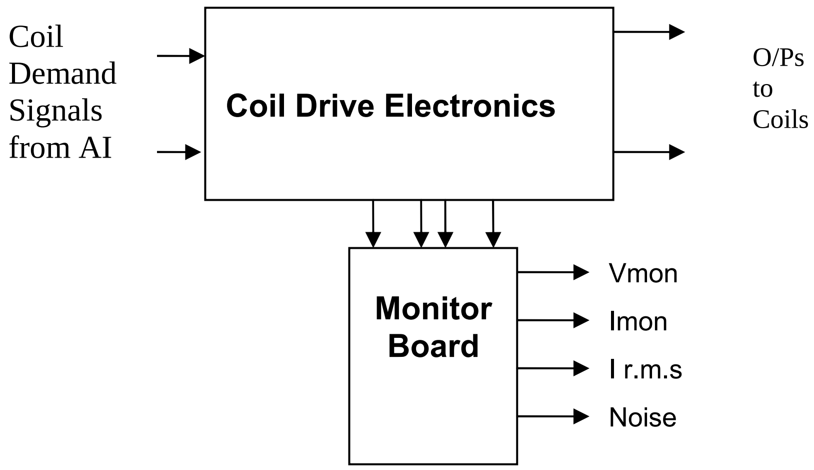


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen……………….
Date ……………13/8/10..……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P28……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….13/11/09…..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Four 0.39uF filter capacitors have been added to the driver board (C200).
Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P28……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….13/11/09……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	**SIGNAL**	**DESCRIPTION**	**Pd in from Sat**	**OK?**
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	**SIGNAL**	**Monitors:**	**In from Sat**	**OK?**
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	**SIGNAL**	**DESCRIPTION**	**DC in Connector**	**OK?**
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P28……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….13/11/09……..……

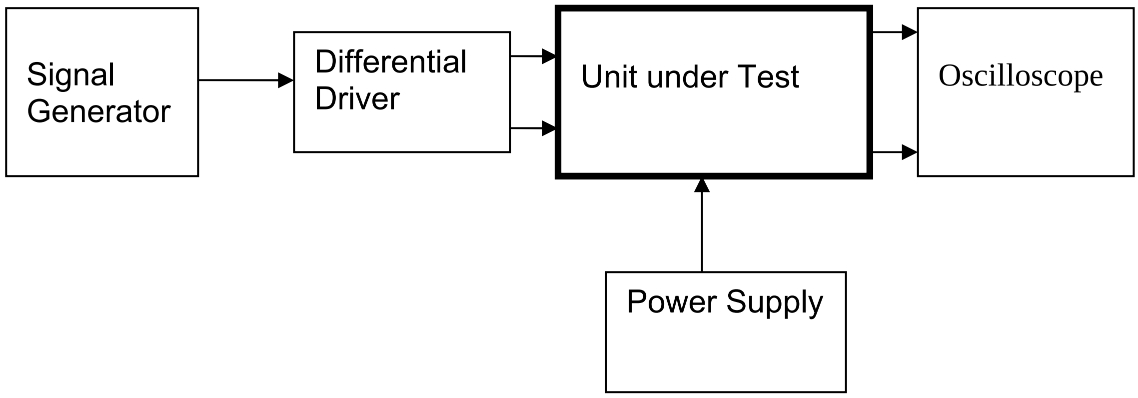
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P28........................Serial No ....
Test Engineer ....Xen...................
Date ....13/11/09.............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P28…………………..Serial No ……………………………..
Test Engineer ….Xen………………
Date …………….13/11/09………..

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P28……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….16/11/09……..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.753	√
	Pin 1	RMS Current	0.75v dc	0.757	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.754	√
	Pin 4	RMS Current	0.75v dc	0.757	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.754	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.752	√

Unit..................T_TOP_P28........................Serial No ....
Test Engineer ....Xen............
Date ....16/11/09......

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.40	2.9μV√Hz	√
2		1.61	2.9μV√Hz	√
3		1.17	2.9μV√Hz	√
4		1.0	2.9μV√Hz	√

Unit……………..T_TOP_P28……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….16/11/09……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit…………………T_TOP_P28…………………….Serial No ………………………………
Test Engineer ….Xen………..
Date …………….16/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

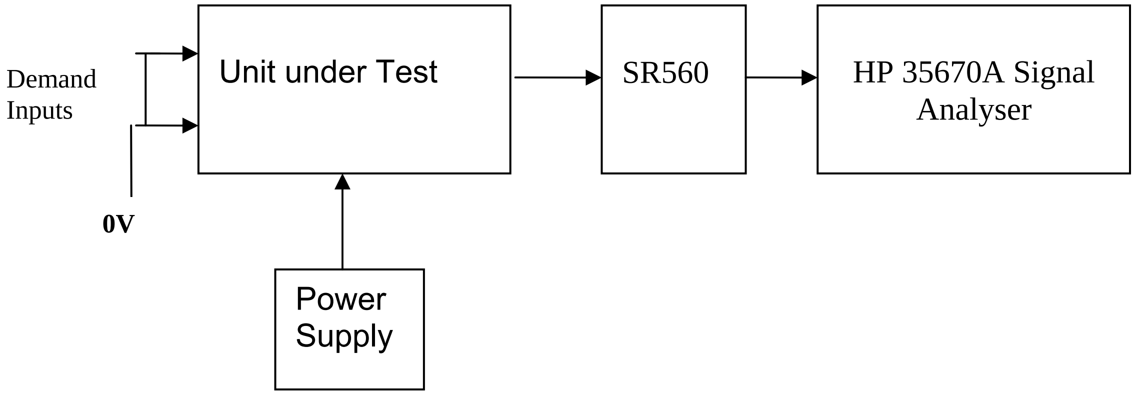
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.21	**CH1 IC1**	40.1	√
CH1 Negative		**CH1 IC5**	44.0	√
CH2 Positive	12.21	**CH2 IC1**	42.8	√
CH2 Negative		**CH2 IC5**	43.6	√
CH3 Positive	12.21	**CH3 IC1**	42.8	√
CH3 Negative		**CH3 IC5**	44.3	√
CH4 Positive	12.21	**CH4 IC1**	42.1	√
CH4 Negative		**CH4 IC5**	42.6	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………24/11/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.5	-160.5
Ch2	-160dB	-101.4	-161.4
Ch3	-160dB	-100.3	-160.3
Ch4	-160dB	-100.8	-160.8

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit………………T_TOP_P28……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….20/7/10..……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s) +/- 2.5mA**	**Pass?**
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit………TTOP28P……………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………30/9/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP28P
Driver board ID	TTOP28P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP28P
Monitor board ID	MON49P
Monitor board Drawing No/Issue No	D0070480_4_K
Monitor board Serial Number	MON49P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P29……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….13/11/09…………

Drive Card ID……T_TOP29P…………
Monitor Card ID...Mon50P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

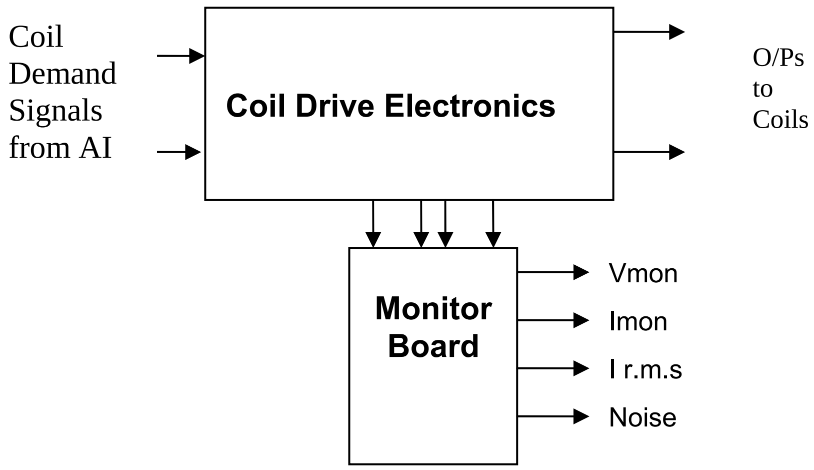

FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P29……………………Serial No ………………………………
Test Engineer…...Xen………….……
Date ……………13/11/09……….…

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
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Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P29…………………..Serial No ………………………………
Test Engineer ….Xen……………..
Date ……………13/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………T_TOP_P29……………………Serial No ………………………………
Test Engineer ….Xen……………..…..
Date …………….13/11/09………….

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P29……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….13/11/09……..……

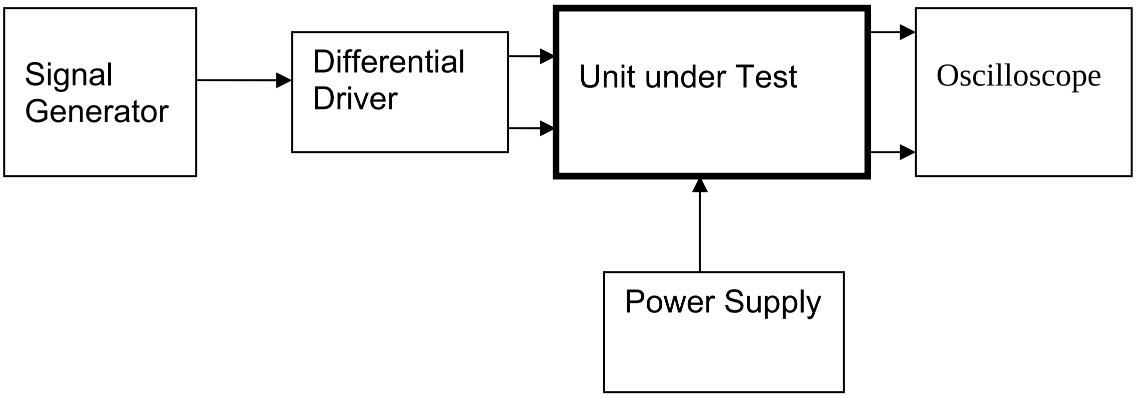
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P29........................Serial No ....
Test Engineer ....Xen...................
Date ....13/11/09.............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit..................T_TOP_P29........................Serial No ....
Test Engineer ....Xen...................
Date ....13/11/09.............

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P29……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….13/11/09……..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.751	√
	Pin 1	RMS Current	0.75v dc	0.752	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.756	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit……………….T_TOP_P29……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….13/11/09……

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise monitor tests

Connect the 39 ohm loads, the blanking plug in place on the drive input, and the relay test box.
Switch in all filters.
Connect power, and power up the unit. Measure the noise output on the noise monitor plug in μV/root Hz, on the HP Dynamic signal Analyser, the preamplifier with a gain of 10, and Stuart Aston's noise measurement set up. Check that it is less than 3 μV/root Hz with respect to ground, which may be found on sockets number 5, 6, 7, 8 or 9.

	Noise Monitor socket pin number	**Noise**	**< 3μV/rt Hz?**
Channel 1	1	2.27	OK
Channel 2	2	2.15	OK
Channel 3	3	1.79	OK
Channel 4	4	1.55	OK

Unit..Serial No ....
Test Engineer ....
Date ....

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Using the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………T_TOP_P29……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….13/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

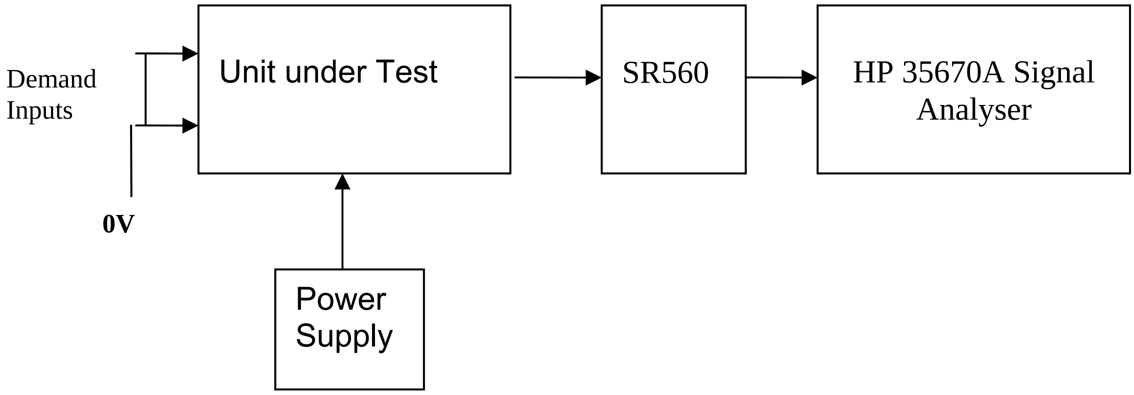
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive		CH1 IC1	41.6	√
CH1 Negative		CH1 IC5	42.8	√
CH2 Positive		CH2 IC1	43.1	√
CH2 Negative		CH2 IC5	44.0	√
CH3 Positive		CH3 IC1	44.0	√
CH3 Negative		CH3 IC5	44.5	√
CH4 Positive		CH4 IC1	42.8	√
CH4 Negative		CH4 IC5	44.5	√

Unit……………………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………30/11/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.0	-160.0
Ch2	-160dB	-97.6	-157.6
Ch3	-160dB	-101.0	-161.0
Ch4	-160dB	-100.3	-160.0

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nV/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P29……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….13/11/09……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	3.36	85.5mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.35	85.2mA	120mA	84.8mA	√
4	39.4	3.34	84.8mA	120mA	84.8mA	√

Unit……………………………………Serial No ………………………………
Test Engineer ………
Date …………………

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP29P
Driver board ID	TTOP29P
Driver board Drawing No/Issue No	D0902747 V6
Driver board Serial Number	TTOP29P
Monitor board ID	MON50P
Monitor board Drawing No/Issue No	DO7O480_04_K
Monitor board Serial Number	MON50P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….10/8/10…………

Drive Card ID……T_TOP30P…………
Monitor Card ID...Mon51P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

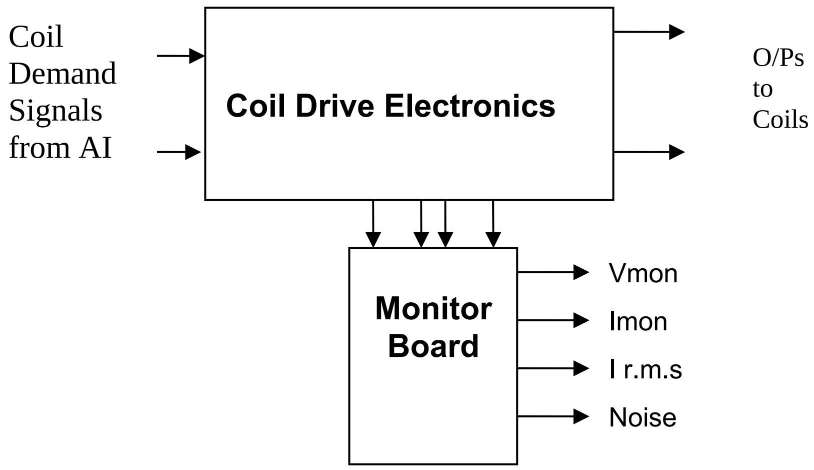


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen…….……….
Date …………….10/8/10…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date …………….3/12/09…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Four 0.39uF filter capacitors have been added to the driver board (C200).
Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….3/12/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	**SIGNAL**	**DESCRIPTION**	**Pd in from Sat**	**OK?**
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	**SIGNAL**	**Monitors:**	**In from Sat**	**OK?**
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	**SIGNAL**	**DESCRIPTION**	**DC in Connector**	**OK?**
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….3/12/09…………

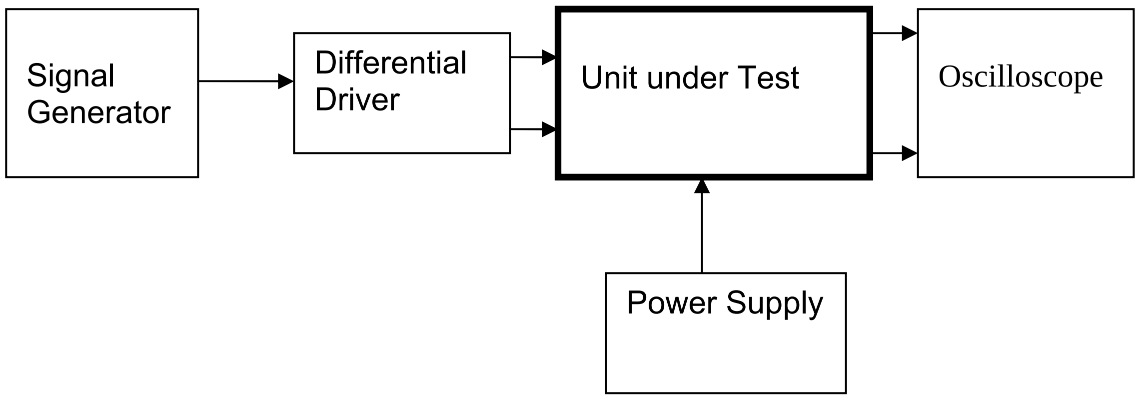
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….3/12/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	**- 16.5 supply current (mA)**
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	**Plus**	**Minus**
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….3/12/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P30…………………….Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….3/12/09…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.759	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.758	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.759	√

Unit………………T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….3/12/09…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.50	2.9μV√Hz	√
2		1.97	2.9μV√Hz	√
3		1.45	2.9μV√Hz	√
4		1.33	2.9μV√Hz	√

Unit………………T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….3/12/09…………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….3/12/09………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.19	**CH1 IC1**	40.1	√
CH1 Negative		**CH1 IC5**	42.1	√
CH2 Positive	12.19	**CH2 IC1**	42.6	√
CH2 Negative		**CH2 IC5**	42.3	√
CH3 Positive	12.19	**CH3 IC1**	41.6	√
CH3 Negative		**CH3 IC5**	41.4	√
CH4 Positive	12.19	**CH4 IC1**	41.6	√
CH4 Negative		**CH4 IC5**	41.8	√

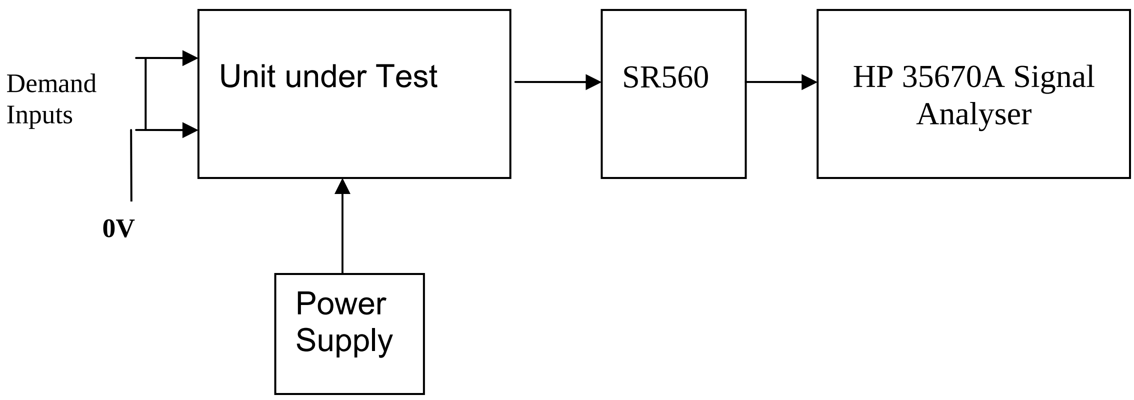
Unit..Serial No ....
Test Engineer ....RMC
Date 3/12/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.0	
Ch2	-160dB	-100.0	
Ch3	-160dB	-99.9	
Ch4	-160dB	-103.0	

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit………………T_TOP_P30……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….22/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.25	82.7mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………TTOP30P………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………23/8/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP30P
Driver board ID	TTOP30P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP30P
Monitor board ID	MON51
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON51

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit..................T_TOP_P31........................Serial No ....
Test Engineer ....Xen.................
Date ....28/7/10............

Drive Card ID......T_TOP31P.............
Monitor Card ID...Mon52P.................

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

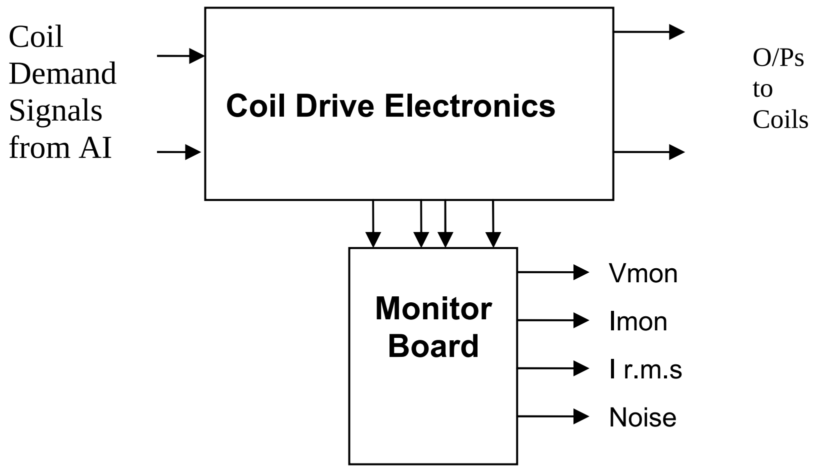


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit..................T_TOP_P31........................Serial No ....
Test Engineer ....Xen.................
Date ....28/7/10............

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………...T_TOP_P31……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….3/12/09…………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P31……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….3/12/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P31……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….3/12/09…………

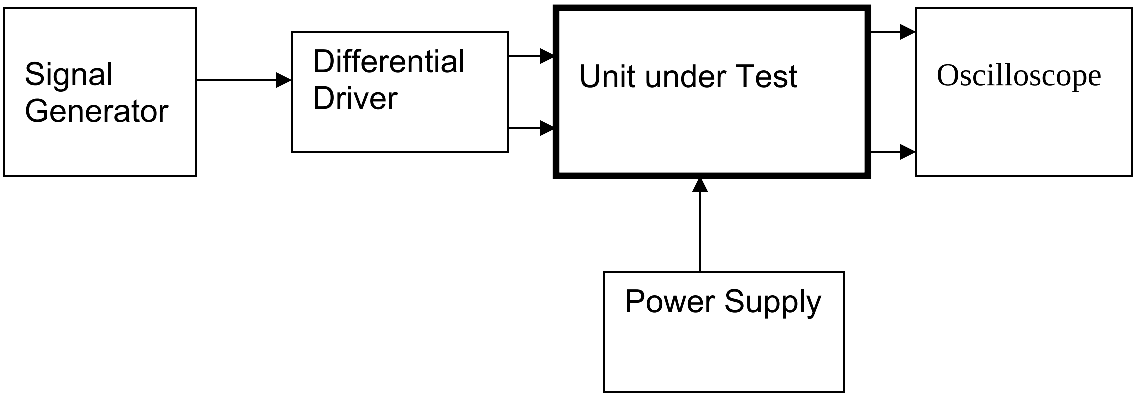
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P31……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….3/12/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P31……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date …………….3/12/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P31……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….3/12/09………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.752	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.756	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit.................T_TOP_P31.......................Serial No ....
Test Engineer ....Xen................
Date ....3/12/09............

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.
Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.41	2.9μV√Hz	√
2		1.10	2.9μV√Hz	√
3		0.84	2.9μV√Hz	√
4		0.99	2.9μV√Hz	√

Unit……………..T_TOP_P31……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….3/12/09………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..T_TOP_P31……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….4/12/09…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

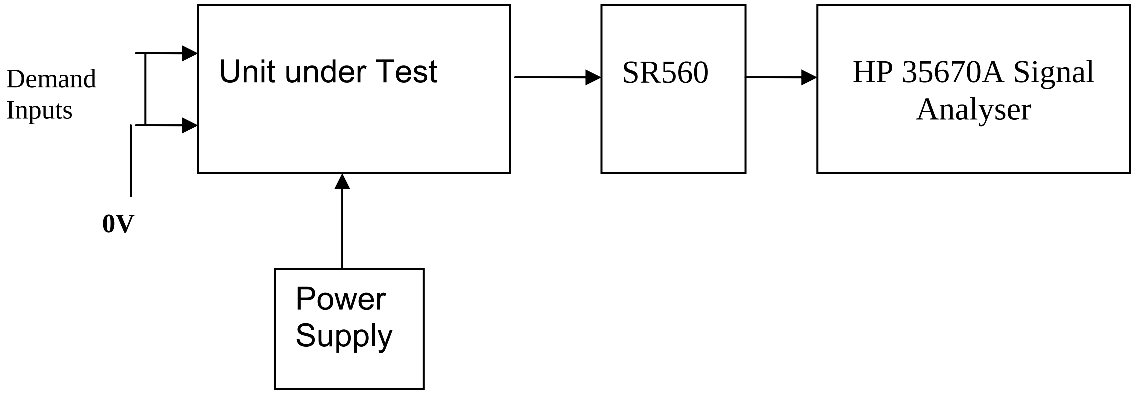
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	**CH1 IC1**	40.4	√
CH1 Negative		**CH1 IC5**	41.4	√
CH2 Positive	12.20	**CH2 IC1**	41.4	√
CH2 Negative		**CH2 IC5**	41.4	√
CH3 Positive	12.19	**CH3 IC1**	41.6	√
CH3 Negative		**CH3 IC5**	40.9	√
CH4 Positive	12.20	**CH4 IC1**	41.1	√
CH4 Negative		**CH4 IC5**	40.6	√

Unit……………..T_TOP_P31……………………Serial No ………………………………
Test Engineer …RMC (1, 2 & 3) / Xen (4)…
Date ……………28/7/10………………..……

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.3	-160.3
Ch2	-160dB	-99.9	-159.9
Ch3	-160dB	-98.4	-158.4
Ch4	-160dB	-101.6	-161.6

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit..................T_TOP_P31........................Serial No ....
Test Engineer ....Xen................
Date ....27/7/10............

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………… TTOP31P …Serial No ………………………………
Test Engineer ………RMC
Date …………………23/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP31P
Driver board ID	TTOP31P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP31P
Monitor board ID	MON52P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON52P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P32……………………Serial No ………………………………
Test Engineer ….Xen…...…..………
Date …………….9/8/10…..…………

Drive Card ID……T_TOP32P…………
Monitor Card ID...Mon53P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

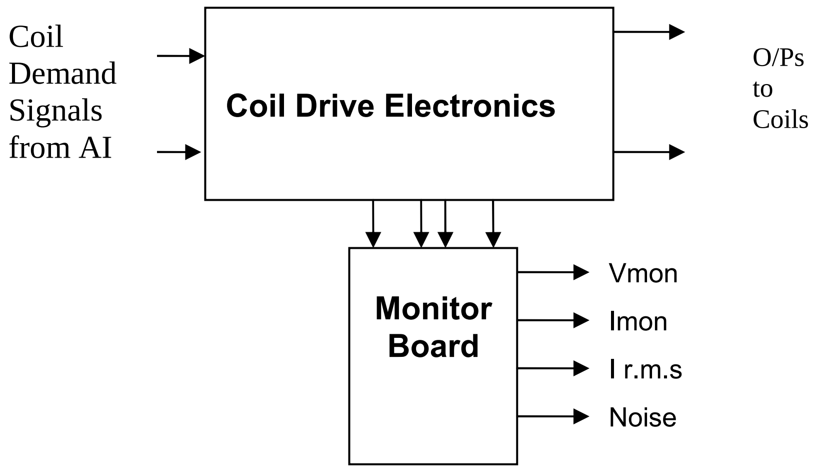


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P32……………………Serial No ………………………………
Test Engineer ….Xen…..…..………
Date …………….9/8/10…..………..

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P32……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date ……………4/12/09…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH3.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P32……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….4/12/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P32……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….4/12/09…………

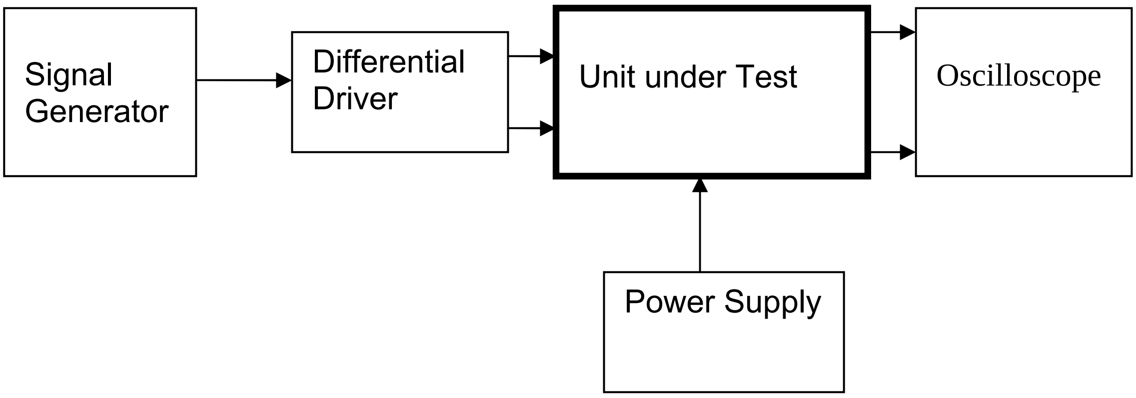
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P32……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….4/12/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P32……………………Serial No ………………………………
Test Engineer ….Xen………….…
Date ……………4/12/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit.................T_TOP_P32.......................Serial No ....
Test Engineer ....Xen................
Date ....4/12/09...........

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.757	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit……………..T_TOP_P32……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….4/12/09………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		0.73	2.9μV√Hz	√
2		1.65	2.9μV√Hz	√
3		1.02	2.9μV√Hz	√
4		1.36	2.9μV√Hz	√

Unit……………..T_TOP_P32……………………Serial No ………………………………
Test Engineer ….Xen……………
Date ……………4/12/09…………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit..................T_TOP_P32........................Serial No ....
Test Engineer ....Xen................
Date ....4/12/09............

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

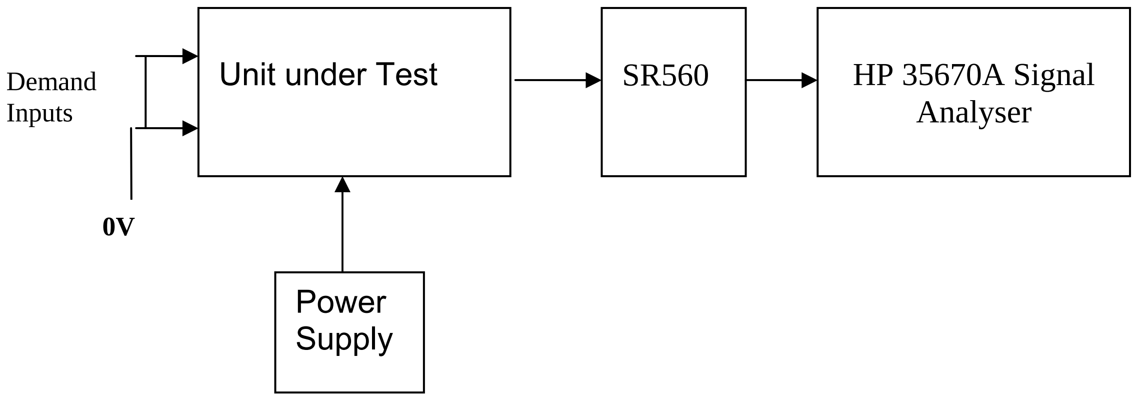
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	CH1 IC1	38.7	√
CH1 Negative		CH1 IC5	40.1	√
CH2 Positive	12.19	CH2 IC1	41.1	√
CH2 Negative		CH2 IC5	40.9	√
CH3 Positive	12.19	CH3 IC1	42.1	√
CH3 Negative		CH3 IC5	41.6	√
CH4 Positive	12.19	CH4 IC1	40.6	√
CH4 Negative		CH4 IC5	42.6	√

Unit......................T_TOP_P32....................Serial No ....
Test Engineer ....RMC (1, 2 & 4) / Xen (3)
Date ....8/12/09 / 28/7/10

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-160dB	-99.4	-159.4
Ch2	-160dB	-99.9	-159.9
Ch3	-160dB	-102.5	-162.5
Ch4	-160dB	-100	-160

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P32……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….27/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP31P……………Serial No ………………………………
Test Engineer ………RMC
Date …………………23/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP32P
Driver board ID	TTOP32P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP32P
Monitor board ID	MON53P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON53P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P33……………………Serial No ………………………………
Test Engineer ….Xen…...…..……..
Date …………….9/8/10…..…………

Drive Card ID……T_TOP33P…………
Monitor Card ID...Mon54P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

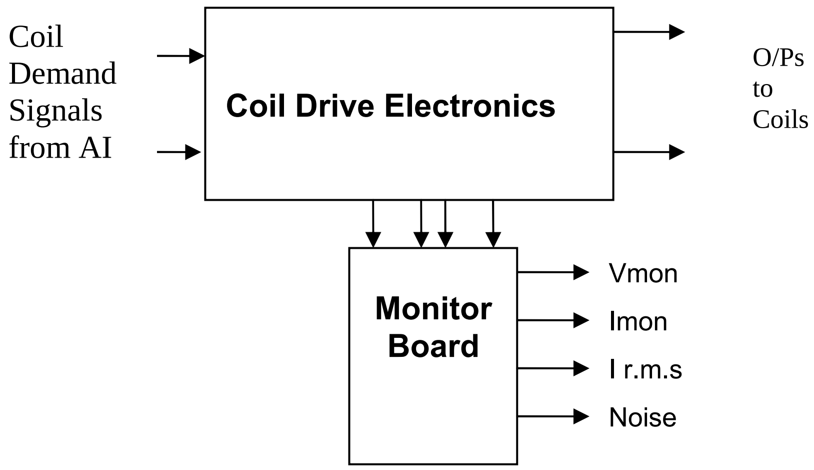


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P33……………………Serial No ………………………………
Test Engineer ….Xen…..…..………
Date …………….9/8/10…..…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P33……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date ……………4/12/09…………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH3.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit.................T_TOP_P33.......................Serial No ....
Test Engineer ....Xen................
Date ....4/12/09............

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………..T_TOP_P33……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….4/12/09…………

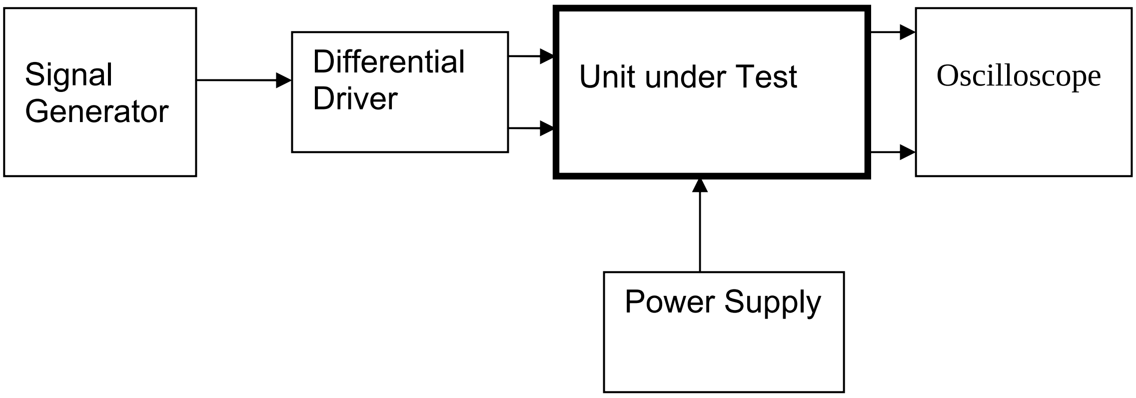
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P33……………………Serial No ………………………………
Test Engineer ….Xen………….…
Date ……………4/12/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit…………………T_TOP_P33…………………………Serial No ……………………………………
Test Engineer ….Xen……..………
Date ………………4/12/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P33……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….4/12/09…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.753	√
	Pin 1	RMS Current	0.75v dc	0.759	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.752	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.758	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.751	√

Unit……………..T_TOP_P33……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….4/12/09………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.29	2.9μV√Hz	√
2		0.82	2.9μV√Hz	√
3		1.53	2.9μV√Hz	√
4		1.74	2.9μV√Hz	√

Unit……………..T_TOP_P33……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….4/12/09………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.85		
Ch4	4.85		

Unit.................T_TOP_P33.......................Serial No ....
Test Engineer ....Xen................
Date ....4/12/09............

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

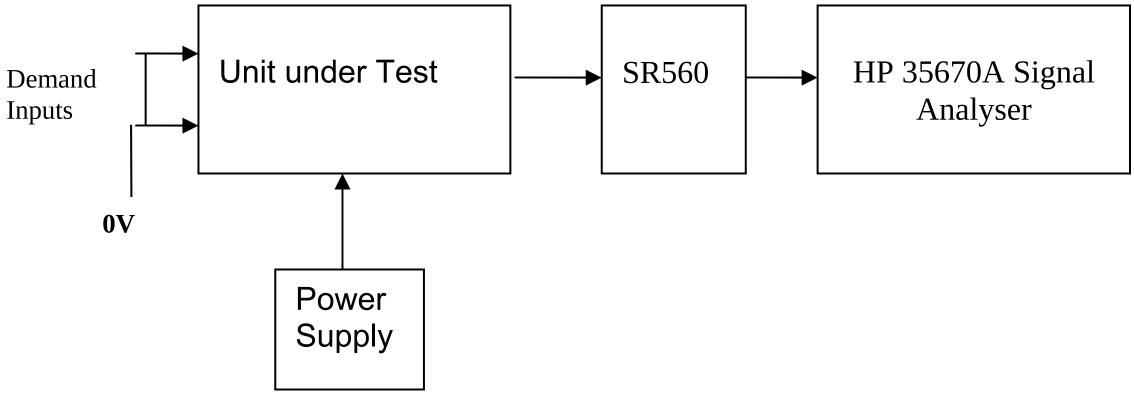
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	CH1 IC1	40.6	√
CH1 Negative		CH1 IC5	42.1	√
CH2 Positive	12.19	CH2 IC1	41.8	√
CH2 Negative		CH2 IC5	43.1	√
CH3 Positive	12.19	CH3 IC1	42.3	√
CH3 Negative		CH3 IC5	43.6	√
CH4 Positive	12.19	CH4 IC1	40.6	√
CH4 Negative		CH4 IC5	42.6	√

Unit......................T_TOP_P33.................Serial No ....
Test Engineer ....RMC (1, 2 & 4) / Xen (3)
Date ....8/12/09 / 28/7/10

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.4	-100.4
Ch2	-160dB	-99.7	-159.7
Ch3	-160dB	-101.0	-161.0
Ch4	-160dB	-100.4	-160.4

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit.................T_TOP_P33.......................Serial No ....
Test Engineer ....Xen................
Date ....27/7/10...........

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit………………… TTOP33P ……………Serial No ………………………………
Test Engineer ………RMC
Date …………………23/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP33P
Driver board ID	TTOP33P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP33P
Monitor board ID	MON54P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON54P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P34……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….9/8/10..…………

Drive Card ID……T_TOP34P…………
Monitor Card ID...Mon55P…..…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

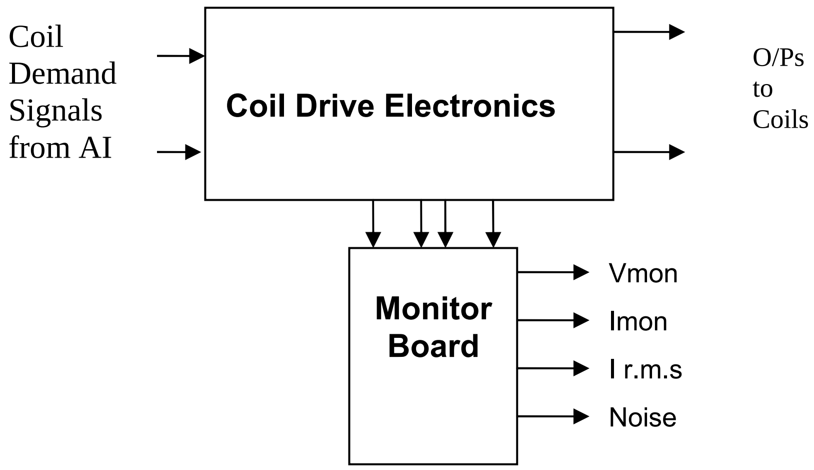


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P34……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….9/8/10..…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_P34……………………..Serial No ……………………………….
Test Engineer ….Xen…….………
Date …………….4/12/09…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P34……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….4/12/09…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………..T_TOP_P34……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….4/12/09…………

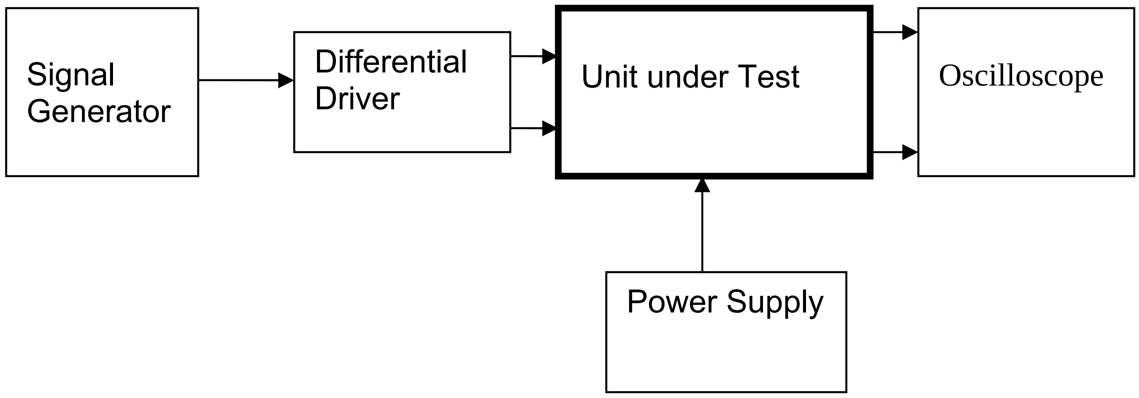
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P34……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….4/12/09…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P34……………………Serial No ……………………………..
Test Engineer ….Xen……..……..
Date ……………4/12/09…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P34……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date ……………4/12/09…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.753	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.758	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.754	√
	Pin 7	RMS Current	0.75v dc	0.758	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit………………T_TOP_P34……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date ……………4/12/09…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.14	2.9μV√Hz	√
2		1.01	2.9μV√Hz	√
3		0.99	2.9μV√Hz	√
4		1.38	2.9μV√Hz	√

Unit……………..T_TOP_P34……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….4/12/09………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………T_TOP_P34……………………Serial No ………………………………
Test Engineer ….Xen……………
Date ……………4/12/09…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

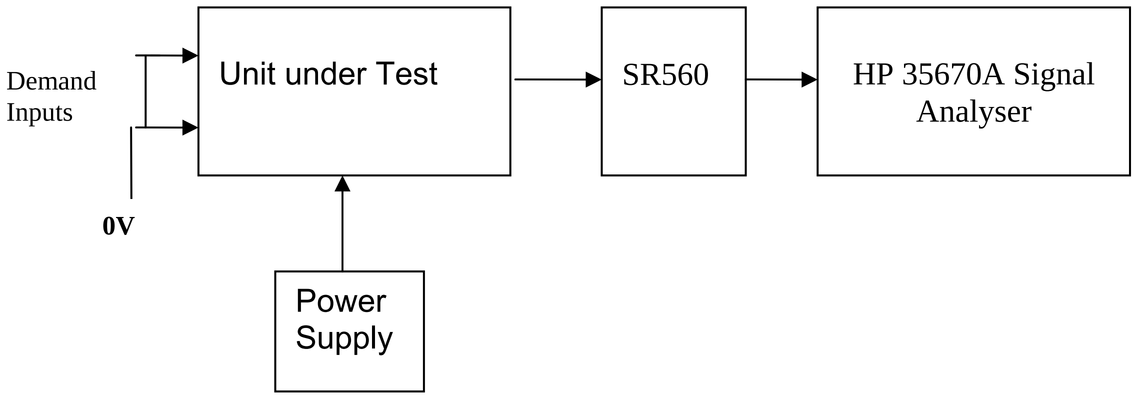
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	**CH1 IC1**	41.1	√
CH1 Negative		**CH1 IC5**	42.6	√
CH2 Positive	12.20	**CH2 IC1**	42.6	√
CH2 Negative		**CH2 IC5**	42.1	√
CH3 Positive	12.20	**CH3 IC1**	43.8	√
CH3 Negative		**CH3 IC5**	44.8	√
CH4 Positive	12.20	**CH4 IC1**	43.1	√
CH4 Negative		**CH4 IC5**	43.3	√

Unit.......................................Serial No ....
Test Engineer ....RMC
Date 8/12/09

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-98.7	-158.7dB
Ch2	-160dB	-100.4	-160.4dB
Ch3	-160dB	-99.8	-159.8dB
Ch4	-160dB	-99.8	-159.8dB

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………….T_TOP_P34……………………..Serial No ………………………………..
Test Engineer ….Xen…….………
Date …………….22/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.27	83.0mA	120mA	84.8mA	√

Unit…………………TTOP34P…………Serial No ………………………………
Test Engineer ………RMC
Date …………………23/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP34P
Driver board ID	TTOP34P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP34P
Monitor board ID	MON55P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON55P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P35……………………Serial No ………………………………
Test Engineer ….Xen…..…..………
Date …………….9/8/10….…………

Drive Card ID……T_TOP35P…………
Monitor Card ID...Mon45………………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

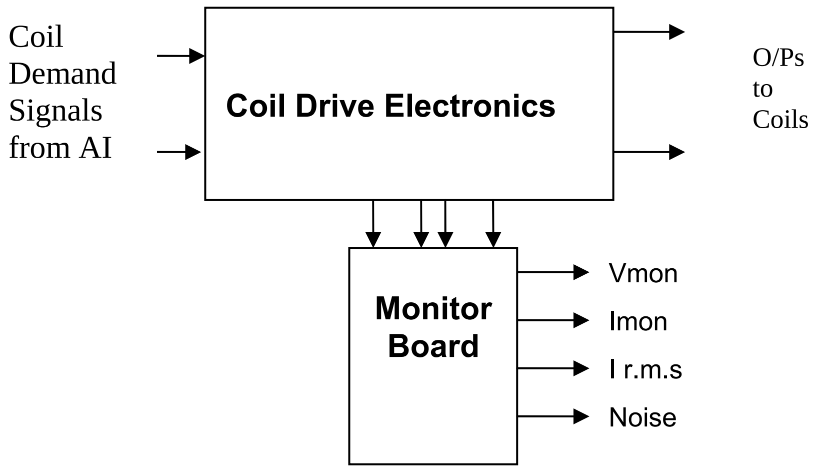


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P35……………………Serial No ………………………………
Test Engineer ….Xen…..…………..
Date …………….9/8/10…..………..

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P35……………………Serial No ………………………………
Test Engineer ….Xen………………
Date ……………21/1/10…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Four 0.39uF filter capacitors have been added to the driver board (C200).
Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P35……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….21/1/10…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit…………………T_TOP_P35……………………….Serial No …………………………………
Test Engineer ….Xen…….………
Date ………………21/1/10…………

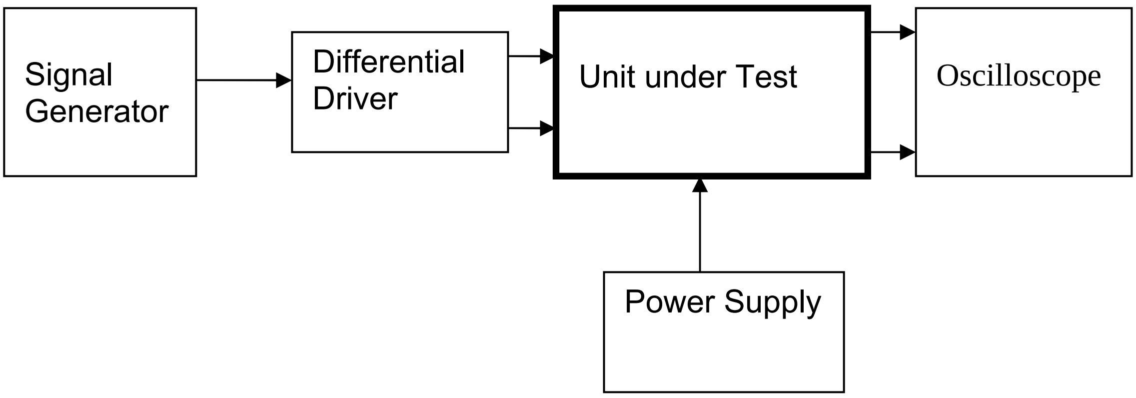
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P35……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….21/1/10…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P35……………………Serial No ……………………………
Test Engineer ….Xen……..……..
Date ……………21/1/10…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P35……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….21/1/10…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.749	√
	Pin 1	RMS Current	0.75v dc	0.757	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.750	√
	Pin 4	RMS Current	0.75v dc	0.754	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.750	√
	Pin 7	RMS Current	0.75v dc	0.753	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.749	√

Unit………………T_TOP_P35……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….21/1/10………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.26	2.9μV√Hz	√
2		0.96	2.9μV√Hz	√
3		1.64	2.9μV√Hz	√
4		0.94	2.9μV√Hz	√

Unit……………..T_TOP_P35……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….21/1/10…………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit..................T_TOP_P35........................Serial No ....
Test Engineer ....Xen................
Date ....21/1/10............

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

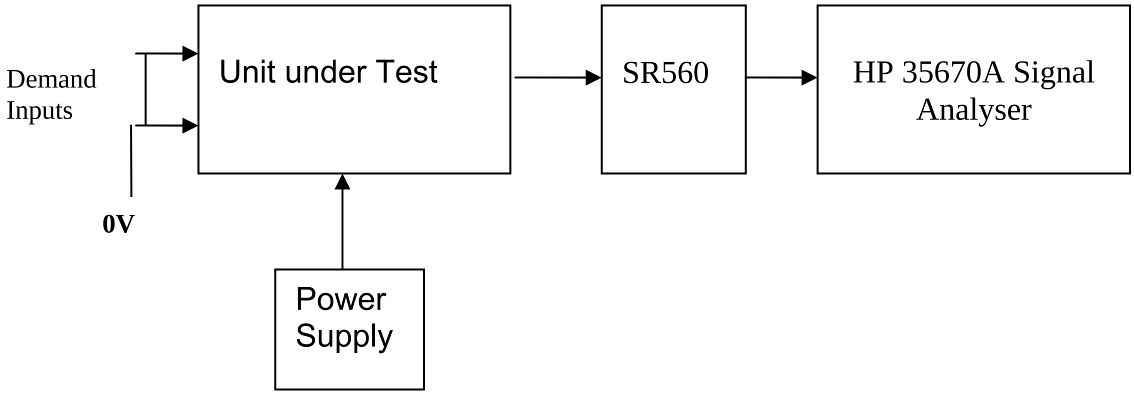
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.21	**CH1 IC1**	37.0	√
CH1 Negative		**CH1 IC5**	38.7	√
CH2 Positive	12.21	**CH2 IC1**	39.2	√
CH2 Negative		**CH2 IC5**	39.7	√
CH3 Positive	12.21	**CH3 IC1**	38.7	√
CH3 Negative		**CH3 IC5**	38.7	√
CH4 Positive	12.21	**CH4 IC1**	37.0	√
CH4 Negative		**CH4 IC5**	39.2	√

Unit……………..T_TOP_P35…………………..Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….28/7/10…………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-98.7	-158.7
Ch2	-160dB	-100.4	-160.4
Ch3	-160dB	-98.5	-158.5
Ch4	-160dB	-101.1	-161.1

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P35……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….26/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.27	83.2mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit...............TTOP35P...........................Serial No ....
Test Engineer ....RMC
Date 24/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP35P
Driver board ID	TTOP35P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP35P
Monitor board ID	MON45P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON45P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P36……………………Serial No ………………………………
Test Engineer ….Xen…..…..………
Date …………….9/8/10…..…………

Drive Card ID……T_TOP36P…………
Monitor Card ID...Mon56………………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

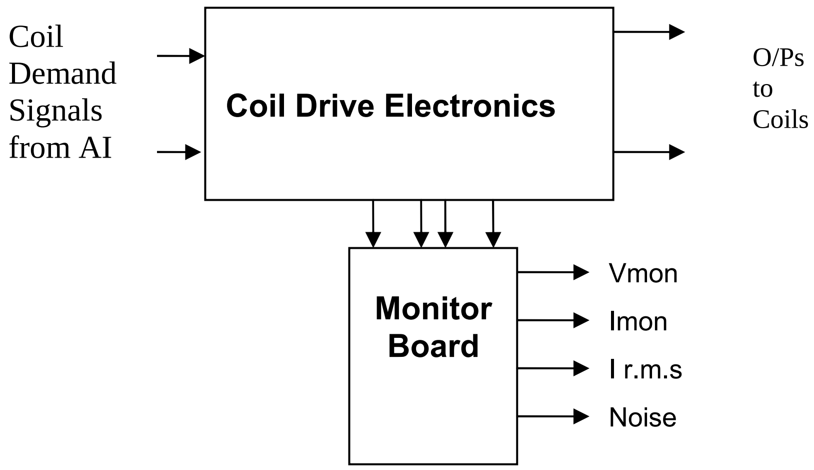


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P36……………………Serial No ………………………………
Test Engineer ….Xen…..….………
Date …………….9/8/10…..………..

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P36……………………Serial No ………………………………
Test Engineer ….Xen……..……
Date …………….20/1/10…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 3 & 4.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P36……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….20/1/10…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P36……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….20/1/10…………

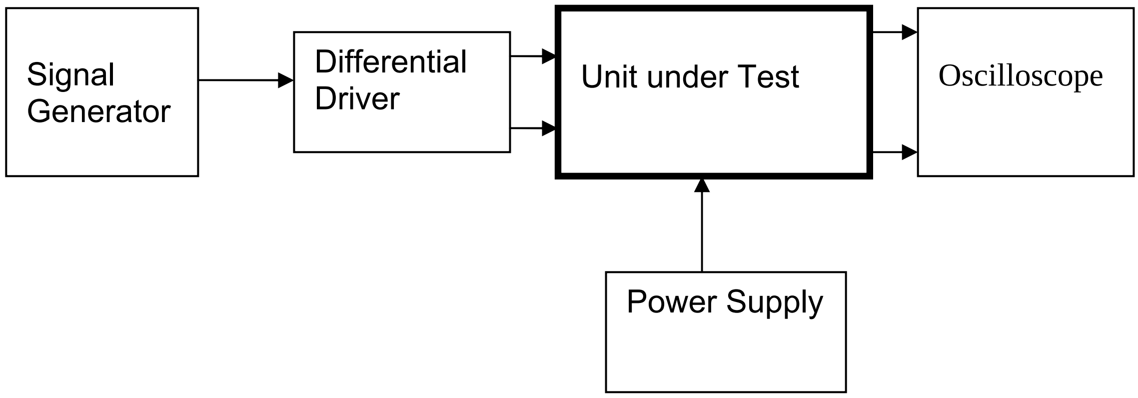
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P36........................Serial No ....
Test Engineer ....Xen.................
Date ....20/1/10............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit..................T_TOP_P36........................Serial No ....
Test Engineer ....Xen................
Date ....20/1/10............

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P36……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….20/1/10…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.750	√
	Pin 1	RMS Current	0.75v dc	0.754	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.748	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.751	√

Unit………………T_TOP_P36……………………Serial No ………………………………
Test Engineer ….Xen………..……
Date …………….20/1/10…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.13	2.9μV√Hz	√
2		0.99	2.9μV√Hz	√
3		1.10	2.9μV√Hz	√
4		1.55	2.9μV√Hz	√

Unit……………..T_TOP_P36…………………..Serial No ……………………………..
Test Engineer ….Xen…………….
Date …………….20/1/10………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit.................T_TOP_P36......................Serial No ....
Test Engineer ....Xen................
Date ....20/1/10...........

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

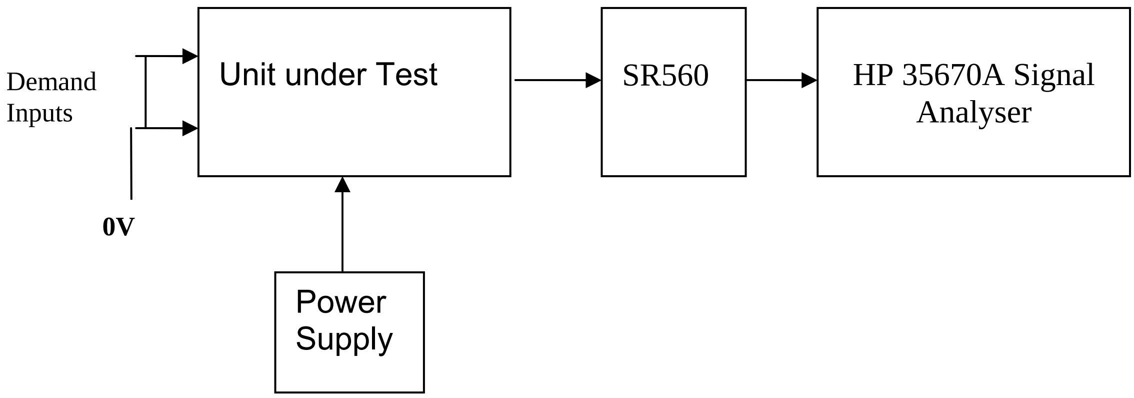
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.20	**CH1 IC1**	40.4	√
CH1 Negative		**CH1 IC5**	42.3	√
CH2 Positive	12.20	**CH2 IC1**	41.1	√
CH2 Negative		**CH2 IC5**	42.3	√
CH3 Positive	12.20	**CH3 IC1**	40.6	√
CH3 Negative		**CH3 IC5**	41.8	√
CH4 Positive	12.20	**CH4 IC1**	39.9	√
CH4 Negative		**CH4 IC5**	41.4	√

Unit.................T_TOP_P36.......................Serial No ....
Test Engineer ....Xen................
Date ....28/7/10............

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.4	-161.4
Ch2	-160dB	-99.6	-159.6
Ch3	-160dB	-102.0	-162.0
Ch4	-160dB	-101.6	-161.6

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P36……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date ……………23/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP36…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………23/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP36P
Driver board ID	TTOP36P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP36P
Monitor board ID	MON56P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON56P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P37……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….28/7/10…………..

Drive Card ID……T_TOP37P…………
Monitor Card ID...Mon58P….…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

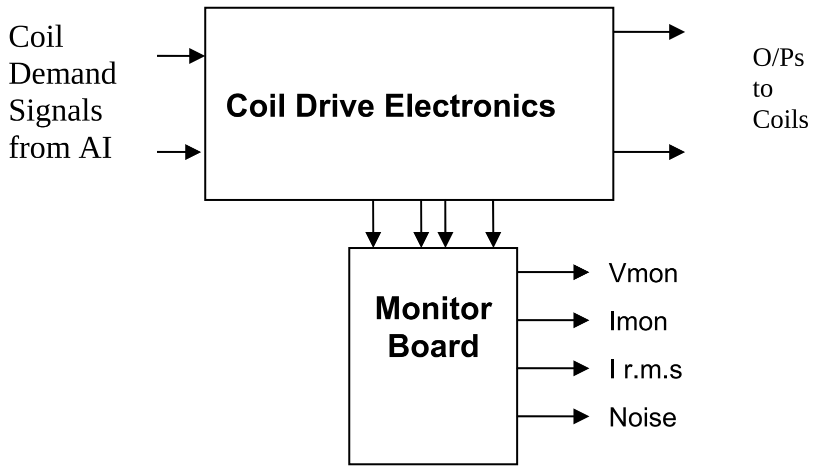


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen..…..…………
Date …………….28/7/10…….……..

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P37……………………Serial No ………………………………
Test Engineer ….Xen……………..
Date …………….13/11/09………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit.................T_TOP_P37.......................Serial No ....
Test Engineer ....Xen.................
Date ....13/11/09.............

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit.................T_TOP_P37.......................Serial No ....
Test Engineer ....Xen..............…….
Date ....13/11/09…….....…..

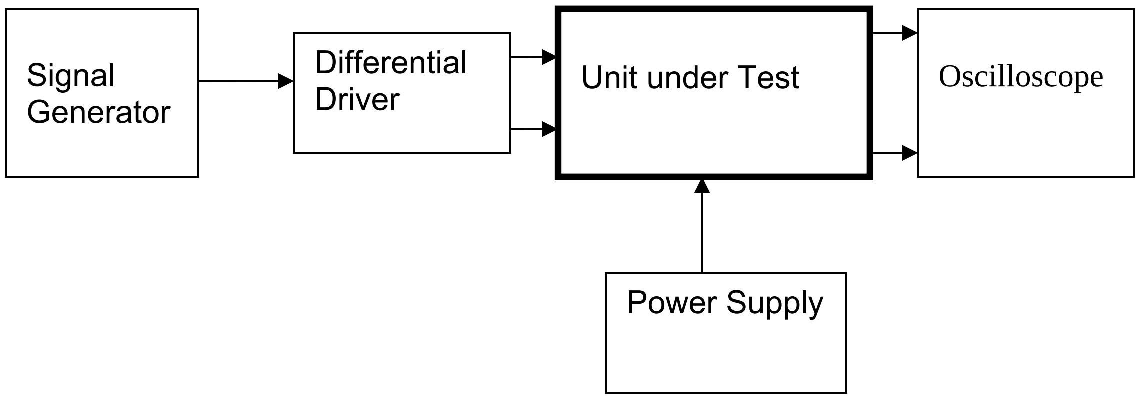
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P37........................Serial No ....
Test Engineer ....Xen..................
Date ....13/11/09.............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P37……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….13/11/09………...

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P37……………………Serial No ………………………………
Test Engineer ….Xen…………..……
Date …………….13/11/09……..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.754	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.753	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.759	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.752	√

Unit………………T_TOP_P37……………………Serial No ………………………………
Test Engineer ….Xen…………
Date …………….13/11/09……

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.51	2.9μV√Hz	√
2		1.05	2.9μV√Hz	√
3		1.40	2.9μV√Hz	√
4		1.08	2.9μV√Hz	√

Unit……………..T_TOP_P37……………………Serial No ……………………………..
Test Engineer ….Xen………..
Date …………….13/11/09……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.8		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P37……………………Serial No ………………………………
Test Engineer ….Xen………..
Date …………….13/11/09……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

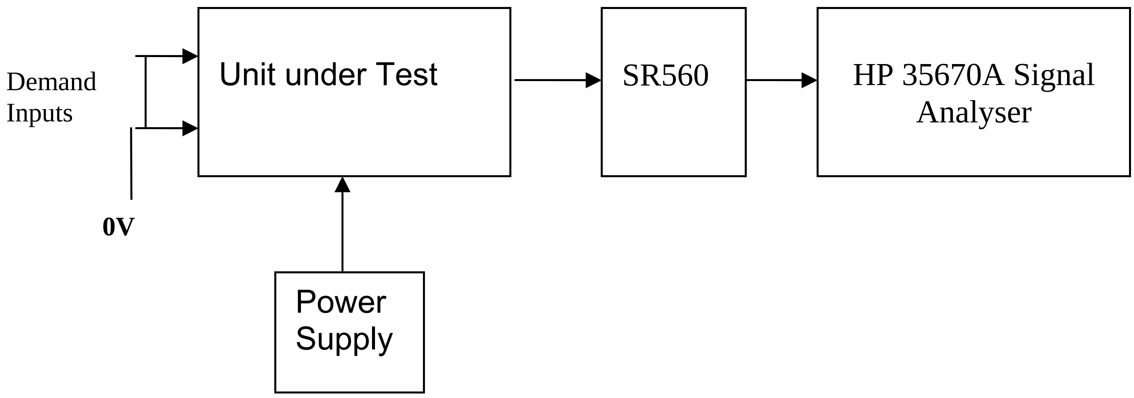
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.18	**CH1 IC1**	42.3	√
CH1 Negative		**CH1 IC5**	42.8	√
CH2 Positive	12.18	**CH2 IC1**	43.6	√
CH2 Negative		**CH2 IC5**	43.6	√
CH3 Positive	12.18	**CH3 IC1**	43.1	√
CH3 Negative		**CH3 IC5**	42.3	√
CH4 Positive	12.18	**CH4 IC1**	42.3	√
CH4 Negative		**CH4 IC5**	44.3	√

Unit…………………..T_TOP_P37……………..Serial No ……………………………..
Test Engineer ………RMC (1, 2 & 3) / Xen (4)…..
Date …………………30/11/09 / 28/7/10…………..

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-98.3	-158.3
Ch2	-160dB	-101.3	-161.3
Ch3	-160dB	-99.2	-159.2
Ch4	-160dB	-100.7	-160.7

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P37……………………Serial No ………………………………
Test Engineer ….Xen…………
Date ……………27/7/10..……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………………TTOP37P………………Serial No ………………………………
Test Engineer ………RMC
Date …………………24/8/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP37P
Driver board ID	TTOP37P
Driver board Drawing No/Issue No	D0902747_V8
Driver board Serial Number	TTOP37P
Monitor board ID	MON58P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON58P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P38……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….10/8/10…………

Drive Card ID……T_TOP38P…………
Monitor Card ID...Mon57………………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

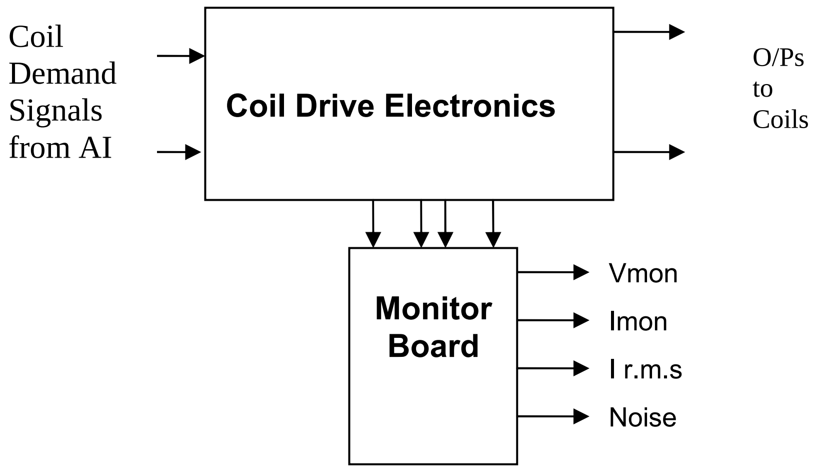


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit..................T_TOP_P38........................Serial No ....
Test Engineer ....Xen.................
Date ....10/8/10............

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P38……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….20/1/10…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Removed capacitors C27 and C32 on all channels and replaced the 33pF ceramic capacitor with a 33pF polypropylene capacitor.

Four 0.39uF filter capacitors have been added to the driver board (C200).
Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………..T_TOP_P38……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….20/1/10…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit..................T_TOP_P38........................Serial No ....
Test Engineer ....Xen................
Date ....20/1/10............

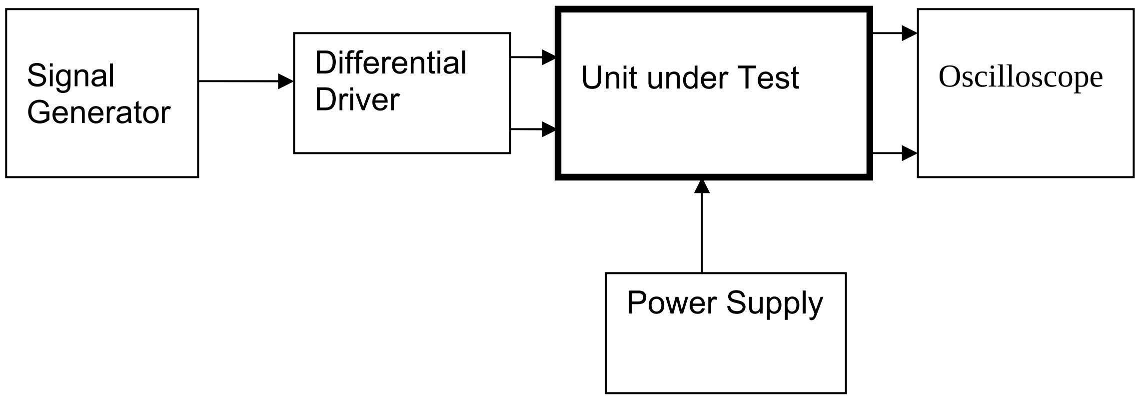
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P38……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….20/1/10…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P38……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date ……………20/1/10…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P38……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….20/1/10…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.753	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.753	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.752	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.751	√

Unit……………..T_TOP_P38……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….20/1/10…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		0.92	2.9μV√Hz	√
2		1.02	2.9μV√Hz	√
3		1.28	2.9μV√Hz	√
4		1.24	2.9μV√Hz	√

Unit……………..T_TOP_P38……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….20/1/10…………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.8		
10Hz	-30.9		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.7		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit.................T_TOP_P38.......................Serial No ....
Test Engineer ....Xen................
Date ....20/1/10............

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

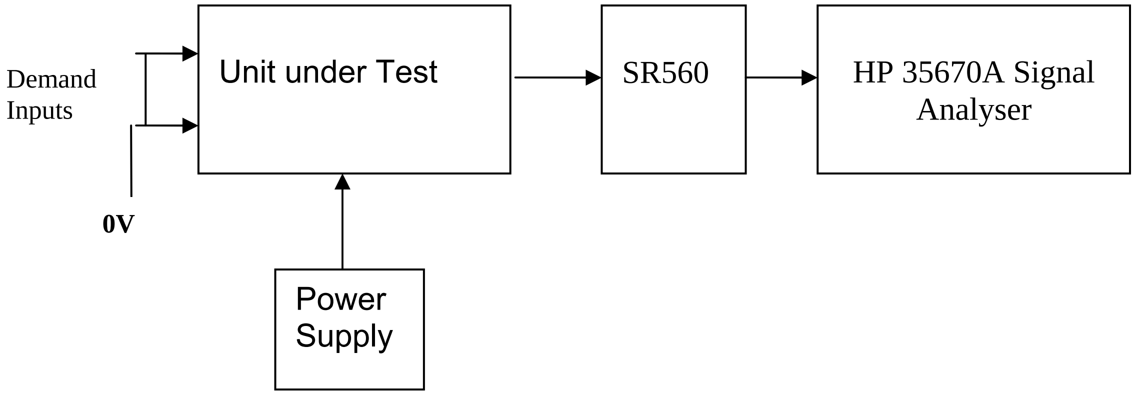
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.21	**CH1 IC1**	39.7	√
CH1 Negative		**CH1 IC5**	40.9	√
CH2 Positive	12.21	**CH2 IC1**	40.6	√
CH2 Negative		**CH2 IC5**	42.8	√
CH3 Positive	12.21	**CH3 IC1**	40.4	√
CH3 Negative		**CH3 IC5**	41.6	√
CH4 Positive	12.21	**CH4 IC1**	39.7	√
CH4 Negative		**CH4 IC5**	41.6	√

Unit……………..T_TOP_P38…………………..Serial No ……………………………
Test Engineer ….Xen…………….
Date …………….26/7/10………..

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.9	-159.9
Ch2	-160dB	-100.1	-160.1
Ch3	-160dB	-99.9	-159.9
Ch4	-160dB	-100.9	-160.9

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P38……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date ……………26/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V =	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………………TTOP38P………Serial No ………………………………
Test Engineer ………RMC
Date …………………30/9/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP38P
Driver board ID	TTOP38P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP38P
Monitor board ID	MON57P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON57P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….10/9/10………………

Drive Card ID……T_TOP39P…………
Monitor Card ID...Mon100……………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

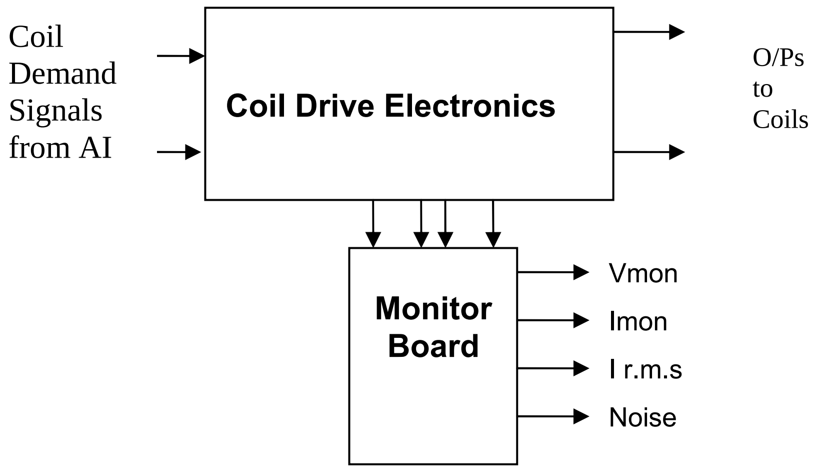


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….10/9/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….20/1/10…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………….T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….20/1/10…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….20/1/10…………

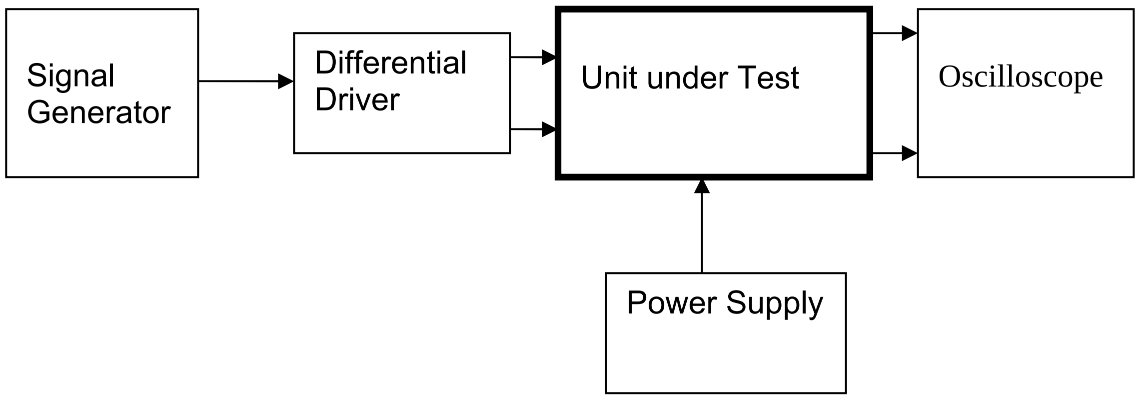
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	**Resistance**	**OK?**
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….20/1/10…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….20/1/10…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….20/1/10………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.752	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.752	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.753	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.751	√

Unit………………T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….20/1/10………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.01	2.9μV√Hz	√
2		1.26	2.9μV√Hz	√
3		1.37	2.9μV√Hz	√
4		1.34	2.9μV√Hz	√

Unit……………..T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen……………
Date ……………20/1/10…………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit.................T_TOP_P39.......................Serial No ....
Test Engineer ....Xen................
Date ....20/1/10............

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

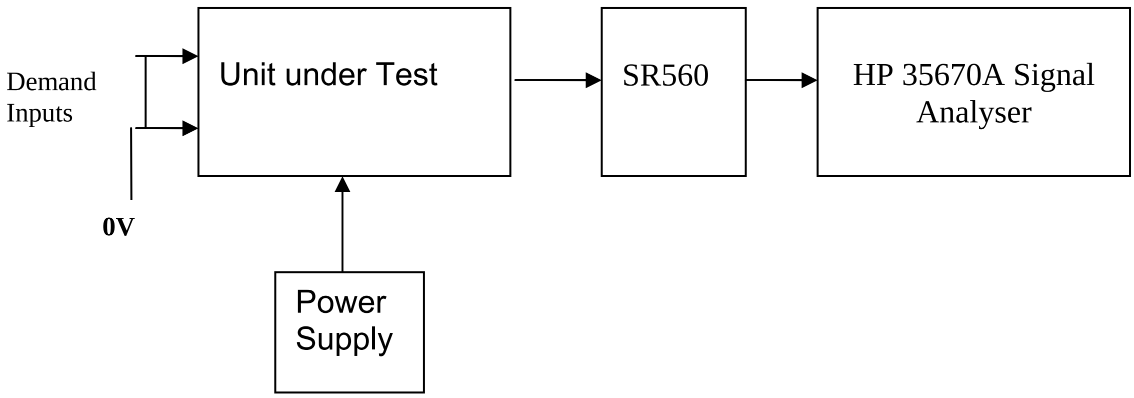
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.18	CH1 IC1	40.1	√
CH1 Negative		CH1 IC5	42.6	√
CH2 Positive	12.18	CH2 IC1	42.1	√
CH2 Negative		CH2 IC5	42.6	√
CH3 Positive	12.18	CH3 IC1	41.8	√
CH3 Negative		CH3 IC5	42.6	√
CH4 Positive	12.18	CH4 IC1	41.4	√
CH4 Negative		CH4 IC5	40.1	√

Unit……………..T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….23/7/10………..

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.9	-159.9
Ch2	-160dB	-102.1	-162.1
Ch3	-160dB	-102.6	-162.6
Ch4	-160dB	-99.9	-159.9

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P39……………………Serial No ………………………………
Test Engineer ….Xen……………
Date ……………23/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit………………TTOP39P……………Serial No ………………………………
Test Engineer ………RMC
Date …………………30/9/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP39P
Driver board ID	TTOP39P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP39P
Monitor board ID	MON100P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON100P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P40……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….7/7/10..…………

Drive Card ID……T_TOP40P…………
Monitor Card ID...Mon101……………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

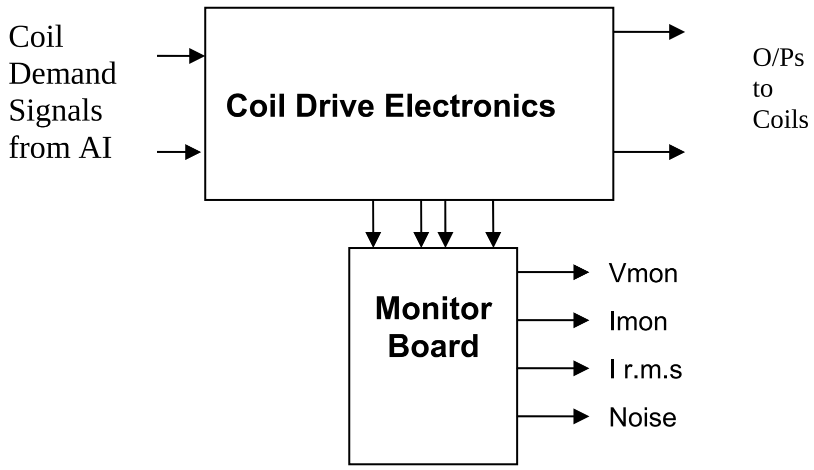


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit..................T_TOP_P40........................Serial No ....
Test Engineer ....Xen.................
Date ....7/7/10..............

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P40……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….19/1/10…………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit.................T_TOP_P40.......................Serial No ....
Test Engineer ....Xen...............
Date ....19/1/10...........

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………..T_TOP_P40……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10…………

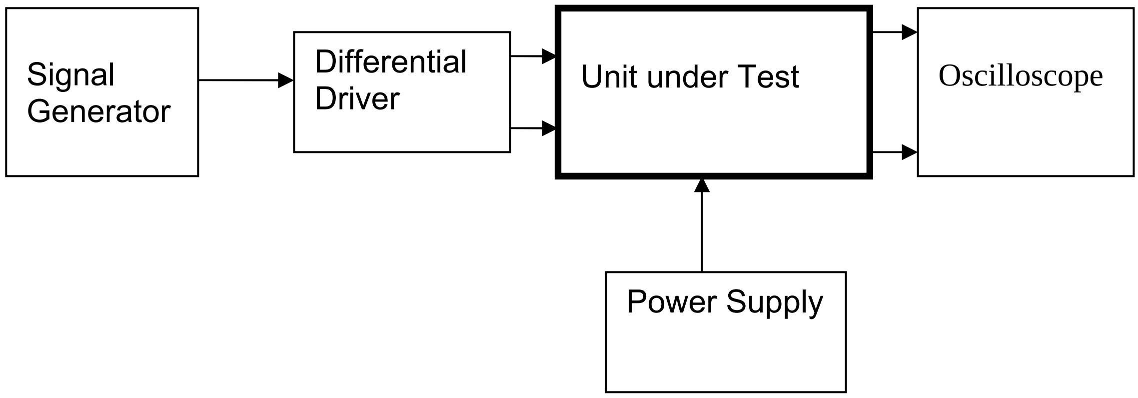
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….T_TOP_P40……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….19/1/10…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit..................T_TOP_P40........................Serial No ....
Test Engineer ....Xen.................
Date ....19/1/10............

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P40……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….6/7/10..…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.751	√
	Pin 1	RMS Current	0.75v dc	0.759	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.747	√
	Pin 4	RMS Current	0.75v dc	0.750	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.749	√
	Pin 10	RMS Current	0.75v dc	0.752	√

Unit..................T_TOP_P40.......................Serial No ....
Test Engineer ....Xen................
Date ....6/7/10..............

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.84	2.9μV√Hz	√
2		1.84	2.9μV√Hz	√
3		0.78	2.9μV√Hz	√
4		1.02	2.9μV√Hz	√

Unit……………..T_TOP_P40……………………Serial No ……………………………..
Test Engineer ….Xen…………….
Date …………….6/7/10…………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..T_TOP_P40……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date ……………6/7/10..…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

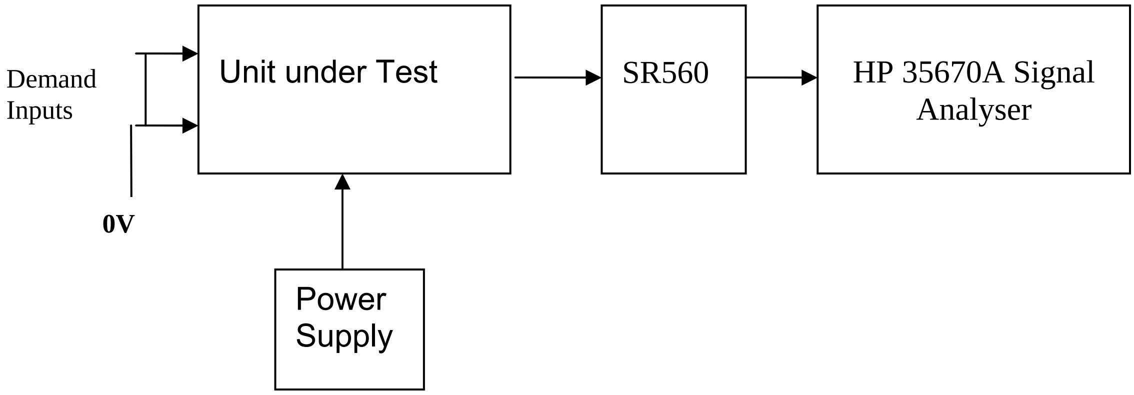
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.19	**CH1 IC1**	38.2	√
CH1 Negative		**CH1 IC5**	40.9	√
CH2 Positive	12.20	**CH2 IC1**	40.4	√
CH2 Negative		**CH2 IC5**	43.1	√
CH3 Positive	12.20	**CH3 IC1**	41.4	√
CH3 Negative		**CH3 IC5**	42.6	√
CH4 Positive	12.20	**CH4 IC1**	38.9	√
CH4 Negative		**CH4 IC5**	41.1	√

Unit.................T_TOP_P40.......................Serial No ....
Test Engineer ....Xen................
Date ....6/7/10..............

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-160dB	-100.7	-160.7
Ch2	-160dB	-101.7	-161.7
Ch3	-160dB	-101.2	-161.2
Ch4	-160dB	-99.9	-159.9

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P40……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….6/7/10..…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………TTOP40P…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………23/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred.

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP40P
Driver board ID	TTOP40P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP40P
Monitor board ID	MON101
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON101

10. Check the security of any modification wires. √

11. Visually inspect.√

12. Put the lid on and fasten all screws, √

Check all external screws for tightness.√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P41……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….28/7/10…………

Drive Card ID……T_TOP41P………….
Monitor Card ID...Mon102……………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

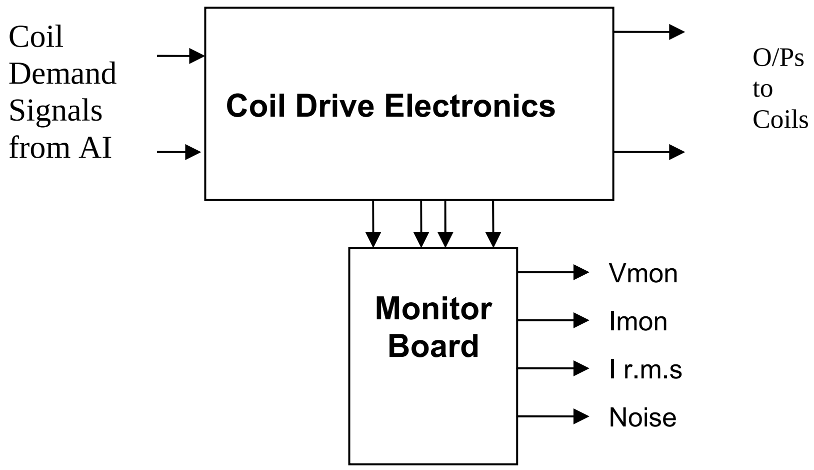


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit..................T_TOP_P41........................Serial No ....
Test Engineer ....Xen.................
Date ....28/7/10............

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit.................T_TOP_P41.......................Serial No ....
Test Engineer ....Xen.................
Date ....19/1/10...........

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P41……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….19/1/10…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit..................T_TOP_P41.........................Serial No ....
Test Engineer ....Xen................
Date ....19/1/10............

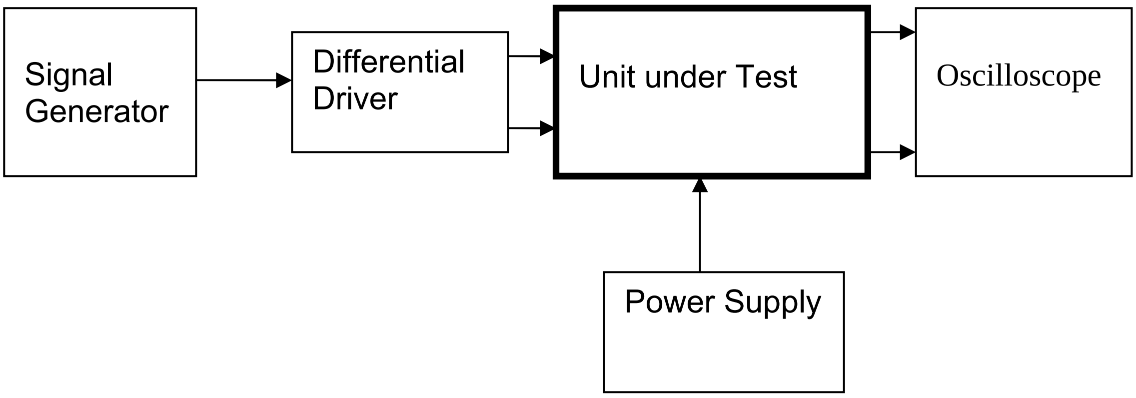
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P41……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….19/1/10…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P41……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….19/1/10…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P41……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….19/1/10…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.751	√
	Pin 1	RMS Current	0.75v dc	0.754	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.754	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit……………..T_TOP_P41……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors
- Monitor coil inputs to board were grounded for all channels.
Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.42	2.9μV√Hz	√
2		1.72	2.9μV√Hz	√
3		1.53	2.9μV√Hz	√
4		1.97	2.9μV√Hz	√

Unit.................T_TOP_P41.......................Serial No ....
Test Engineer ....Xen................
Date ....19/1/10...........

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P41……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.21	**CH1 IC1**	39.7	√
CH1 Negative		**CH1 IC5**	42.6	√
CH2 Positive	12.21	**CH2 IC1**	40.4	√
CH2 Negative		**CH2 IC5**	39.7	√
CH3 Positive	12.20	**CH3 IC1**	40.1	√
CH3 Negative		**CH3 IC5**	42.1	√
CH4 Positive	12.21	**CH4 IC1**	39.2	√
CH4 Negative		**CH4 IC5**	42.1	√

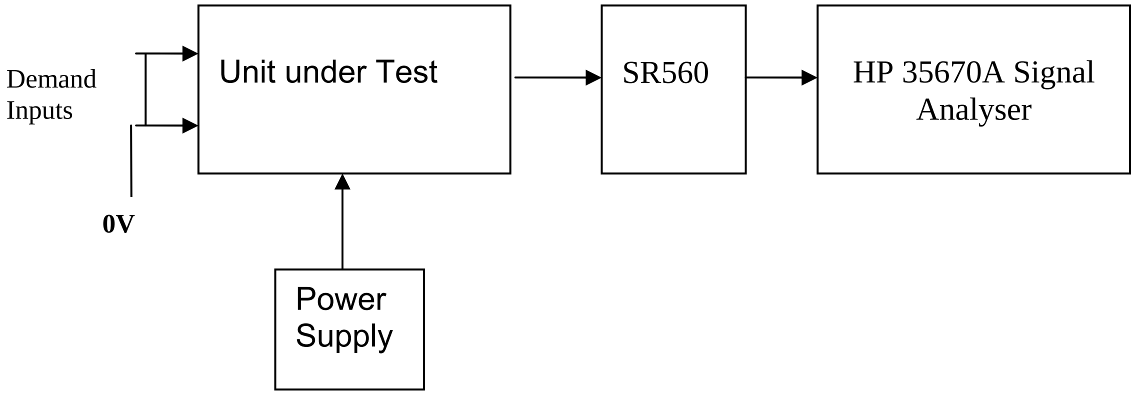
Unit……………..T_TOP_P41……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….28/7/10………..

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-160dB	-100.5	-160.5
Ch2	-160dB	-100.3	-160.3
Ch3	-160dB	-99.2	-159.2
Ch4	-160dB	-101.1	-161.1

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………….T_TOP_P41……………………..Serial No ……………………………….
Test Engineer ….Xen…….………
Date …………….23/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP41P……………Serial No ………………………………
Test Engineer ………RMC
Date …………………23/8/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP41P
Driver board ID	TTOP41P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP41P
Monitor board ID	MON102
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON102

10. Check the security of any modification wires. √

11. Visually inspect.√

12. Put the lid on and fasten all screws, √

Check all external screws for tightness.√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P42……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….9/8/10..…………

Drive Card ID……T_TOP42P………...
Monitor Card ID...Mon103….………….

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

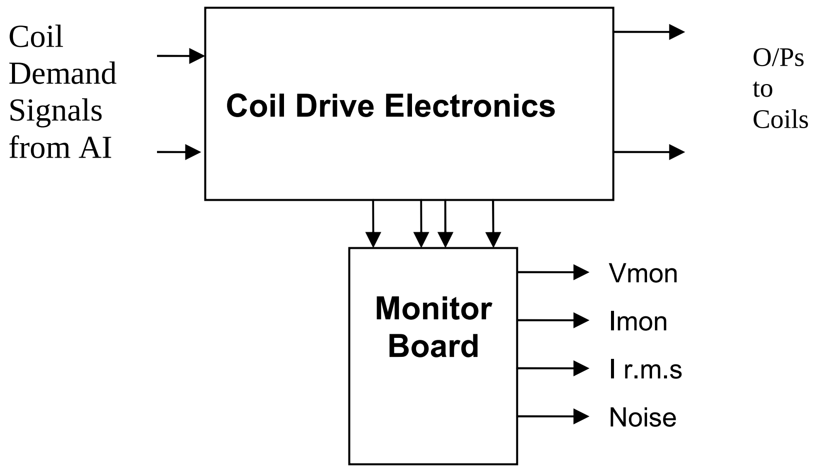


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P42……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….9/8/10..…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	**Manufacturer**	**Model**	**Serial Number**
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P42……………………Serial No ………………………………
Test Engineer ….Xen……..…….
Date …………….19/1/10………..

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………..T_TOP_P42…………………..Serial No ……………………………..
Test Engineer ….Xen…………….
Date …………….19/1/10………..

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit..................T_TOP_P42........................Serial No ....
Test Engineer ....Xen................
Date ....19/1/10............

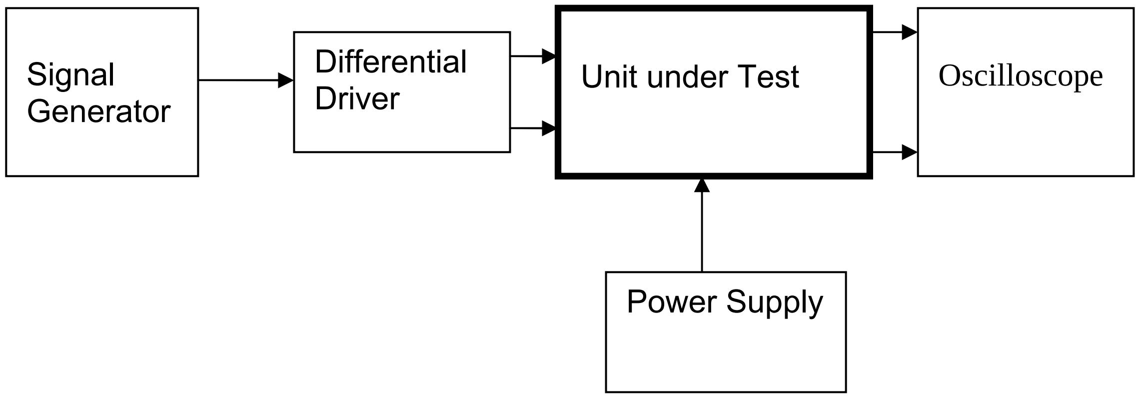
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P42……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P42……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date ……………19/1/10…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P42……………………Serial No ……………………………….
Test Engineer ….Xen…………….
Date …………….19/1/10…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	**Monitor Connector**	**Parameter**	**Theoretical Value (+/- .1v)**	**Measured Value**	**Pass/ Fail**
1	Pin 2	Current Monitor	0.75v r.m.s	0.751	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.753	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.754	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.757	√

Unit……………..T_TOP_P42……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….19/1/10…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.16	2.9μV√Hz	√
2		0.96	2.9μV√Hz	√
3		1.48	2.9μV√Hz	√
4		1.81	2.9μV√Hz	√

Unit.................T_TOP_P42.......................Serial No ....
Test Engineer ....Xen................
Date ....19/1/10............

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P42……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.19	**CH1 IC1**	40.4	√
CH1 Negative		**CH1 IC5**	43.3	√
CH2 Positive	12.19	**CH2 IC1**	41.1	√
CH2 Negative		**CH2 IC5**	42.1	√
CH3 Positive	12.19	**CH3 IC1**	41.8	√
CH3 Negative		**CH3 IC5**	42.6	√
CH4 Positive	12.19	**CH4 IC1**	40.4	√
CH4 Negative		**CH4 IC5**	41.6	√

Unit……………..T_TOP_P42……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….28/7/10…………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

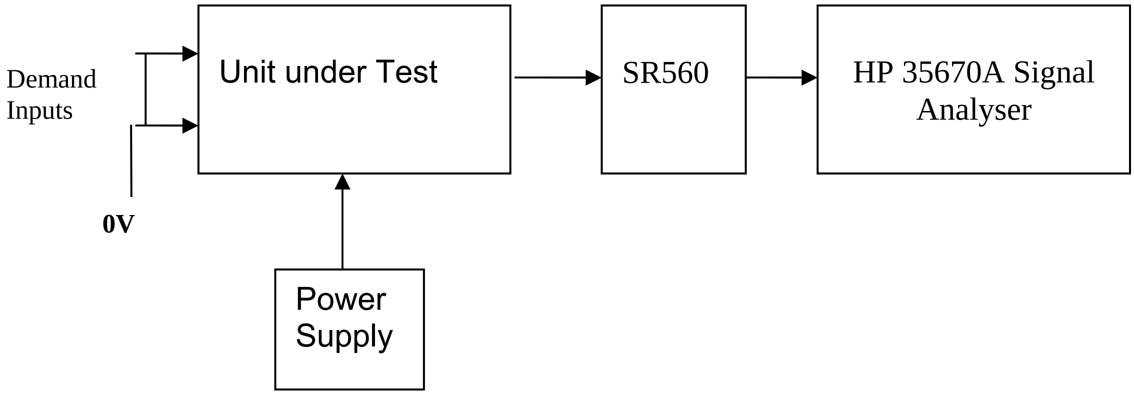
Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.

Switch the filters in.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-160dB	-98.3	-158.3
Ch2	-160dB	-100.7	-160.7
Ch3	-160dB	-100.6	-160.6
Ch4	-160dB	-100.8	-160.8

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………….T_TOP_P42……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….23/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.27	83.2mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit………… TTOP 42P ……………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………23/8/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP 42P
Driver board ID	TTOP 42P
Driver board Drawing No/Issue No	D0902747 V6
Driver board Serial Number	TTOP 42P
Monitor board ID	MON103
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON103

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….10/9/10………..

Drive Card ID……T_TOP43P…………
Monitor Card ID...Mon104……………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

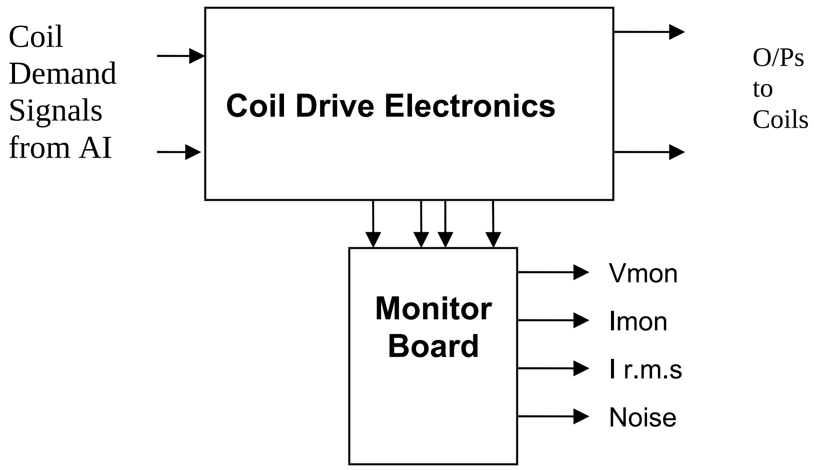


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….10/9/10…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen………..……
Date ……………19/1/10…………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 1 & 4.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………..T_TOP_P43…………………..Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10………..

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………..T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10…………

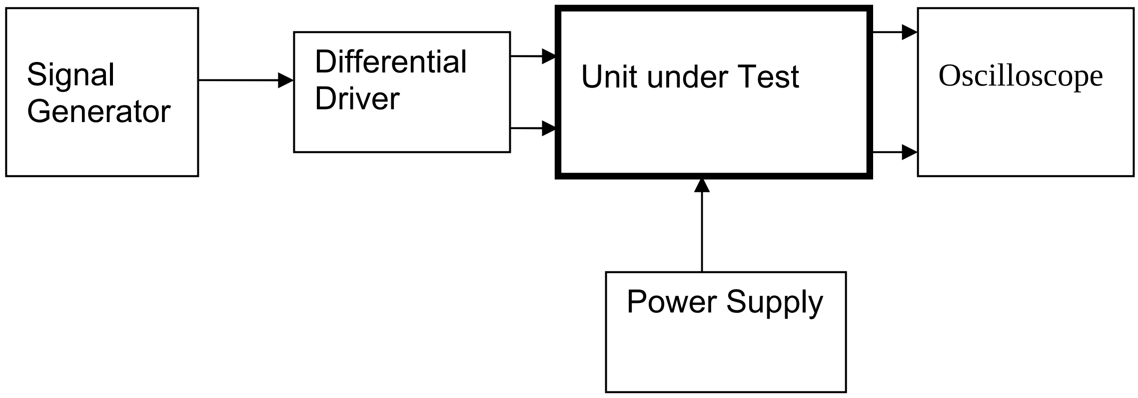
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	**Resistance**	**OK?**
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…………………T_TOP_P43…………………………Serial No ……………………………………
Test Engineer ….Xen………………
Date ………………19/1/10…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.756	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.754	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.755	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.753	√
	Pin 10	RMS Current	0.75v dc	0.756	√

Unit………………T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.47	2.9μV√Hz	√
2		1.14	2.9μV√Hz	√
3		1.23	2.9μV√Hz	√
4		1.34	2.9μV√Hz	√

Unit……………..T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen……………
Date …………….19/1/10…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	40.4	√
CH1 Negative		CH1 IC5	43.6	√
CH2 Positive	12.20	CH2 IC1	42.3	√
CH2 Negative		CH2 IC5	42.3	√
CH3 Positive	12.20	CH3 IC1	40.4	√
CH3 Negative		CH3 IC5	41.1	√
CH4 Positive	12.20	CH4 IC1	40.6	√
CH4 Negative		CH4 IC5	42.3	√

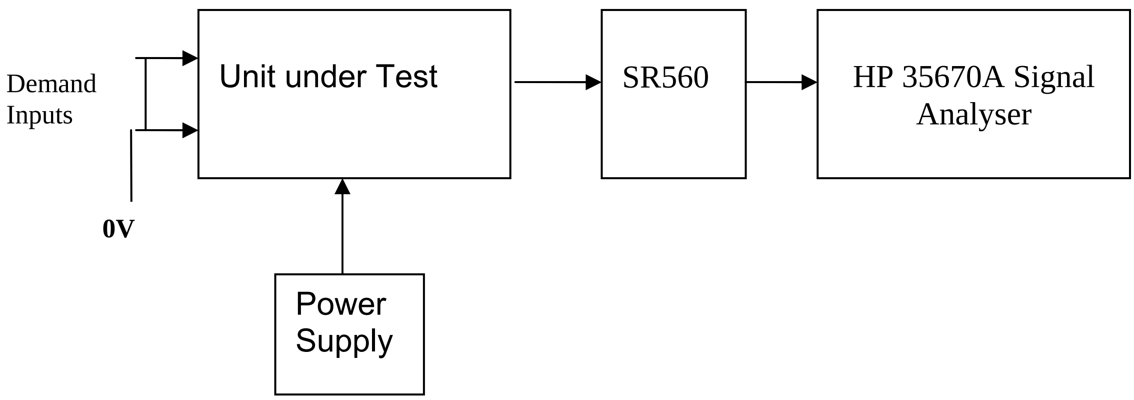
Unit……………..T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen……………
Date ……………28/7/10…………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-102.9	-162.9
Ch2	-160dB	-100.8	-160.8
Ch3	-160dB	-100.5	-160.5
Ch4	-160dB	-102.1	-162.1

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P43……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s) +/- 2.5mA**	**Pass?**
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP43P………………Serial No ………………………………
Test Engineer ………RMC
Date …………………30/9/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP43P
Driver board ID	TTOP43P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP43P
Monitor board ID	MON104
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON104

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P44……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….22/7/10…………

Drive Card ID……T_TOP44P…………
Monitor Card ID...Mon105……………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

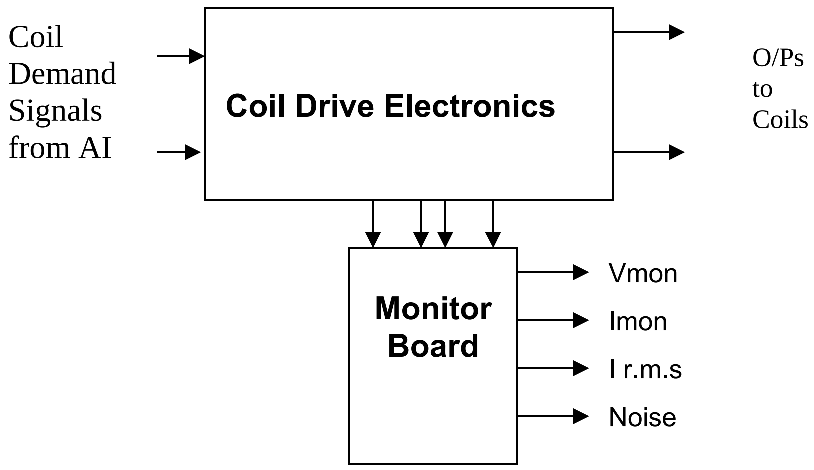


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit..................T_TOP_P44.........................Serial No ....
Test Engineer ....Xen.................
Date ....21/7/10............

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P44……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date …………….18/1/10………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH 2.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit..................T_TOP_P44........................Serial No ....
Test Engineer ....Xen.................
Date ....18/1/10............

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit..................T_TOP_P44........................Serial No ....
Test Engineer ....Xen.................
Date ....18/1/10............

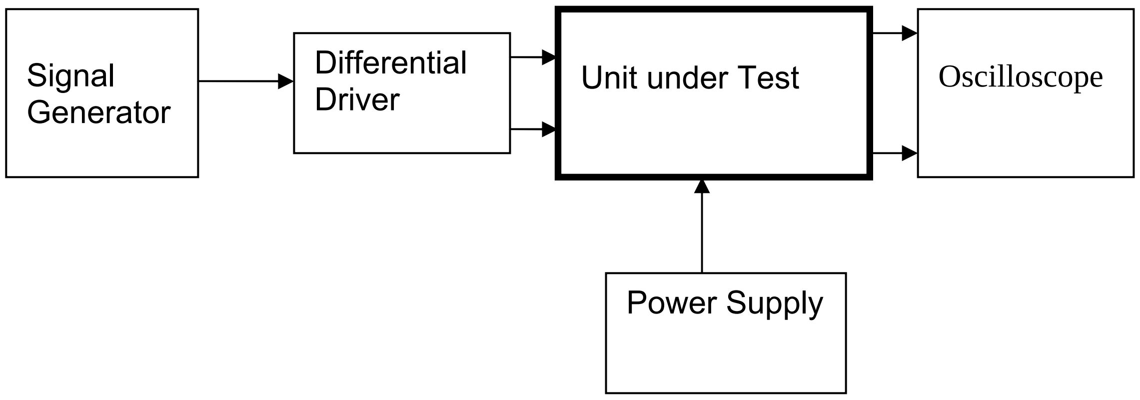
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P44……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….18/1/10…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P44……………………Serial No ………………………………
Test Engineer ….Xen…….……….
Date …………….18/1/10…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P44……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date ……………18/1/10…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.756	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.757	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.750	√
	Pin 7	RMS Current	0.75v dc	0.755	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.752	√

Unit………………T_TOP_P44……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….18/1/10…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.79	2.9μV√Hz	√
2		1.45	2.9μV√Hz	√
3		0.83	2.9μV√Hz	√
4		1.54	2.9μV√Hz	√

Unit..................T_TOP_P44........................Serial No ....
Test Engineer ....Xen.................
Date ....19/1/10............

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..T_TOP_P44……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/1/10………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	**CH1 IC1**	40.4	√
CH1 Negative		**CH1 IC5**	40.6	√
CH2 Positive	12.19	**CH2 IC1**	41.8	√
CH2 Negative		**CH2 IC5**	42.1	√
CH3 Positive	12.19	**CH3 IC1**	41.4	√
CH3 Negative		**CH3 IC5**	42.3	√
CH4 Positive	12.19	**CH4 IC1**	41.1	√
CH4 Negative		**CH4 IC5**	42.8	√

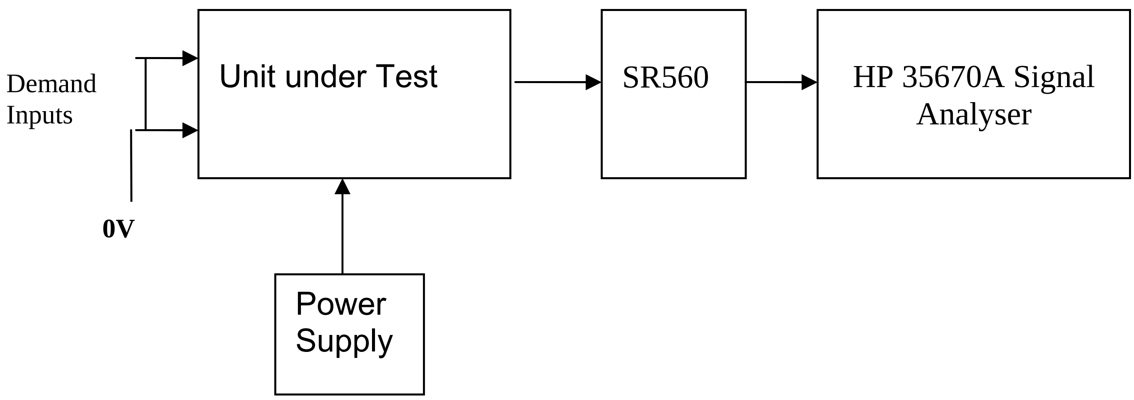
Unit.................T_TOP_P44.......................Serial No ....
Test Engineer ....Xen................
Date ....22/7/10............

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.1	-160.1
Ch2	-160dB	-103.1	-163.1
Ch3	-160dB	-97.6	-157.6
Ch4	-160dB	-103.1	-163.1

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P44……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….19/7/10…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………TTOP44P………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………5/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP44P
Driver board ID	TTOP44P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP44P
Monitor board ID	MON105
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON105

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P45……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….18/1/10…………

Drive Card ID……T_TOP45P…………
Monitor Card ID...Mon106……………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

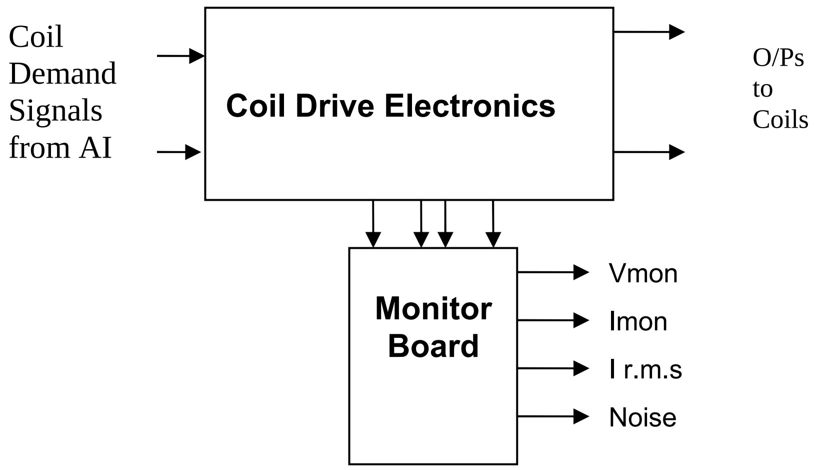


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P45……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….18/1/10…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P45……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….18/1/10…………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 2 & 3.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit……………….T_TOP_P45……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….18/1/10…………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V			
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit..................T_TOP_P45........................Serial No ....
Test Engineer ....Xen.................
Date ....18/1/10............

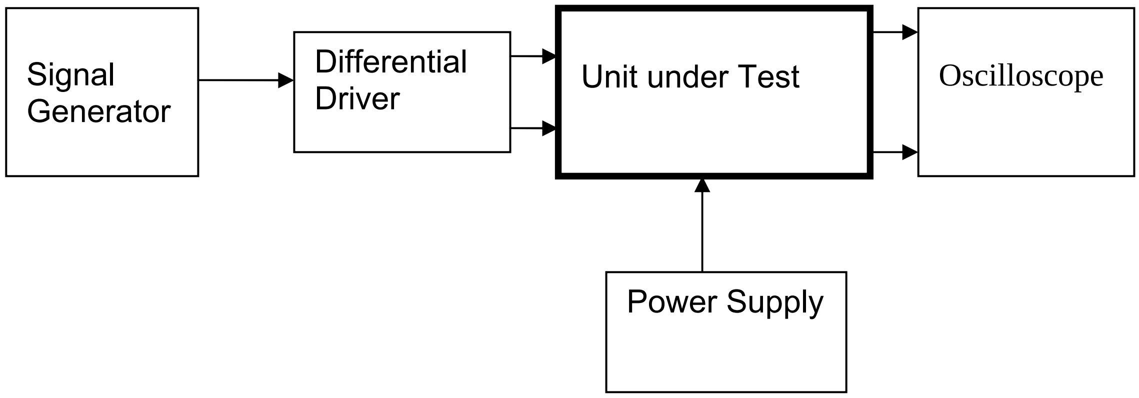
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P45……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….18/1/10…………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P45……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….18/1/10…………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P45……………………Serial No ……………………………
Test Engineer ….Xen………..…..
Date ……………18/1/10………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.752	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.749	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.750	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.751	√

Unit……………….T_TOP_P45……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….18/1/10………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.42	2.9μV√Hz	√
2		0.95	2.9μV√Hz	√
3		1.05	2.9μV√Hz	√
4		1.03	2.9μV√Hz	√

Unit………………T_TOP_P45……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….18/1/10…………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit.................T_TOP_P45.......................Serial No ....
Test Engineer ....Xen................
Date ....18/1/10............

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.19	**CH1 IC1**	39.7	√
CH1 Negative		**CH1 IC5**	41.6	√
CH2 Positive	12.19	**CH2 IC1**	40.6	√
CH2 Negative		**CH2 IC5**	42.8	√
CH3 Positive	12.19	**CH3 IC1**	40.4	√
CH3 Negative		**CH3 IC5**	42.1	√
CH4 Positive	12.19	**CH4 IC1**	38.9	√
CH4 Negative		**CH4 IC5**	40.6	√

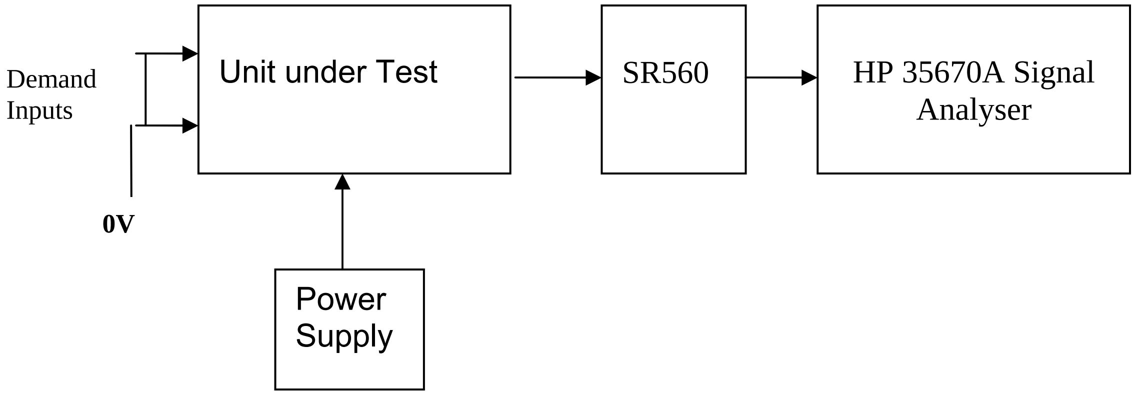
Unit…………….T_TOP_P45……………………Serial No ………………………………
Test Engineer ….Xen……………
Date ……………21/7/10…………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.3	-159.3
Ch2	-160dB	-100.9	-160.9
Ch3	-160dB	-97.8	-157.8
Ch4	-160dB	-100.9	-160.9

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P45……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….18/1/10………..

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.25	82.7mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP45P………………Serial No ………………………………
Test Engineer ………RMC
Date …………………5/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP46P
Driver board ID	TTOP46P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP46P
Monitor board ID	MON107P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON107P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

Drive Card ID……T_TOP46P…..……
Monitor Card ID…Mon107……………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

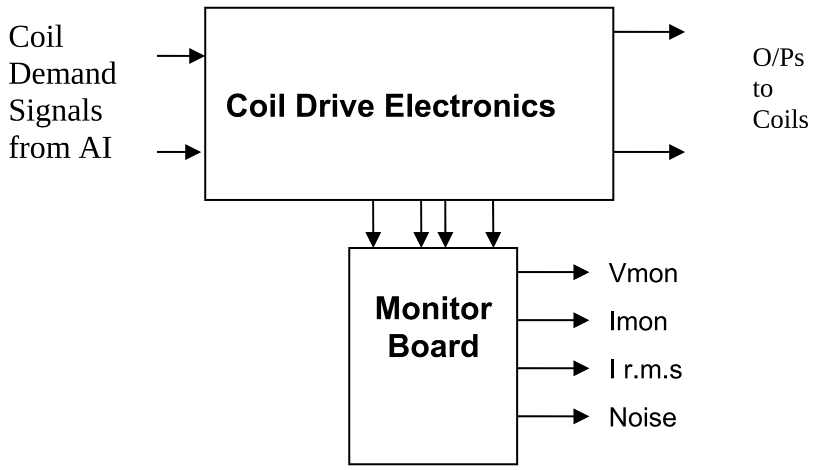


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit……………..T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10……………..……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

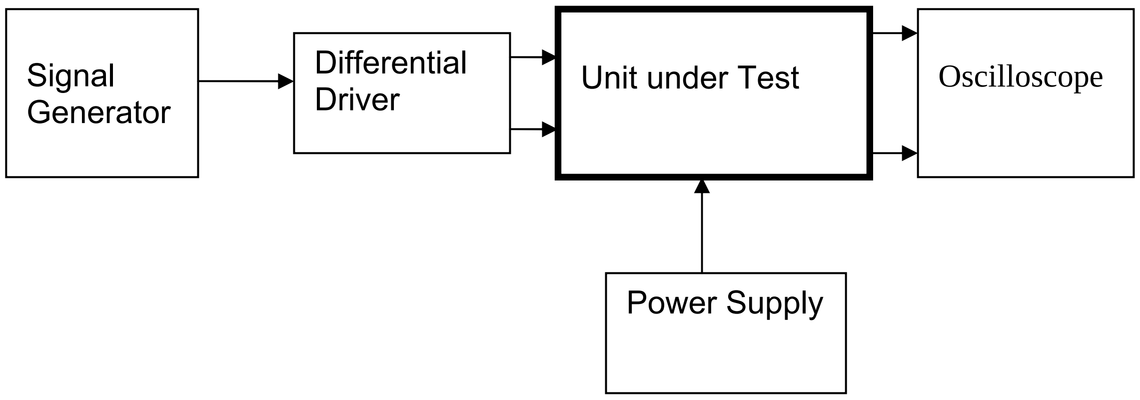
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)
Pd In from Sat pin 9, 10 = +16.5v or DC in A1
Pd In from Sat pin 11, 12 = -16.5 or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v or DC in A2

Coil Drive Outputs
Ch1+ = Coil out to Sat pin 1 Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3 Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5 Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7 Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10……………..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	**Monitor Connector**	**Parameter**	**Theoretical Value (+/- .1v)**	**Measured Value**	**Pass/ Fail**
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.758	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.759	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit………………T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.81	2.9μV√Hz	√
2		1.20	2.9μV√Hz	√
3		1.65	2.9μV√Hz	√
4		1.86	2.9μV√Hz	√

Unit………………T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..…

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..……………….
Date……………..16/7/10……………..……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	40.4	√
CH1 Negative		CH1 IC5	43.3	√
CH2 Positive	12.20	CH2 IC1	42.1	√
CH2 Negative		CH2 IC5	42.3	√
CH3 Positive	12.20	CH3 IC1	43.6	√
CH3 Negative		CH3 IC5	42.6	√
CH4 Positive	12.20	CH4 IC1	42.8	√
CH4 Negative		CH4 IC5	44.3	√

Unit……………..T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.

Replace the lid of the box, and replace screws.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode

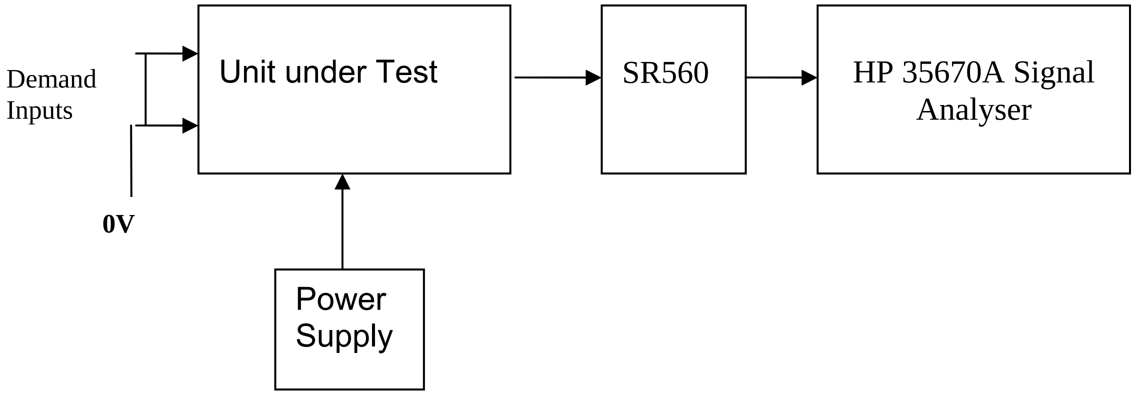
Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.

Switch the filters in.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.0	-160.0
Ch2	-160dB	-100.7	-160.7
Ch3	-160dB	-100.3	-160.3
Ch4	-160dB	-100.6	-160.6

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10…………….……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/-2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP46P……………Serial No ………………………………
Test Engineer…………………RMC
Date……………………………5/8/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP46P
Driver board ID	TTOP46P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP46P
Monitor board ID	MON107
Monitor board Drawing No/Issue No	D070480_4_k
Monitor board Serial Number	MON107

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

Drive Card ID……T_TOP47P…..……
Monitor Card ID…Mon108……………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

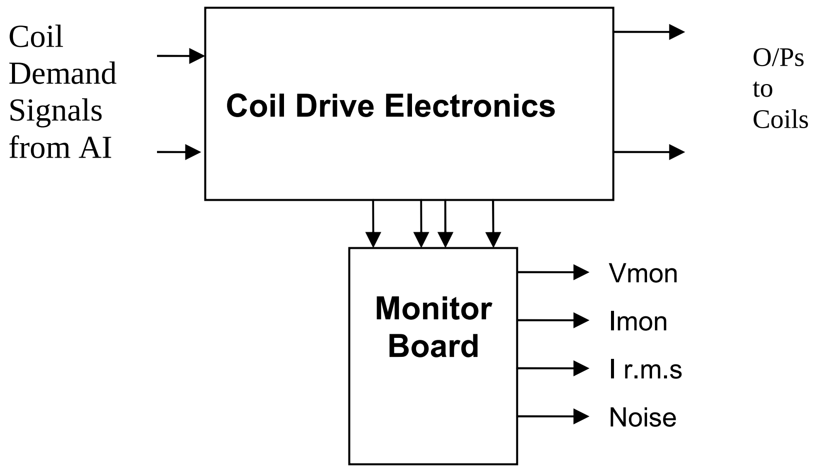


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/7/10………………..……

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH1.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit……………….T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/7/10…………….……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/7/10……………..……

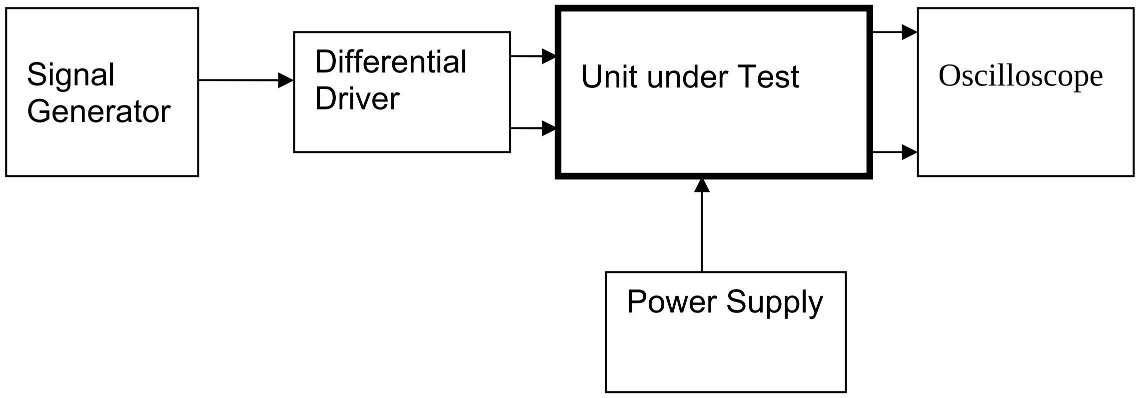
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/7/10………………..……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/7/10………………..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/7/10………………..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	**Monitor Connector**	**Parameter**	**Theoretical Value (+/- .1v)**	**Measured Value**	**Pass/ Fail**
1	Pin 2	Current Monitor	0.75v r.m.s	0.750	√
	Pin 1	RMS Current	0.75v dc	0.753	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.752	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.755	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.749	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit……………..T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/7/10………………..……

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.44	2.9μV√Hz	√
2		1.75	2.9μV√Hz	√
3		0.91	2.9μV√Hz	√
4		1.17	2.9μV√Hz	√

Unit……………..T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10…………….……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit……………….T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

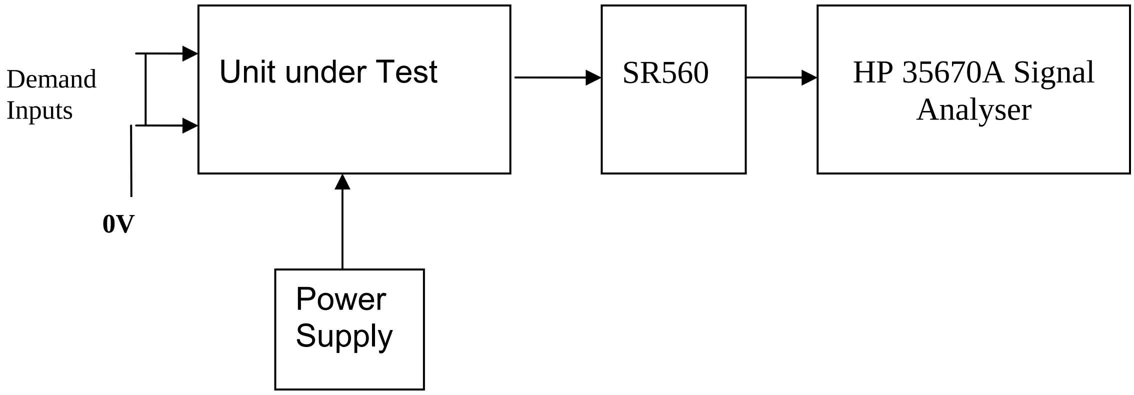
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	CH1 IC1	38.2	√
CH1 Negative		CH1 IC5	41.6	√
CH2 Positive	12.19	CH2 IC1	40.1	√
CH2 Negative		CH2 IC5	40.1	√
CH3 Positive	12.19	CH3 IC1	43.3	√
CH3 Negative		CH3 IC5	43.3	√
CH4 Positive	12.19	CH4 IC1	43.1	√
CH4 Negative		CH4 IC5	41.1	√

Unit……………..T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.8	-161.8
Ch2	-160dB	-100.1	-160.1
Ch3	-160dB	-100.8	-160.8
Ch4	-160dB	-100.3	-160.3

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..16/7/10………………..……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/-2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………………TTOP47P………………Serial No ………………………………
Test Engineer…………RMC
Date……………………18/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP47P
Driver board ID	TTOP47P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP47P
Monitor board ID	MON108
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON108

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10………………..….

Drive Card ID……T_TOP48P…..……
Monitor Card ID…Mon109……………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

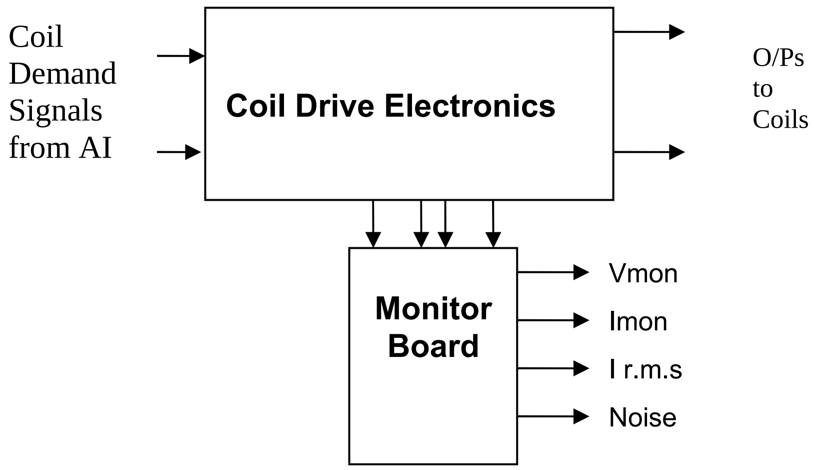


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10…………….……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10………………..……

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit………………T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10………………..……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P48……………………Serial No ……………………………….
Test Engineer…..Xen……..………………
Date……………..15/6/10……………..……

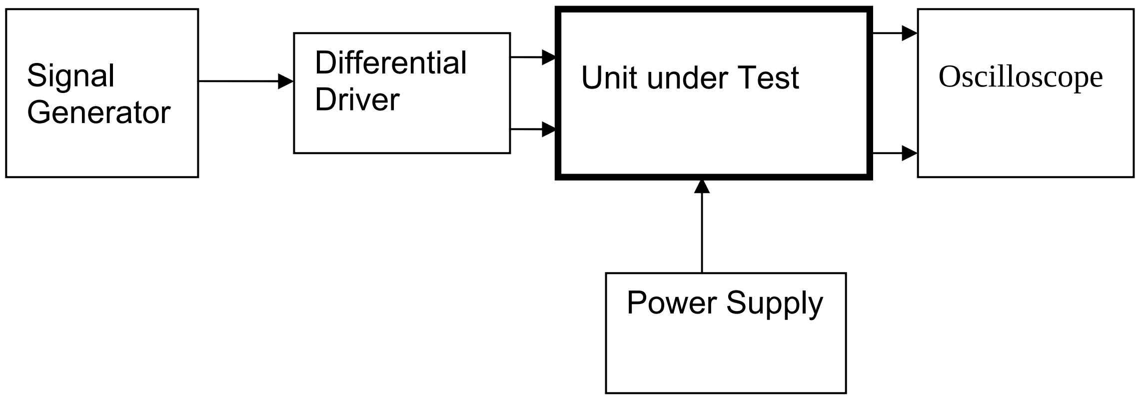
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10………………..……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10………………..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10……………..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	**Monitor Connector**	**Parameter**	**Theoretical Value (+/- .1v)**	**Measured Value**	**Pass/ Fail**
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.756	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.753	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.748	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.752	√

Unit………………T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10………………..……

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.01	2.9μV√Hz	√
2		1.22	2.9μV√Hz	√
3		1.33	2.9μV√Hz	√
4		1.10	2.9μV√Hz	√

Unit……………..T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10………………..……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit……………..T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10………………..……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

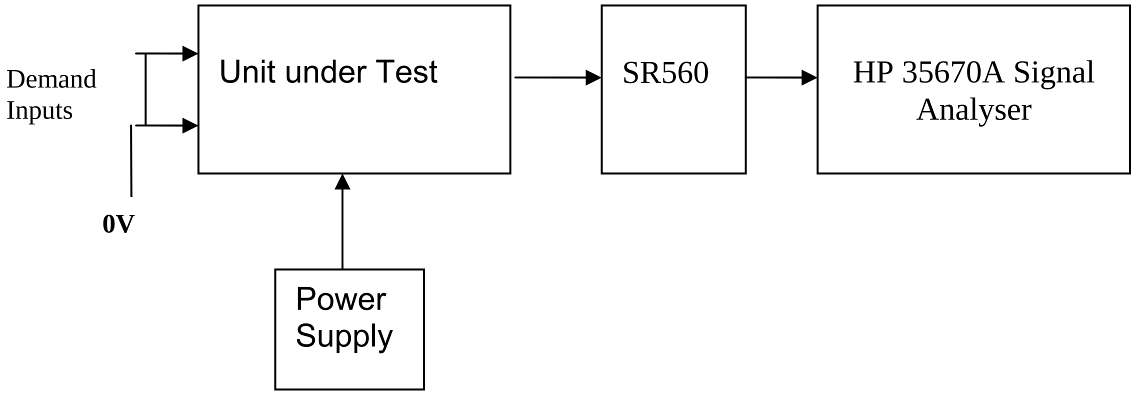
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	**CH1 IC1**	42.1	√
CH1 Negative		**CH1 IC5**	41.4	√
CH2 Positive	12.19	**CH2 IC1**	44.8	√
CH2 Negative		**CH2 IC5**	45.5	√
CH3 Positive	12.19	**CH3 IC1**	44.5	√
CH3 Negative		**CH3 IC5**	43.8	√
CH4 Positive	12.19	**CH4 IC1**	42.1	√
CH4 Negative		**CH4 IC5**	43.3	√

Unit……………..T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10…………….……

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.5	-159.5
Ch2	-160dB	-100.8	-160.8
Ch3	-160dB	-97.8	-157.8
Ch4	-160dB	-100.8	-160.8

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/6/10…………….……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/-2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………..TTOP48P……………………Serial No ………………………………
Test Engineer…………………RMC
Date……………………………18/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP48P
Driver board ID	D0902747_V9
Driver board Drawing No/Issue No	TTOP48P
Driver board Serial Number	TTOP48P
Monitor board ID	MON109
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON109

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/7/10…………………

Drive Card ID……T_TOP49P…..…
Monitor Card ID…Mon110…………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

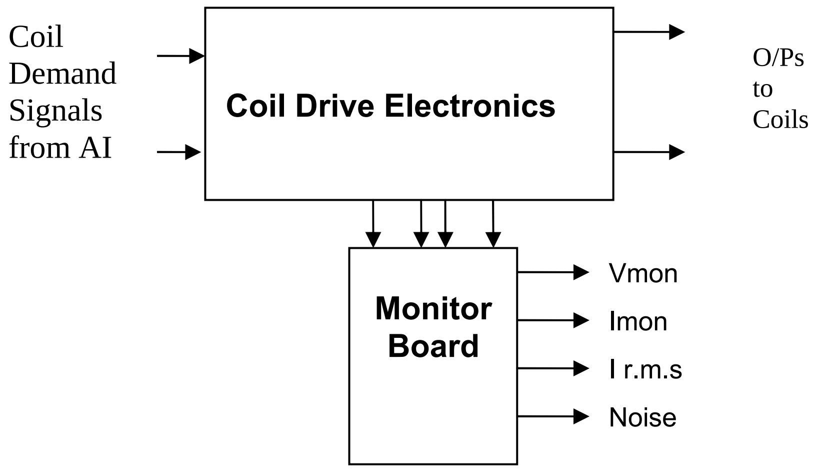


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/7/10………………..……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..14/7/10………………..……

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH3.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit……………..T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..14/7/10……………..……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..14/7/10………………..……

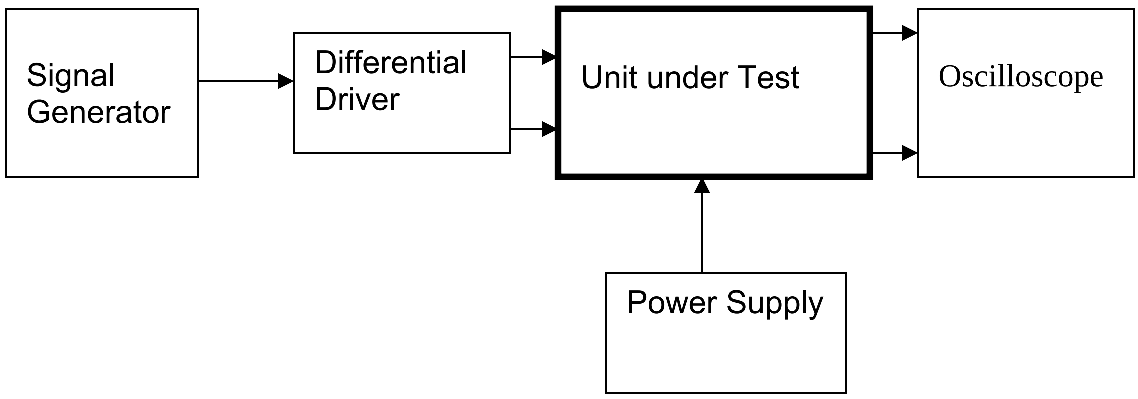
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)
Pd In from Sat pin 9, 10 = +16.5v or DC in A1
Pd In from Sat pin 11, 12 = -16.5 or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..14/7/10………………..……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..14/7/10………………..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..14/7/10…………….……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.749	√
	Pin 1	RMS Current	0.75v dc	0.746	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.750	√
	Pin 4	RMS Current	0.75v dc	0.751	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.750	√
	Pin 7	RMS Current	0.75v dc	0.752	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.749	√
	Pin 10	RMS Current	0.75v dc	0.751	√

Unit……………..T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..14/7/10………………..……

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.33	2.9μV√Hz	√
2		1.04	2.9μV√Hz	√
3		0.95	2.9μV√Hz	√
4		1.04	2.9μV√Hz	√

Unit……………..T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..14/7/10………………..…

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.5		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit……………..T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen…………………………
Date……………..14/7/10……………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

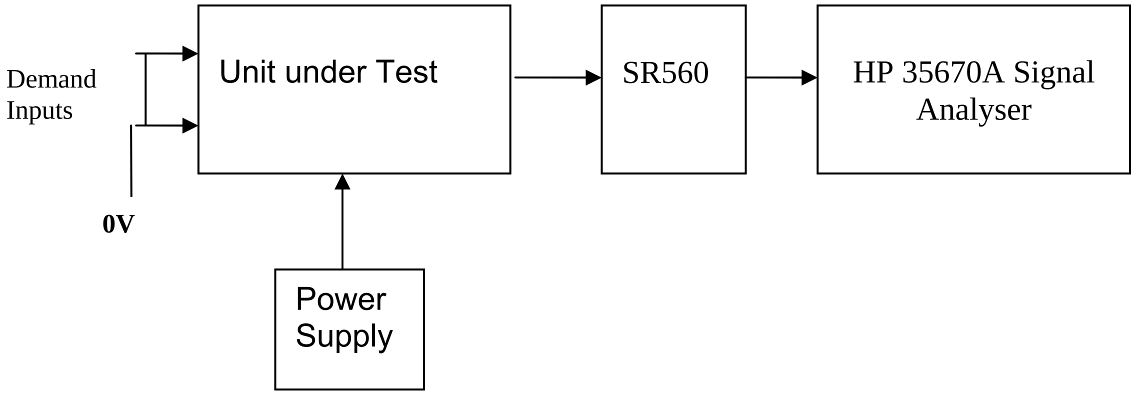
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	37.2	√
CH1 Negative		CH1 IC5	40.6	√
CH2 Positive	12.20	CH2 IC1	40.1	√
CH2 Negative		CH2 IC5	40.6	√
CH3 Positive	12.20	CH3 IC1	40.6	√
CH3 Negative		CH3 IC5	42.6	√
CH4 Positive	12.20	CH4 IC1	40.4	√
CH4 Negative		CH4 IC5	41.6	√

Unit……………..T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..15/7/10………………..……

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.1	-160.1
Ch2	-160dB	-98.5	-158.5
Ch3	-160dB	-101.0	-161.0
Ch4	-160dB	-102.3	-162.3

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit………………T_TOP_P49……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..14/7/10………………..……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/-2.5mA	Pass?
1	39.3	3.27	83.2mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………..TTOP49P……………………Serial No ………………………………
Test Engineer…………………RMC
Date……………………………18/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP49P
Driver board ID	TTOP49P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP49P
Monitor board ID	MON110
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON110

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

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LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P50……………………Serial No ………………………………
Test Engineer…..Xen………..……………
Date……………..14/7/10……………..……

Drive Card ID……T_TOP50P…..……
Monitor Card ID…Mon111……………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

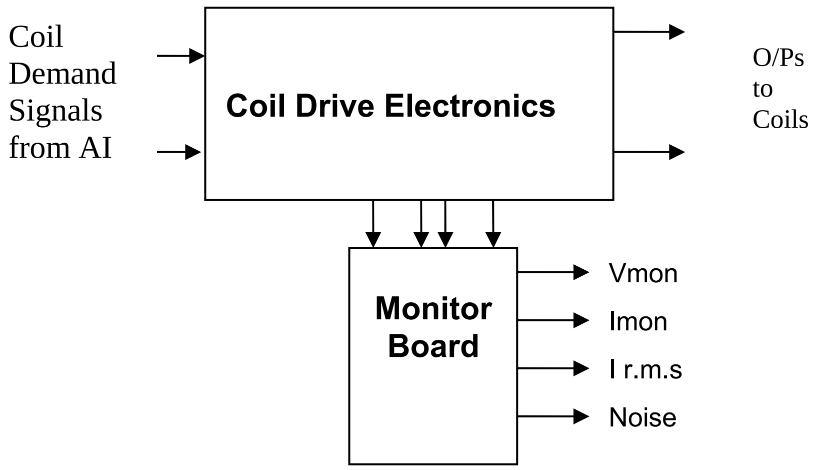

FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P50……………………Serial No ………………………………
Test Engineer…..Xen………..……………
Date……………..14/7/10………………..……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P50……………………Serial No ………………………………
Test Engineer…..Xen………..……………
Date……………..13/7/10………………..……

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected.

Unit……………..T_TOP_P50……………………Serial No ………………………………
Test Engineer…..Xen………..……………
Date……………..13/7/10………………..……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P50……………………Serial No ………………………………
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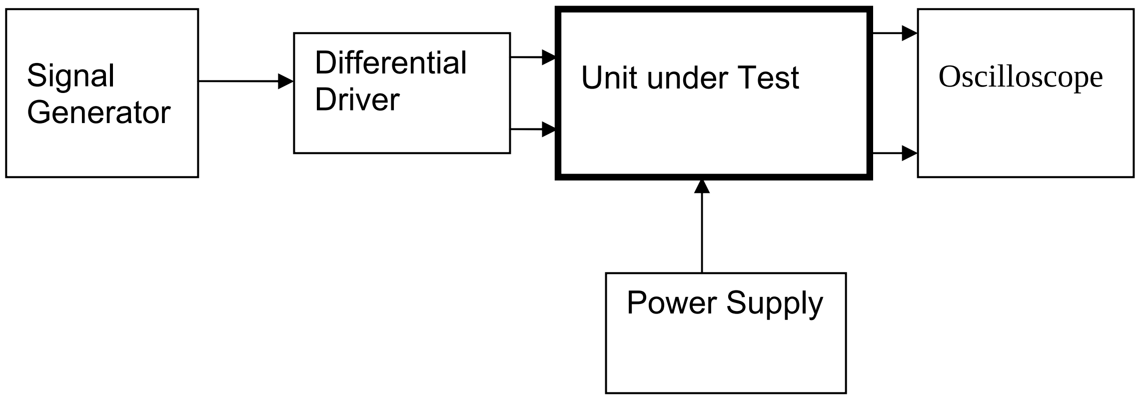
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit…………….…T_TOP_P50……………………Serial No ………………………………
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6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P50……………………Serial No ………………………………
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P50……………………Serial No ………………………………
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8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.729	√
	Pin 1	RMS Current	0.75v dc	0.735	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.729	√
	Pin 4	RMS Current	0.75v dc	0.730	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.729	√
	Pin 7	RMS Current	0.75v dc	0.737	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.730	√
	Pin 10	RMS Current	0.75v dc	0.731	√

Unit……………..T_TOP_P50……………………Serial No ………………………………
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9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.14	2.9μV√Hz	√
2		1.31	2.9μV√Hz	√
3		1.36	2.9μV√Hz	√
4		1.72	2.9μV√Hz	√

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10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

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11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	**CH1 IC1**	41.1	√
CH1 Negative		**CH1 IC5**	41.6	√
CH2 Positive	12.20	**CH2 IC1**	42.8	√
CH2 Negative		**CH2 IC5**	43.6	√
CH3 Positive	12.20	**CH3 IC1**	43.6	√
CH3 Negative		**CH3 IC5**	43.8	√
CH4 Positive	12.20	**CH4 IC1**	40.9	√
CH4 Negative		**CH4 IC5**	41.8	√

Unit…………… T_TOP_P50…………………. Serial No ……………………………
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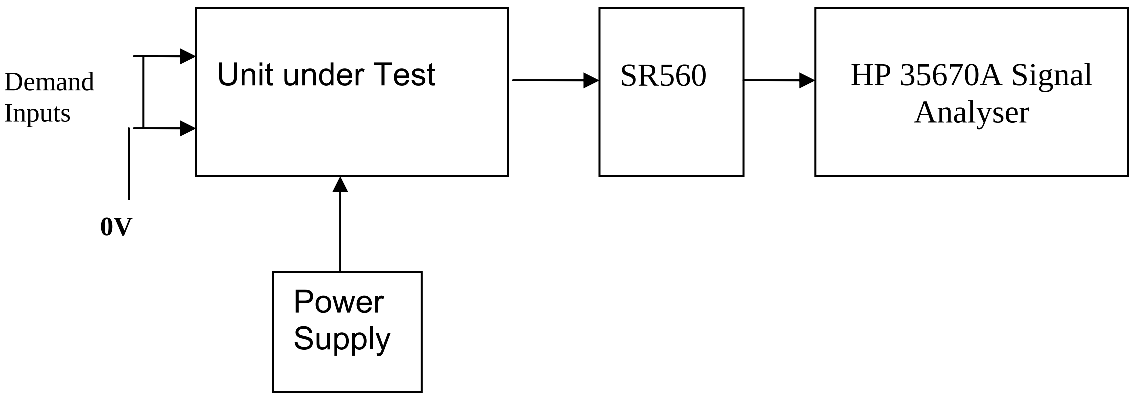
13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.3	-160.3
Ch2	-160dB	-100.8	-160.8
Ch3	-160dB	-100.8	-160.8
Ch4	-160dB	-100.2	-160.2

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P50……………………Serial No ………………………………
Test Engineer…..Xen………..…………..
Date……………..14/7/10………………..……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/-2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.25	82.5mA	120mA	84.8mA	√

Unit.....................TTOP50P.....................Serial No ....
Test Engineer.....................RMC
Date................................19/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP50P
Driver board ID	TTOP50P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP50P
Monitor board ID	MON111
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON111

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..13/7/10…………….……

Drive Card ID……T_TOP51P..………
Monitor Card ID…Mon112……………

Contents

1. Description

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It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

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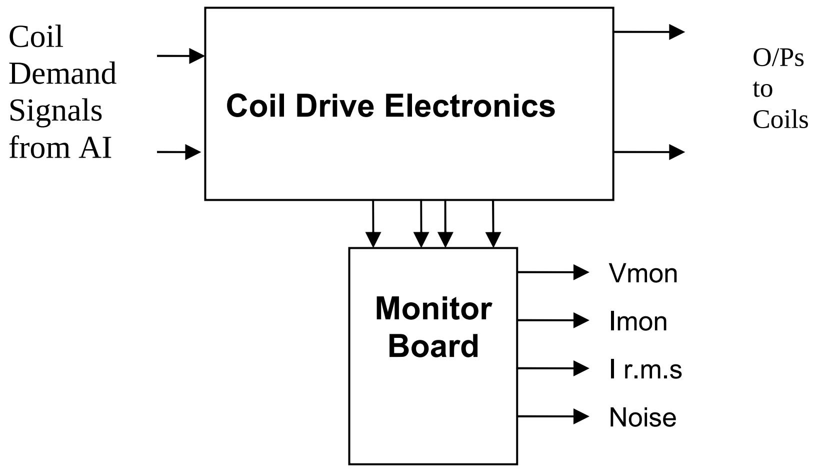

FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..13/7/10………………..……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10………………..……

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 3 & 4.

The four 0.39uF filter capacitors C200 were added, and checked for short circuits and open circuit resistor joints. Visually inspected.

Unit………………T_TOP_P51……………………Serial No ………………………………
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4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10………………..……

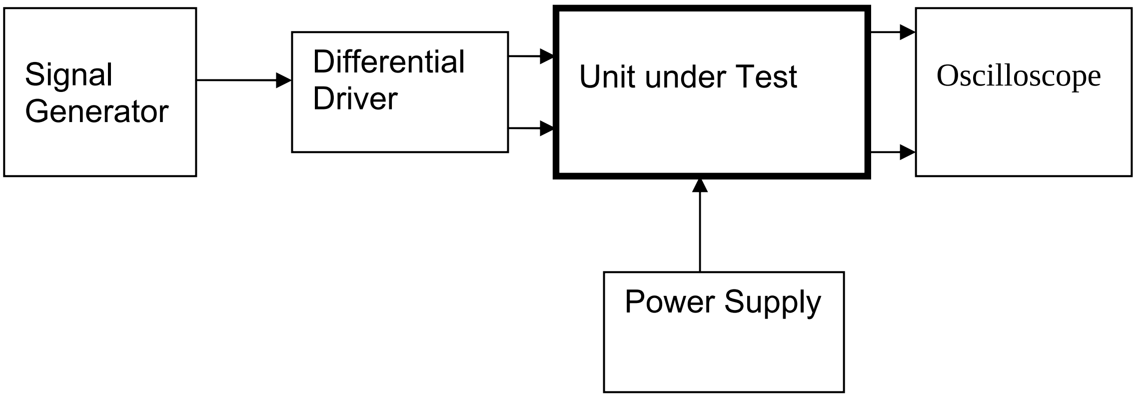
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10………………..……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	**- 16.5 supply current (mA)**
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	**Plus**	**Minus**
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10………………..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10………………..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	**Monitor Connector**	**Parameter**	**Theoretical Value (+/- .1v)**	**Measured Value**	**Pass/ Fail**
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.753	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.752	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.756	√

Unit……………….T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10………………..……

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.72	2.9μV√Hz	√
2		1.53	2.9μV√Hz	√
3		1.82	2.9μV√Hz	√
4		1.61	2.9μV√Hz	√

Unit.................T_TOP_P51.......................Serial No ....
Test Engineer.....Xen........................
Date.................13/7/10.......................

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit………………T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..13/7/10……………..……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.17	**CH1 IC1**	37.9	√
CH1 Negative		**CH1 IC5**	40.9	√
CH2 Positive	12.18	**CH2 IC1**	40.6	√
CH2 Negative		**CH2 IC5**	40.6	√
CH3 Positive	12.17	**CH3 IC1**	41.8	√
CH3 Negative		**CH3 IC5**	41.4	√
CH4 Positive	12.18	**CH4 IC1**	40.4	√
CH4 Negative		**CH4 IC5**	40.6	√

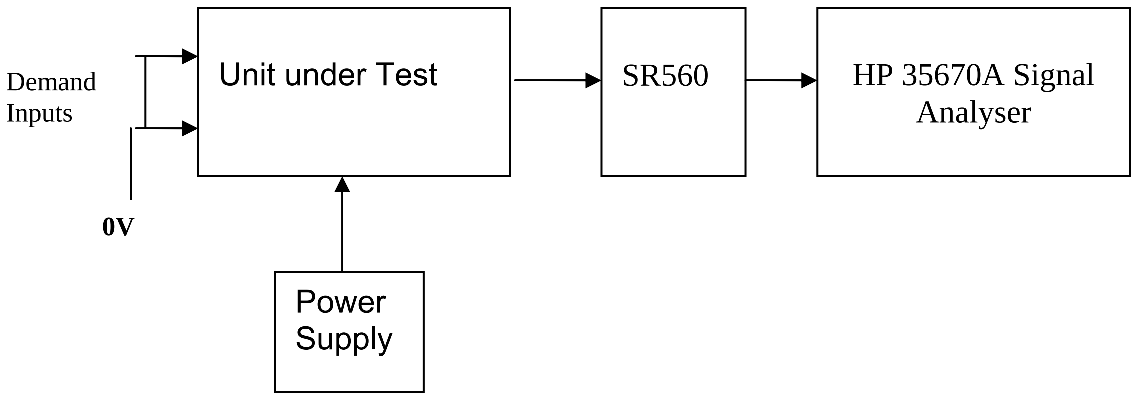
Unit……………..T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..13/7/10………………..……

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.0	-161.0
Ch2	-160dB	-100.5	-160.5
Ch3	-160dB	-100.5	-160.5
Ch4	-160dB	-101.6	-161.6

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………….T_TOP_P51……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..13/7/10………………..……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/-2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit.................TTOP51P.......................Serial No ....
Test Engineer.....................RMC
Date................................19.6/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP51P
Driver board ID	TTOP51P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP51P
Monitor board ID	MON112
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON112

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10……………..……

Drive Card ID……T_TOP52P...………………
Monitor Card ID…Mon113……………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

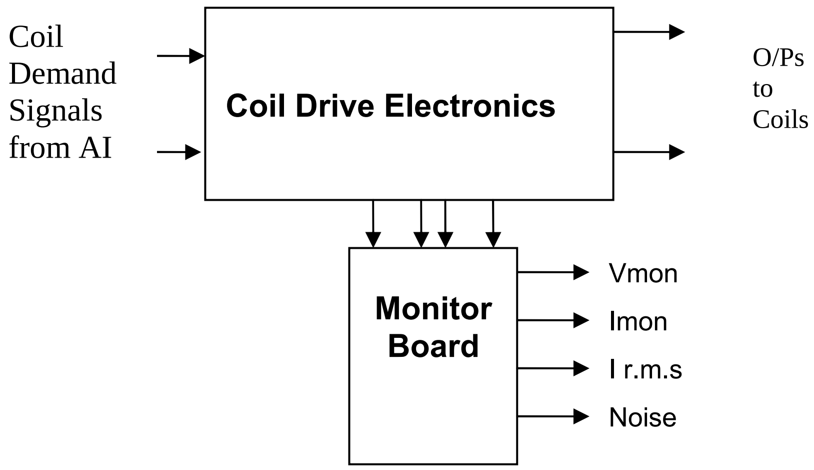


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10………………..……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10…………….……

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 3 & 4.

The four 0.39uF filter capacitors C200 were added, and checked for short circuits and open circuit resistor joints. Visually inspected.

Unit………………T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10………………..……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10……………..……

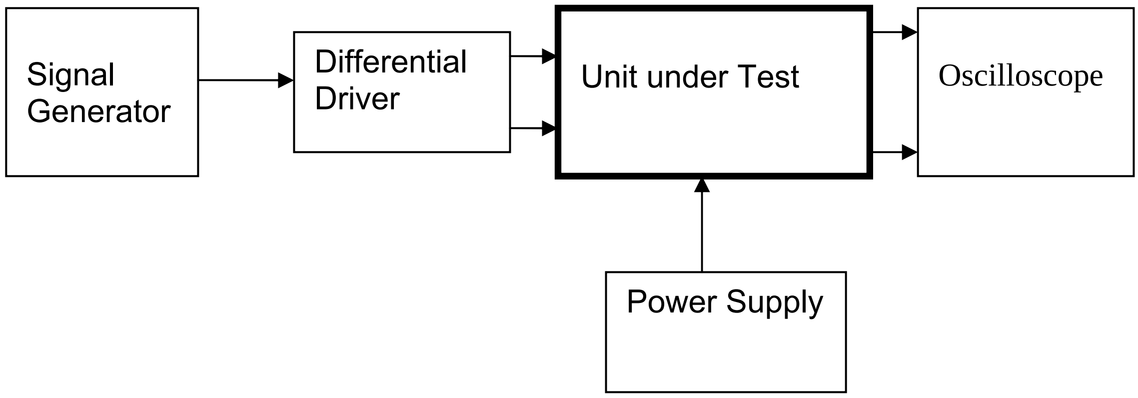
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10………………..……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P52…………………….Serial No ……………………………….
Test Engineer…..Xen……………………
Date……………..9/7/10……………..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……………………
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8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.750	√
	Pin 1	RMS Current	0.75v dc	0.749	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.754	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.748	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.754	√

Unit……………..T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10…………….……

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.25	2.9μV√Hz	√
2		1.20	2.9μV√Hz	√
3		1.32	2.9μV√Hz	√
4		1.46	2.9μV√Hz	√

Unit.................T_TOP_P52.......................Serial No ....
Test Engineer.....Xen.......................
Date................9/7/10.....................

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.6		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit……………..T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10………………..……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

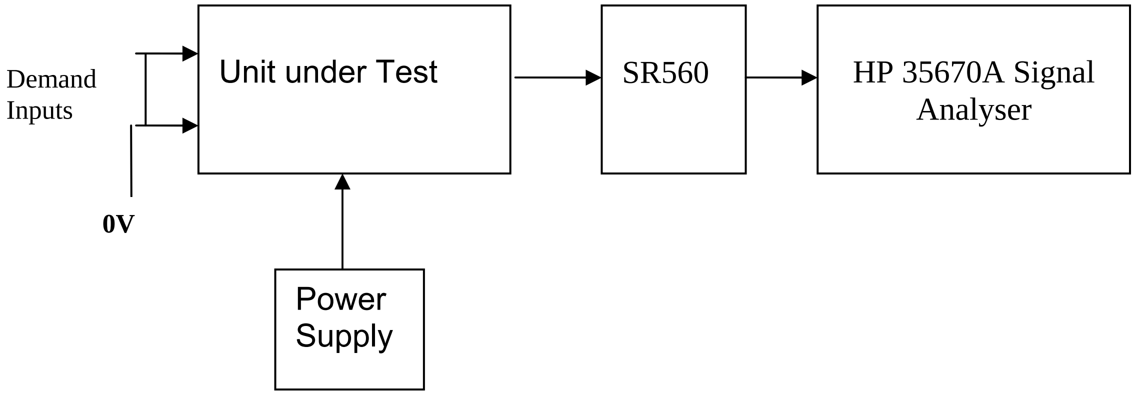
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	39.7	√
CH1 Negative		CH1 IC5	41.6	√
CH2 Positive	12.20	CH2 IC1	41.4	√
CH2 Negative		CH2 IC5	40.6	√
CH3 Positive	12.20	CH3 IC1	40.1	√
CH3 Negative		CH3 IC5	41.4	√
CH4 Positive	12.20	CH4 IC1	40.9	√
CH4 Negative		CH4 IC5	42.3	√

Unit……………….T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10………………..……

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.1	-160.1
Ch2	-160dB	-100.8	-160.8
Ch3	-160dB	-100.7	-160.7
Ch4	-160dB	-100.7	-160.7

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………...T_TOP_P52……………………Serial No ………………………………
Test Engineer…..Xen……..………………
Date……………..12/7/10……………..……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s) +/-2.5mA**	**Pass?**
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit…………………TTOP52P…………………Serial No ………………………………
Test Engineer…………………RMC
Date……………………………19/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP52P
Driver board ID	TTOP52P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP52P
Monitor board ID	MON113
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON113

10. Check the security of any modification wires. √

11. Visually inspect.√

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10…………….……

Drive Card ID……T_TOP53P…..…………………
Monitor Card ID…Mon114…..…..…………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

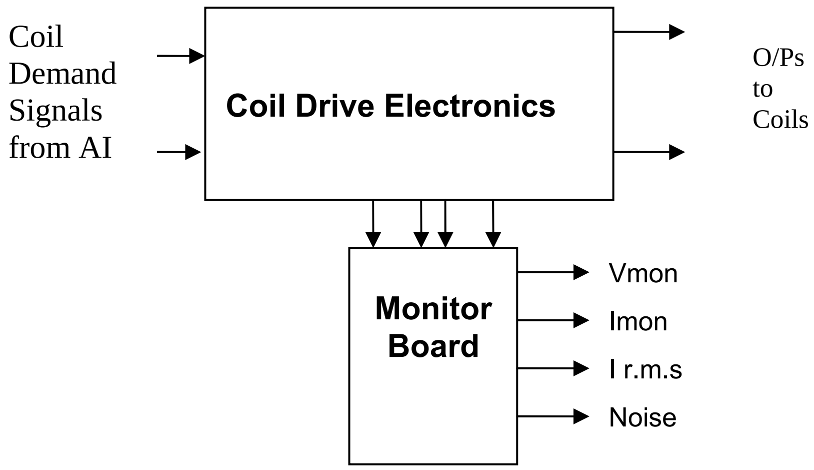


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10………………..….

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10……………..……

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH1.

Four 0.39uF filter capacitors C200 added, and checked for short circuits and open circuit resistor joints. Visually inspected.

Unit……………….T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10…………….……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10…………….……

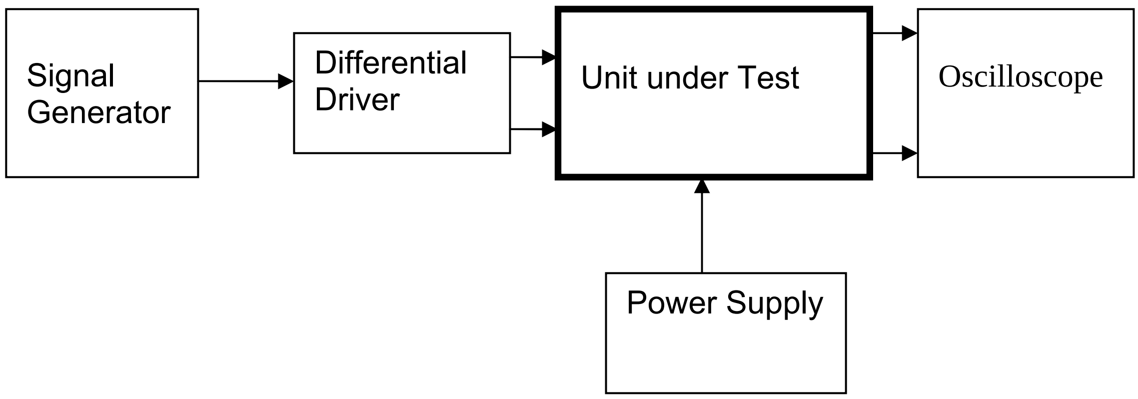
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10………………..……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10………………..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10……………..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.753	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.756	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.761	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.753	√
	Pin 10	RMS Current	0.75v dc	0.754	√

Unit……………..T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10…………….……

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.09	2.9μV√Hz	√
2		1.07	2.9μV√Hz	√
3		0.88	2.9μV√Hz	√
4		1.64	2.9μV√Hz	√

Unit……………..T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10……………..……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit……………..T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10………………..…

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

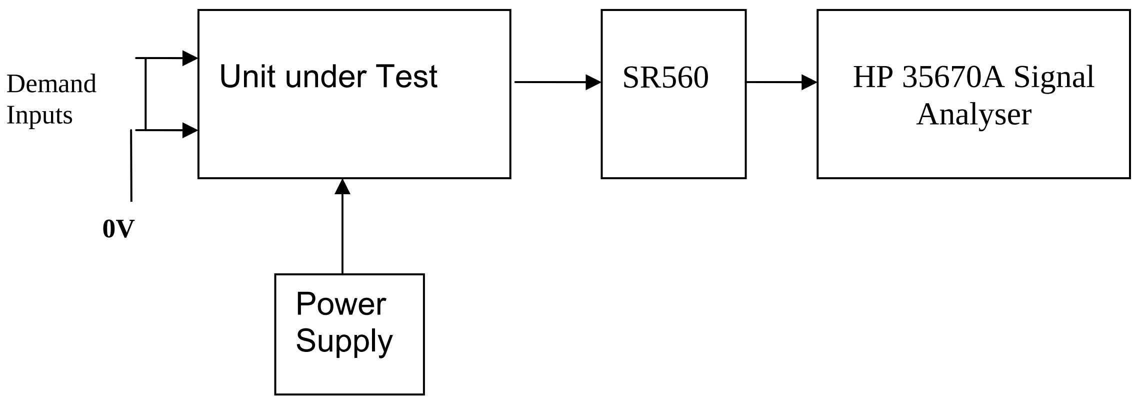
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	40.1	√
CH1 Negative		CH1 IC5	40.4	√
CH2 Positive	12.20	CH2 IC1	42.6	√
CH2 Negative		CH2 IC5	41.1	√
CH3 Positive	12.20	CH3 IC1	42.6	√
CH3 Negative		CH3 IC5	41.6	√
CH4 Positive	12.20	CH4 IC1	42.6	√
CH4 Negative		CH4 IC5	42.3	√

Unit……………..T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10…………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.1	-161.1
Ch2	-160dB	-101.0	-161.0
Ch3	-160dB	-100.2	-160.2
Ch4	-160dB	-101.8	-161.8

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P53……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..9/7/10………………..…

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s) +/-2.5mA**	**Pass?**
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit.................TTOP53P.......................Serial No ....
Test Engineer....................RMC
Date...............................19/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP53P
Driver board ID	TTOP53P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP53P
Monitor board ID	MON114
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON114

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx Advanced LIGO UK 11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10……………..……

Drive Card ID……T_TOP54P…..…………………
Monitor Card ID…Mon115…..….…..…………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

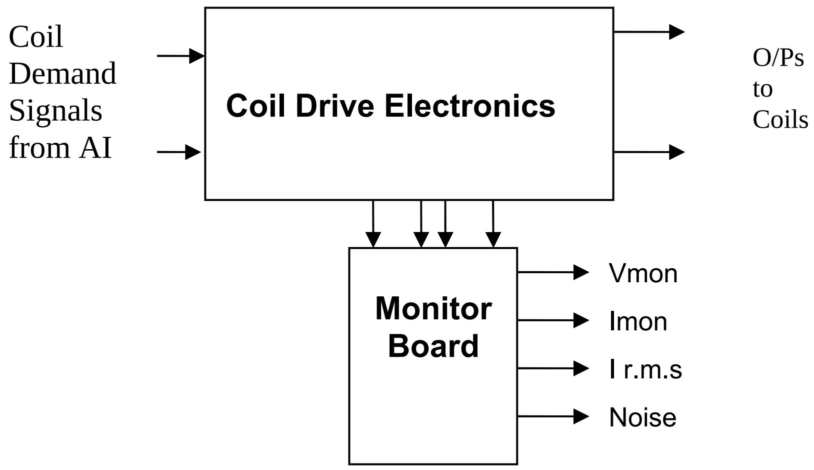


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10……………..……

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10………………..……

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 1 & 2.

Four 0.39uF filter capacitors C200 added, and checked for short circuits and open circuit resistor joints. Visually inspected.

Unit……………..T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10…………….……

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10…………….……

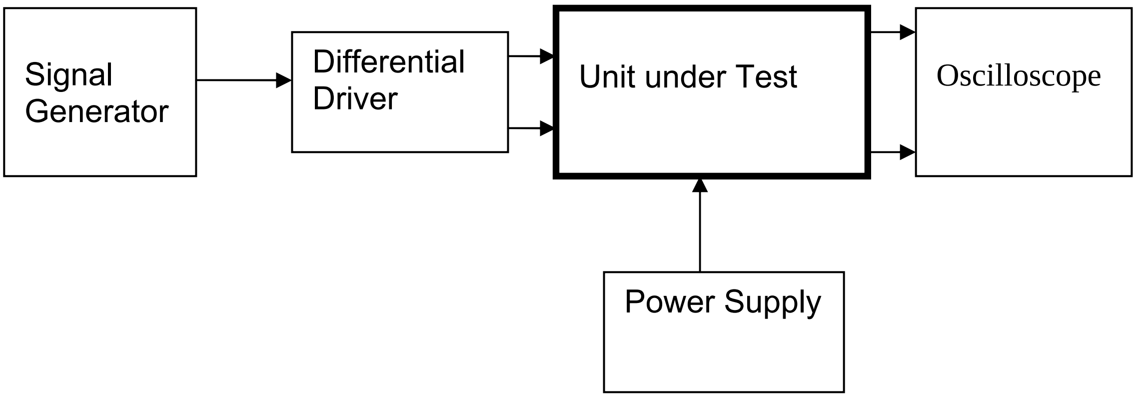
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10…………….……

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P54……………………Serial No ……………………………….
Test Engineer…..Xen……………………
Date……………..8/7/10……………..……

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10………………..……

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.756	√
	Pin 1	RMS Current	0.75v dc	0.762	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.755	√
	Pin 4	RMS Current	0.75v dc	0.760	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.754	√
	Pin 7	RMS Current	0.75v dc	0.757	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.754	√
	Pin 10	RMS Current	0.75v dc	0.759	√

Unit……………..T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10…………….……

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.68	2.9μV√Hz	√
2		1.06	2.9μV√Hz	√
3		0.91	2.9μV√Hz	√
4		0.94	2.9μV√Hz	√

Unit……………..T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10…………….……

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10…………….……

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

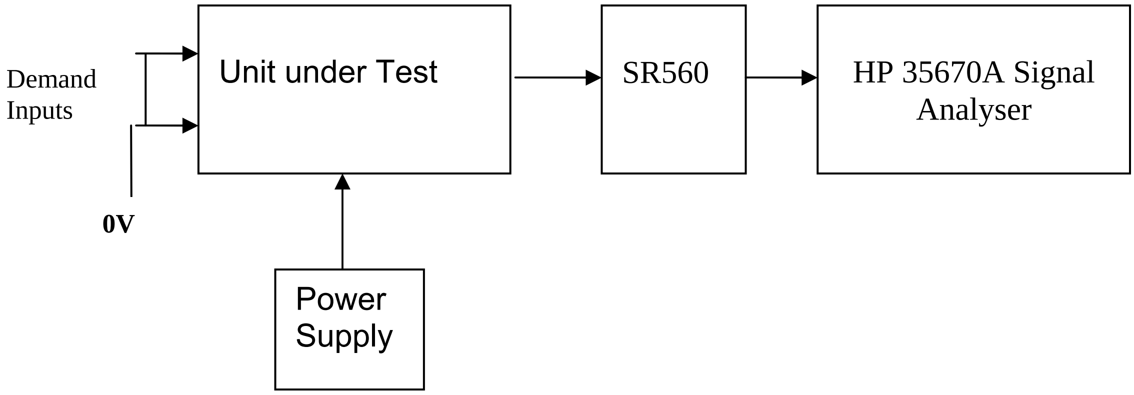
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	**CH1 IC1**	45.3	√
CH1 Negative		**CH1 IC5**	45.5	√
CH2 Positive	12.20	**CH2 IC1**	44.0	√
CH2 Negative		**CH2 IC5**	42.1	√
CH3 Positive	12.19	**CH3 IC1**	42.8	√
CH3 Negative		**CH3 IC5**	45.0	√
CH4 Positive	12.20	**CH4 IC1**	43.3	√
CH4 Negative		**CH4 IC5**	42.3	√

Unit……………..T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10…………….……

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.5	-160.5
Ch2	-160dB	-100.6	-160.6
Ch3	-160dB	-99.8	-159.8
Ch4	-160dB	-100.3	-160.3

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P54……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..8/7/10……………..……

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/-2.5mA	Pass?
1	39.3	3.25	82.7mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.25	82.5mA	120mA	84.8mA	√

Unit...............TTOP54P...........................Serial No ....
Test Engineer.....................RMC
Date................................19/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.

8. Check that links W4 and W5 are in place.

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	
Driver board ID	
Driver board Drawing No/Issue No	
Driver board Serial Number	
Monitor board ID	
Monitor board Drawing No/Issue No	
Monitor board Serial Number	

10. Check the security of any modification wires. √

11. Visually inspect.

12. Put the lid on and fasten all screws,

    Check all external screws for tightness.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P55……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

Drive Card ID……T_TOP55P…………………
Monitor Card ID…Mon116…..…………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

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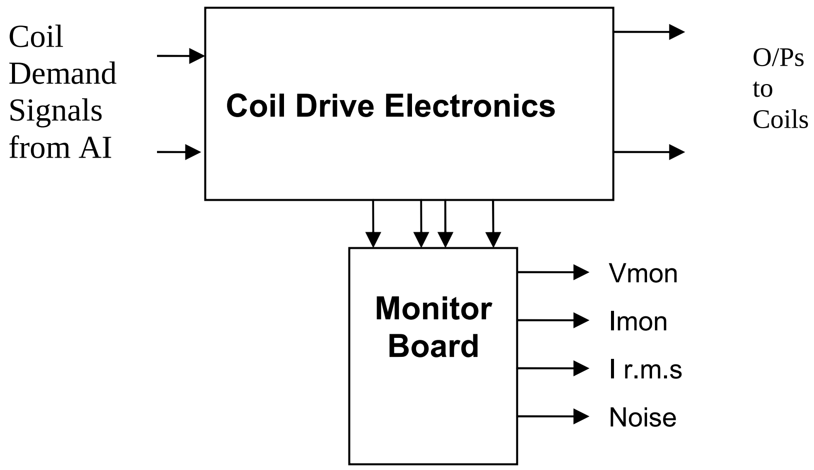


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….T_TOP_P55……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P55……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

3. Inspection

Remove the lid of the case.

Workmanship
Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 3 & 4.

Four 0.39uF filter capacitors C200 added, and checked for short circuits and open circuit resistor joints. Visually inspected.

Unit.................T_TOP_P55.......................Serial No ....
Test Engineer.....Xen....................
Date................8/7/10..................

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………..T_TOP_P55……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

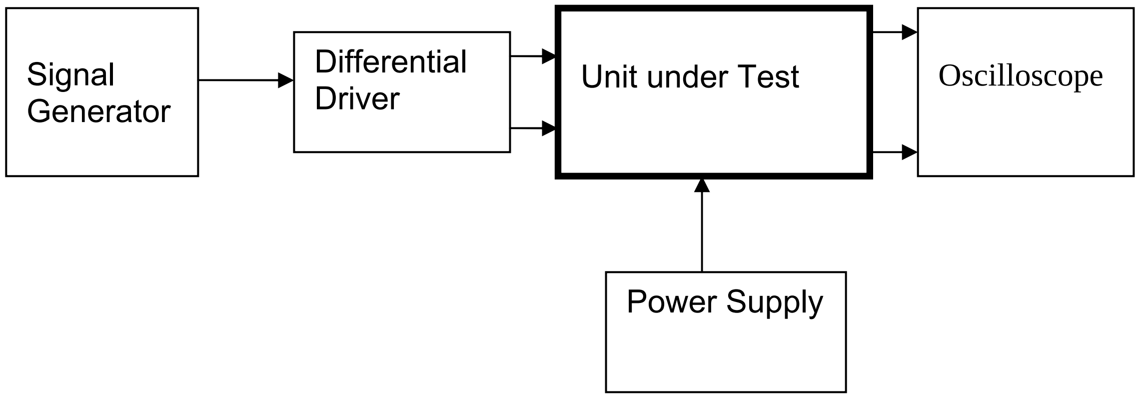
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P55……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P55……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P55……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.750	√
	Pin 1	RMS Current	0.75v dc	0.753	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.755	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.754	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.752	√

Unit………………T_TOP_P55……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors
- Monitor coil inputs to board were grounded for all channels.
Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.02	2.9μV√Hz	√
2		1.02	2.9μV√Hz	√
3		1.46	2.9μV√Hz	√
4		1.09	2.9μV√Hz	√

Unit……………..T_TOP_P55……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit……………….T_TOP_P55…………………….Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

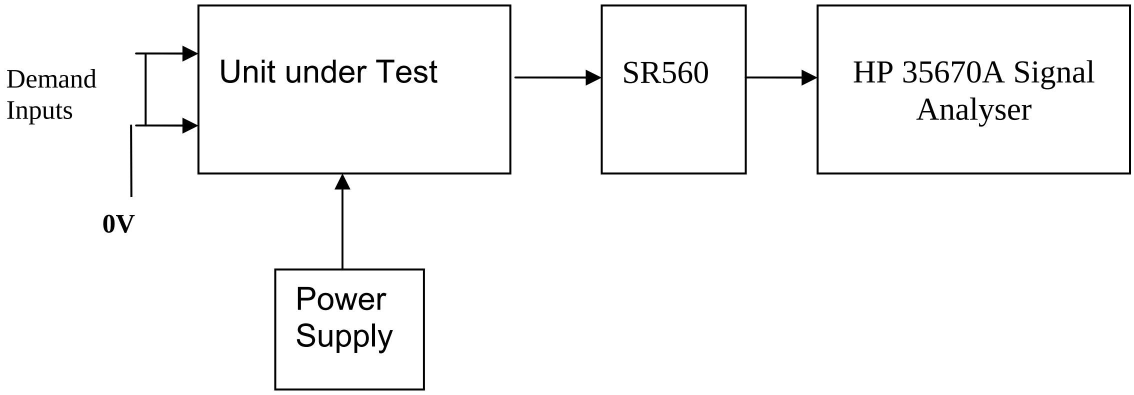
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	**CH1 IC1**	40.4	√
CH1 Negative		**CH1 IC5**	43.3	√
CH2 Positive	12.19	**CH2 IC1**	45.7	√
CH2 Negative		**CH2 IC5**	43.1	√
CH3 Positive	12.20	**CH3 IC1**	42.8	√
CH3 Negative		**CH3 IC5**	43.6	√
CH4 Positive	12.20	**CH4 IC1**	42.1	√
CH4 Negative		**CH4 IC5**	42.6	√

Unit……………..T_TOP_P55…………………..Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-98.1	-158.1
Ch2	-160dB	-98.4	-158.4
Ch3	-160dB	-99.0	-159.0
Ch4	-160dB	-98.3	-158.3

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P55……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/-2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit....................TTOP55P....................Serial No ....
Test Engineer....................RMC
Date................................19/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP55P
Driver board ID	D0902747_V9
Driver board Drawing No/Issue No	TTOP55P
Driver board Serial Number	TTOP55P
Monitor board ID	MON116P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON116P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10..………………

Drive Card ID……T_TOP56P…………………
Monitor Card ID…Mon117…..…………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

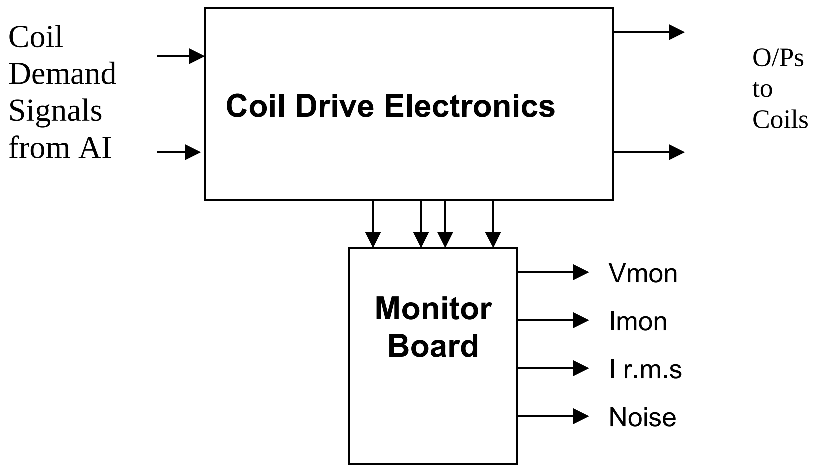


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/7/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/7/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected.

Unit………………T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/7/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/7/10………………

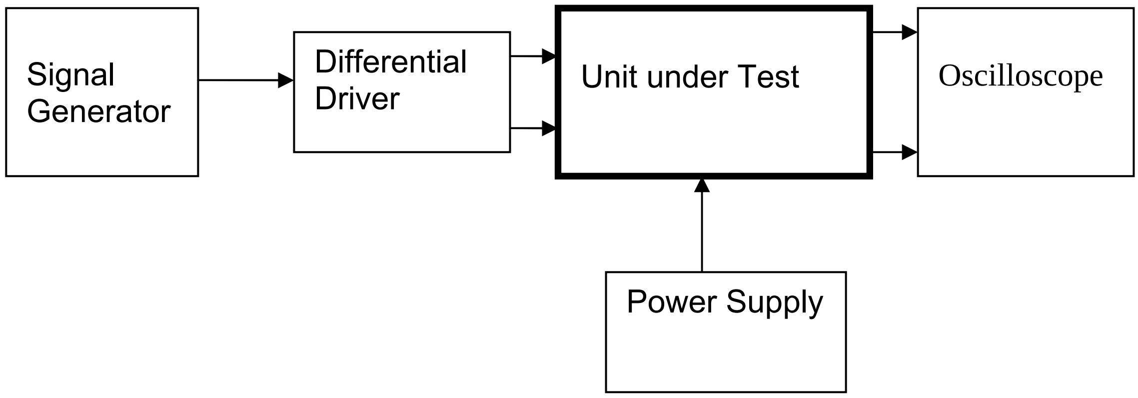
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/7/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/7/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/7/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.758	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.754	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.754	√

Unit……………..T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/7/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.60	2.9μV√Hz	√
2		0.80	2.9μV√Hz	√
3		0.98	2.9μV√Hz	√
4		1.66	2.9μV√Hz	√

Unit……………..T_TOP_P56…………………..Serial No ……………………………
Test Engineer…..Xen…………………
Date……………..7/7/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.81		
Ch2	4.81		
Ch3	4.81		
Ch4	4.81		

Unit………………T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/7/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	CH1 IC1	42.3	√
CH1 Negative		CH1 IC5	44.5	√
CH2 Positive	12.19	CH2 IC1	44.0	√
CH2 Negative		CH2 IC5	46.2	√
CH3 Positive	12.19	CH3 IC1	43.6	√
CH3 Negative		CH3 IC5	44.5	√
CH4 Positive	12.19	CH4 IC1	43.8	√
CH4 Negative		CH4 IC5	43.3	√

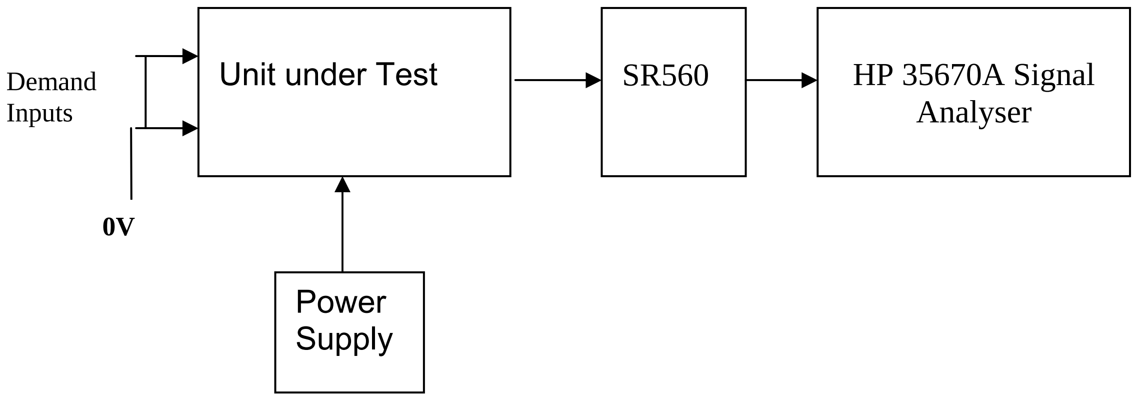
Unit……………..T_TOP_P56……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/7/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-98.9	-158.9
Ch2	-160dB	-99.1	-159.1
Ch3	-160dB	-101.1	-161.1
Ch4	-160dB	-101.5	-161.5

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P56……………………Serial No ……………………………….
Test Engineer…..Xen…………………
Date……………..7/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.25	82.5mA	120mA	84.8mA	√

Unit..................TTOP56P........................Serial No ....
Test Engineer.....................RMC
Date................................19/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP56P
Driver board ID	D0902747_V9
Driver board Drawing No/Issue No	TTOP56P
Driver board Serial Number	TTOP56P
Monitor board ID	MON117
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON117

10. Check the security of any modification wires.

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P57……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….7/7/10..…………

Drive Card ID……T_TOP57P…………
Monitor Card ID...Mon118……………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

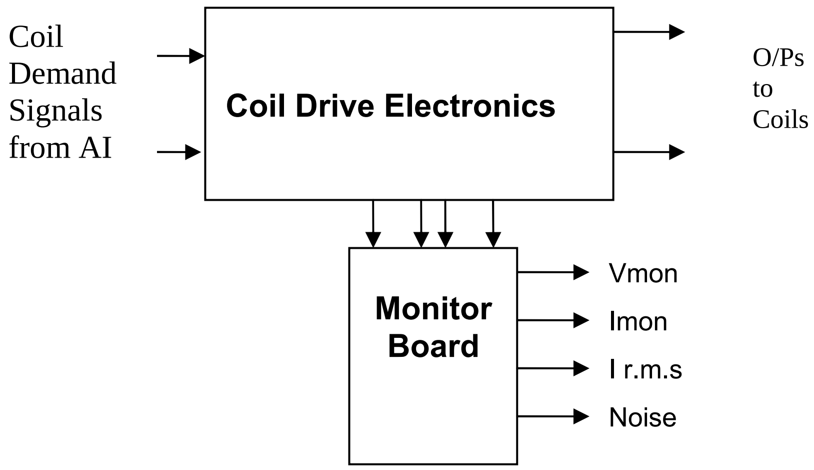


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….T_TOP_P57……………………Serial No ………………………………
Test Engineer ….Xen……..………
Date …………….7/7/10..…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P57……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date …………….27/1/10…………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected.

Unit..................T_TOP_P57........................Serial No ....
Test Engineer ....Xen................
Date ....27/1/10............

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P57……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….27/1/10…………

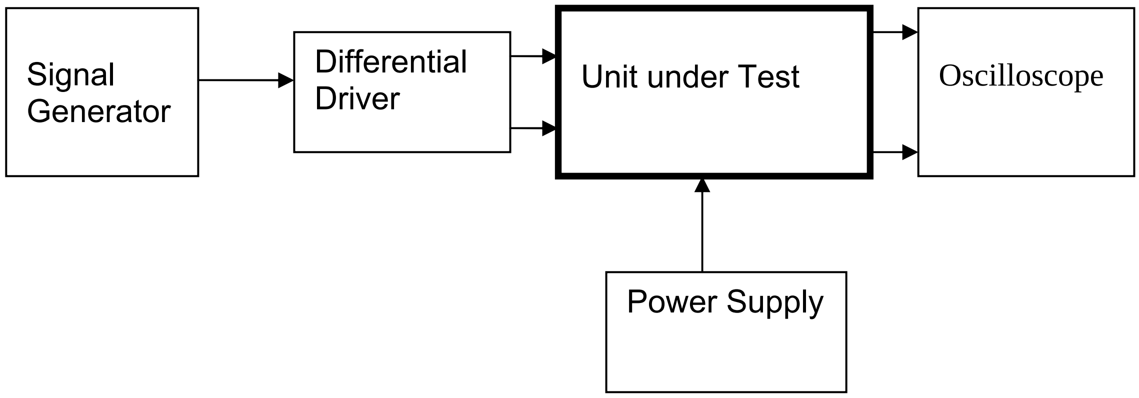
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit..................T_TOP_P57........................Serial No ....
Test Engineer ....Xen................
Date ....27/1/10............

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit..................T_TOP_P57........................Serial No ....
Test Engineer ....Xen.................
Date ....27/1/10............

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P57……………………Serial No ……………………………
Test Engineer ….Xen………..……
Date ……………27/1/10…………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to DC.

1v across load resistor

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.757	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit………………T_TOP_P57……………………Serial No ………………………………
Test Engineer ….Xen………………
Date …………….27/1/10…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.02	2.9μV√Hz	√
2		1.13	2.9μV√Hz	√
3		1.56	2.9μV√Hz	√
4		1.01	2.9μV√Hz	√

Unit……………..T_TOP_P57……………………Serial No ………………………………
Test Engineer ….Xen…….………
Date …………….27/1/10…………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct. Ensure that links W4 and W5 are present.

Use the dynamic signal analyser and the signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output (V)	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………T_TOP_P57……………………Serial No ………………………………
Test Engineer ….Xen…………….
Date …………….27/1/10…………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	38.2	√
CH1 Negative		CH1 IC5	40.1	√
CH2 Positive	12.21	CH2 IC1	39.2	√
CH2 Negative		CH2 IC5	40.4	√
CH3 Positive	12.20	CH3 IC1	37.5	√
CH3 Negative		CH3 IC5	39.9	√
CH4 Positive	12.21	CH4 IC1	39.4	√
CH4 Negative		CH4 IC5	37.5	√

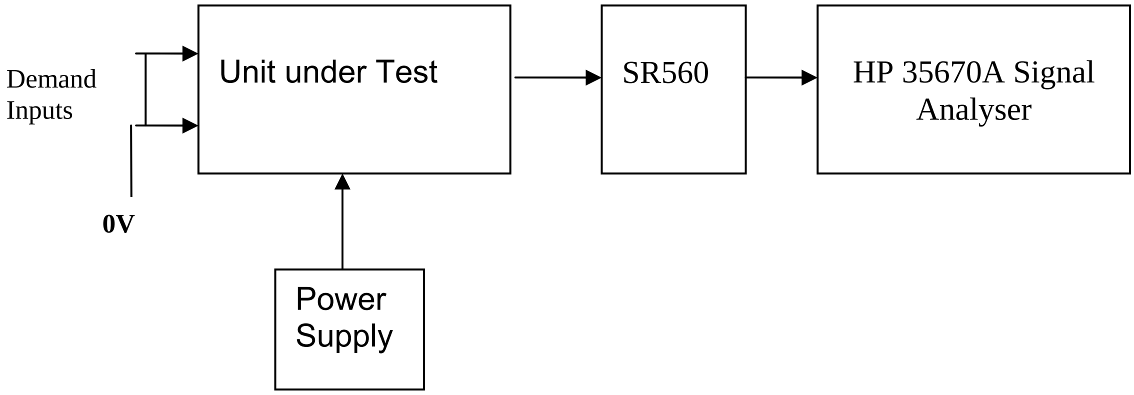
Unit.................T_TOP_P57.......................Serial No ....
Test Engineer ....Xen................
Date ....7/7/10..............

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.4	-161.4
Ch2	-160dB	-101.5	-161.5
Ch3	-160dB	-101.4	-161.4
Ch4	-160dB	-99.5	-159.5

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P57……………………Serial No ………………………………
Test Engineer ….Xen……..……..
Date …………….7/7/10..…………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………………TTOP57P………………Serial No ………………………………
Test Engineer ………RMC
Date …………………19/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP57P
Driver board ID	TTOP57P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP57P
Monitor board ID	MON118P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON118P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws √,

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..21/7/10………………

Drive Card ID……T_TOP58P…………………
Monitor Card ID…Mon69………………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

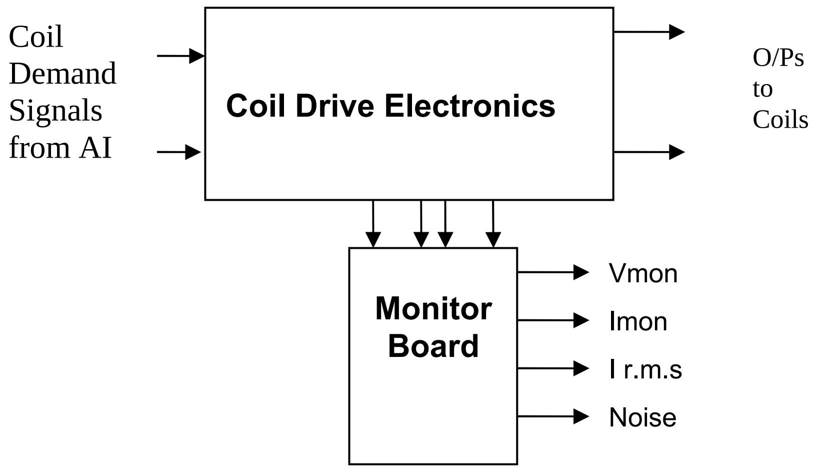


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..21/7/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit………………T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

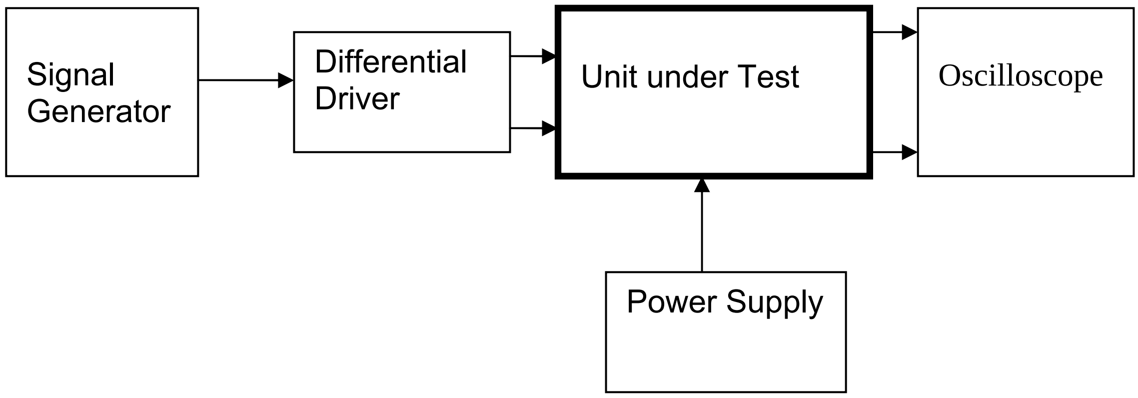
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..18/3/10……………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.756	√
	Pin 1	RMS Current	0.75v dc	0.759	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.756	√
	Pin 4	RMS Current	0.75v dc	0.755	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.754	√
	Pin 7	RMS Current	0.75v dc	0.758	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.754	√
	Pin 10	RMS Current	0.75v dc	0.758	√

Unit……………..T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..18/3/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.55	2.9μV√Hz	√
2		1.35	2.9μV√Hz	√
3		1.62	2.9μV√Hz	√
4		1.60	2.9μV√Hz	√

Unit..................T_TOP_P58........................Serial No ....
Test Engineer.....Xen......................
Date.................18/3/10..................

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit………………T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..18/3/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

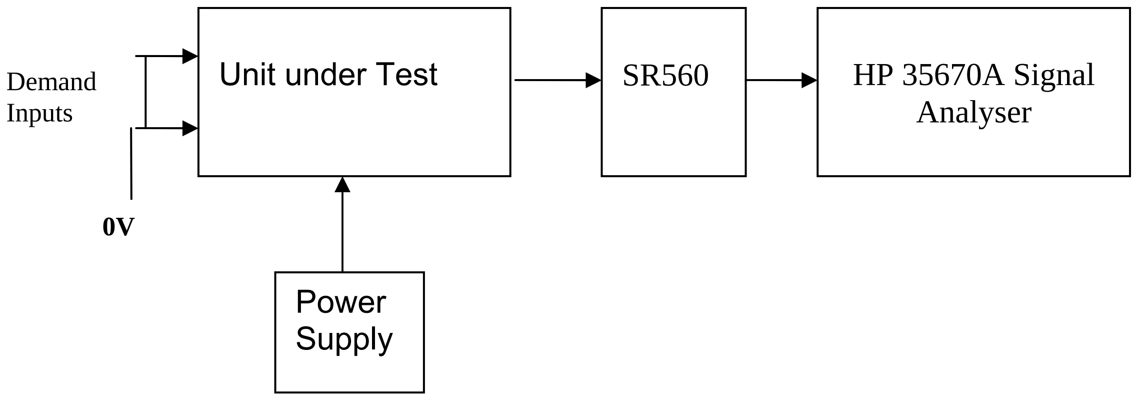
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.21	**CH1 IC1**	38.9	√
CH1 Negative		**CH1 IC5**	43.3	√
CH2 Positive	12.21	**CH2 IC1**	43.8	√
CH2 Negative		**CH2 IC5**	43.6	√
CH3 Positive	12.21	**CH3 IC1**	43.1	√
CH3 Negative		**CH3 IC5**	44.0	√
CH4 Positive	12.21	**CH4 IC1**	42.1	√
CH4 Negative		**CH4 IC5**	42.1	√

Unit……………..T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..20/7/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.2	-159.2
Ch2	-160dB	-99.7	-159.7
Ch3	-160dB	-101.8	-161.8
Ch4	-160dB	-99.7	-159.7

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P58……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..20/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s) +/- 2.5mA**	**Pass?**
1	39.3	3.25	82.7mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.25	82.5mA	120mA	84.8mA	√

Unit……………..TTOP58P……………..Serial No ……………………………
Test Engineer……………..RMC
Date………………………..18/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP58P
Driver board ID	TTOP58P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP58P
Monitor board ID	MON69
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON69

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P59……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..18/3/10……………..

Drive Card ID……T_TOP59P………………..
Monitor Card ID…Mon70……………………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

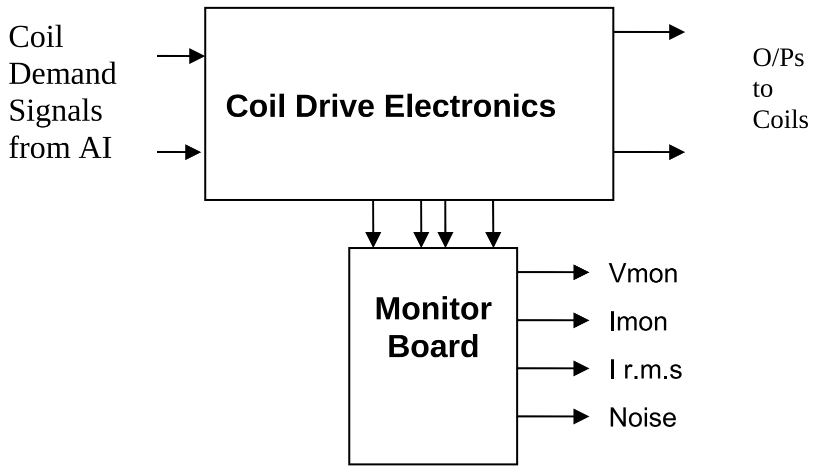


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit.................T_TOP_P59.......................Serial No ....
Test Engineer.....Xen.......................
Date..................18/3/10..................

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P59……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..18/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit……………..T_TOP_P59……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P59……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

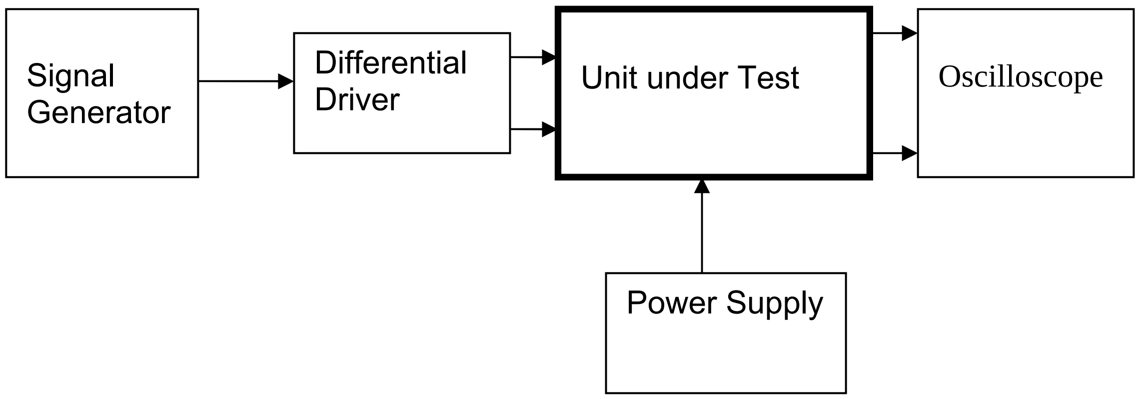
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P59……………………Serial No ……………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit.................T_TOP_P59.......................Serial No ....
Test Engineer.....Xen......................
Date.................18/3/10.................

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P59……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..18/3/10……………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.753	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.753	√
	Pin 4	RMS Current	0.75v dc	0.754	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit……………..T_TOP_P59……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..18/3/10………………

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit………………T_TOP_P59……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..18/3/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit………………T_TOP_P59……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..18/3/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.21	CH1 IC1	41.4	√
CH1 Negative		CH1 IC5	43.8	√
CH2 Positive	12.21	CH2 IC1	43.8	√
CH2 Negative		CH2 IC5	42.1	√
CH3 Positive	12.20	CH3 IC1	43.1	√
CH3 Negative		CH3 IC5	43.3	√
CH4 Positive	12.21	CH4 IC1	42.6	√
CH4 Negative		CH4 IC5	43.1	√

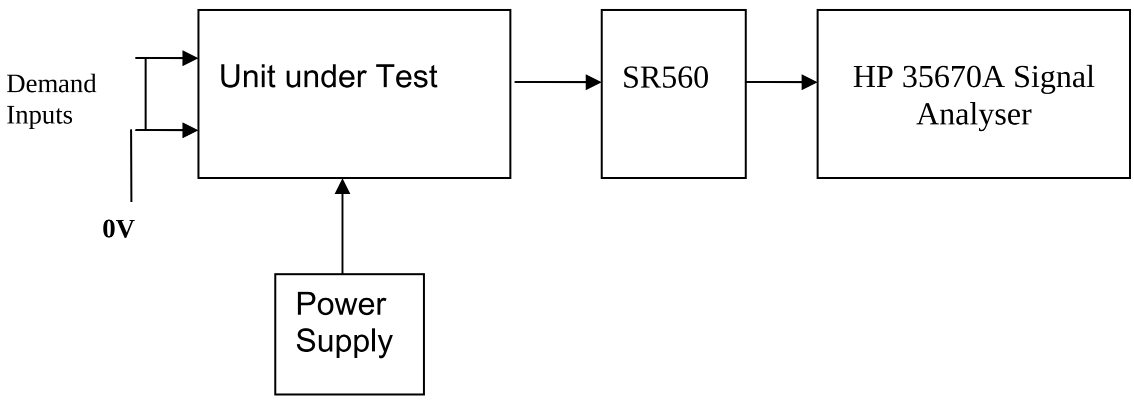
Unit.......................................Serial No ....
Test Engineer....................
Date...............................

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.15	-159.15
Ch2	-160dB	-100.59	-160.59
Ch3	-160dB	-101.36	-161.36
Ch4	-160dB	-100.0	-160.0

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P59……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..18/3/10……………..

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.36	85.5mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.36	85.5mA	120mA	84.8mA	√
4	39.4	3.36	85.3mA	120mA	84.8mA	√

15. Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in µV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	Output	/(Pre-amplifier gain)	Maximum value	Pass/Fail
1	26.3	2.63	2.9	Pass
2	14.1	1.41	2.9	Pass
3	11.4	1.14	2.9	Pass
4	15.9	1.59	2.9	Pass

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

16. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP59P
Driver board ID	TTOP59P
Driver board Drawing No/Issue No	D0902747 V 6
Driver board Serial Number	TTOP59P
Monitor board ID	MON70
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON70

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date …………….10/9/10…………

Drive Card ID……T_TOP60P…………………
Monitor Card ID…Mon164…..…………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

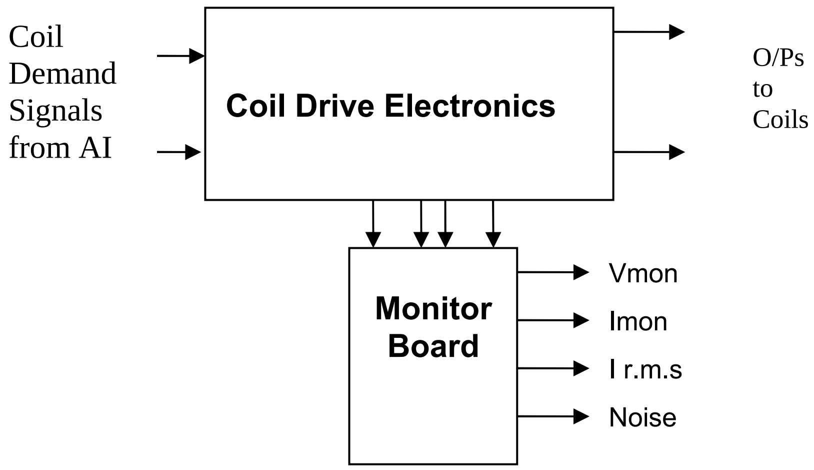


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen…...................
Date …………….10/9/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH1.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit………………T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

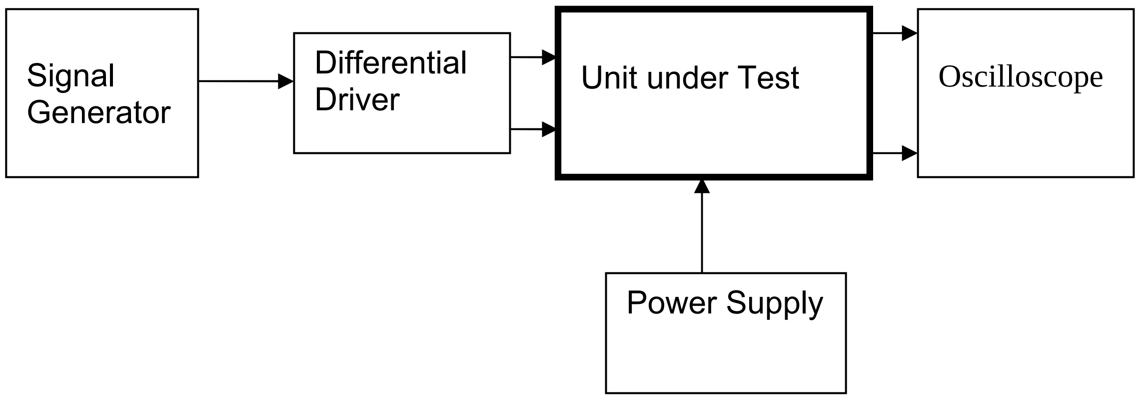
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….T_TOP_P60…………………….Serial No ……………………………….
Test Engineer…..Xen……..…………….
Date……………..18/3/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..18/3/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.751	√
	Pin 1	RMS Current	0.75v dc	0.756	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.752	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.753	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit……………..T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..18/3/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.67	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.39	2.9μV√Hz	√
2		1.28	2.9μV√Hz	√
3		1.25	2.9μV√Hz	√
4		1.33	2.9μV√Hz	√

Unit……………..T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	CH1 IC1	39.7	√
CH1 Negative		CH1 IC5	41.6	√
CH2 Positive	12.19	CH2 IC1	41.6	√
CH2 Negative		CH2 IC5	41.4	√
CH3 Positive	12.19	CH3 IC1	41.1	√
CH3 Negative		CH3 IC5	41.8	√
CH4 Positive	12.19	CH4 IC1	40.1	√
CH4 Negative		CH4 IC5	41.4	√

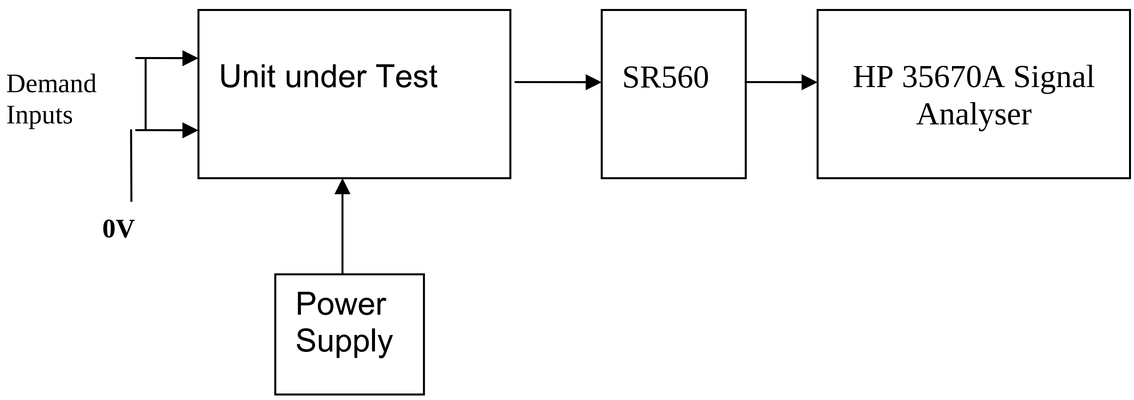
Unit………………T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..28/7/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.7	-161.7
Ch2	-160dB	-98.7	-158.7
Ch3	-160dB	-98.6	-158.6
Ch4	-160dB	-100.5	-160.5

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P60……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..19/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.27	83.2mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.27	83.0mA	120mA	84.8mA	√

Unit..............TTOP60P....................Serial No ....
Test Engineer....................RMC
Date...............................23/8/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP60P
Driver board ID	TTOP60P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP60P
Monitor board ID	MON164
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON164

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P61……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..18/3/10……………..

Drive Card ID……T_TOP61P………………..
Monitor Card ID…Mon165…..………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

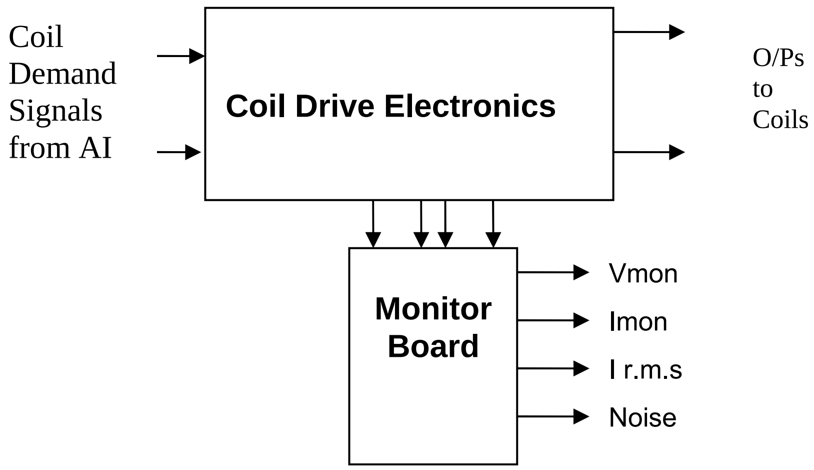


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit..................T_TOP_P61.......................Serial No ....
Test Engineer.....Xen.......................
Date.................18/3/10..................

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………T_TOP_P61……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………T_TOP_P61……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..18/3/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P61……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..18/3/10………………

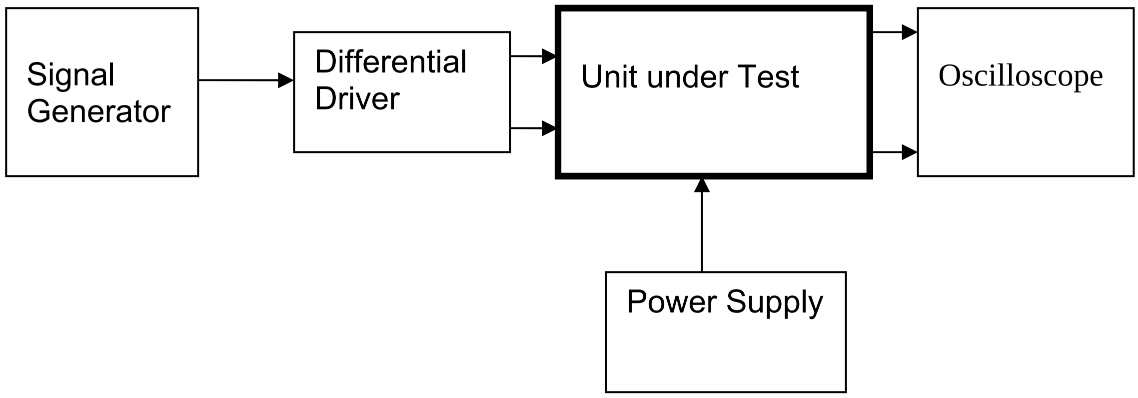
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	**Resistance**	**OK?**
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)
Pd In from Sat pin 9, 10 = +16.5v or DC in A1
Pd In from Sat pin 11, 12 = -16.5 or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v or DC in A2

Coil Drive Outputs
Ch1+ = Coil out to Sat pin 1 Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3 Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5 Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7 Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P61……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..18/3/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	**- 16.5 supply current (mA)**
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	**Plus**	**Minus**
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P61……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P61……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.753	√
	Pin 1	RMS Current	0.75v dc	0.752	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.757	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.754	√
	Pin 7	RMS Current	0.75v dc	0.751	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.754	√

Unit……………..T_TOP_P61……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..18/3/10………………

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit……………..T_TOP_P61……………………Serial No ……………………………
Test Engineer…..Xen…….……………
Date……………..18/3/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.7		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..T_TOP_P61……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..18/3/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

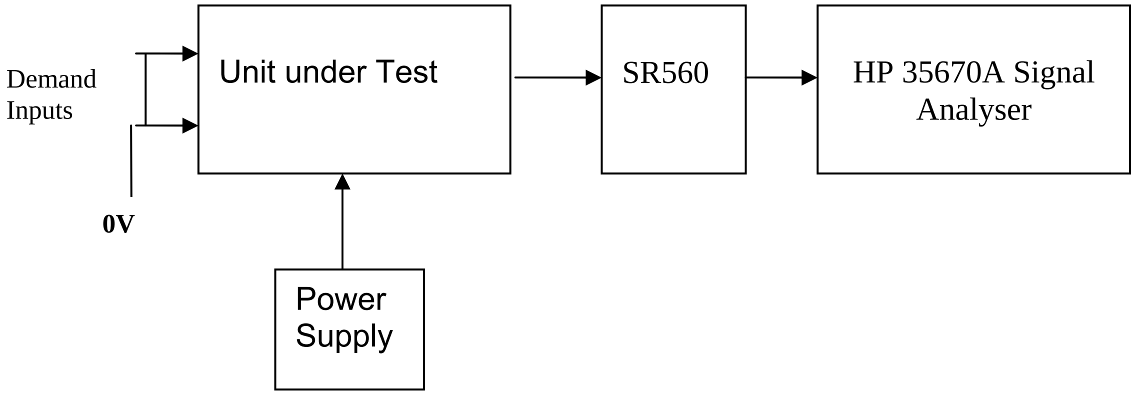
The output voltages should be recorded.

Output	**Voltage**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	12.19	**CH1 IC1**	39.2	√
CH1 Negative		**CH1 IC5**	40.6	√
CH2 Positive	12.19	**CH2 IC1**	38.4	√
CH2 Negative		**CH2 IC5**	40.9	√
CH3 Positive	12.19	**CH3 IC1**	42.8	√
CH3 Negative		**CH3 IC5**	42.1	√
CH4 Positive	12.19	**CH4 IC1**	38.7	√
CH4 Negative		**CH4 IC5**	41.6	√

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.28	-161.28
Ch2	-160dB	-99.46	-159.46
Ch3	-160dB	-101.28	-161.28
Ch4	-160dB	-100.82	-160.82

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P61……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..18/3/10……………..

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.35	85.2mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.35	85.2mA	120mA	84.8mA	√
4	39.4	3.35	85.0mA	120mA	84.8mA	√

15. Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	Output	/(Pre-amplifier gain)	Maximum value	Pass/Fail
1	14.3	1.43	2.9	Pass
2	15.3	1.53	2.9	Pass
3	18.7	1.87	2.9	Pass
4	16.5	1.65	2.9	Pass

Unit...Serial No ....
Test Engineer.....................
Date.................................

16. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP 61P
Driver board ID	TTOP 61P
Driver board Drawing No/Issue No	D0902747 V6
Driver board Serial Number	TTOP 61P
Monitor board ID	MON165
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON165

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P62……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10……………..

Drive Card ID……T_TOP62P…………………
Monitor Card ID…Mon67………………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

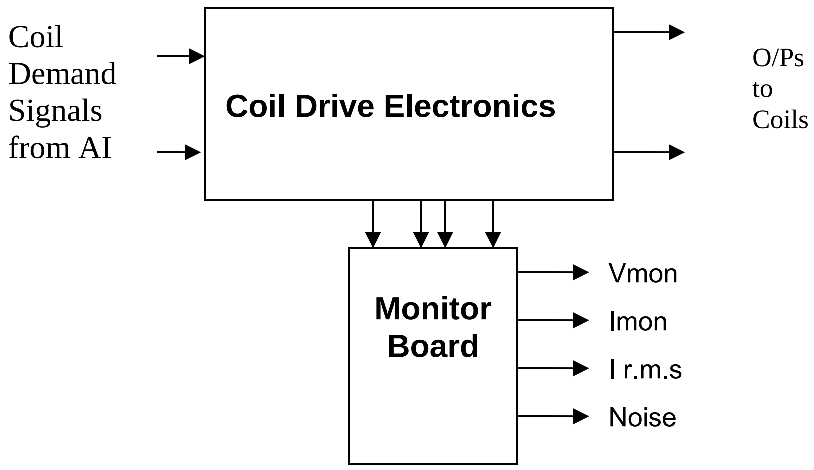


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P62……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………...T_TOP_P62……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit.................T_TOP_P62......................Serial No ....
Test Engineer.....Xen.....................
Date................17/3/10.................

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P62……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..17/3/10………………

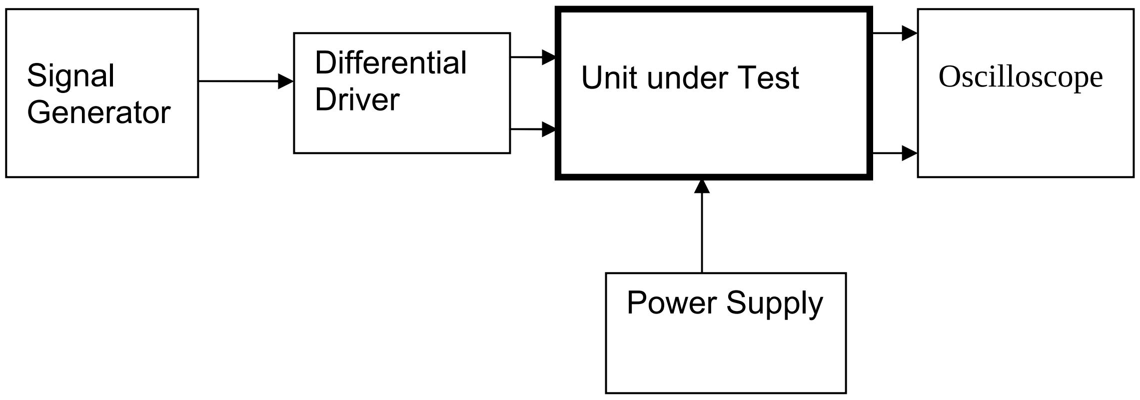
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P62……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..17/3/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit.................T_TOP_P62......................Serial No ....
Test Engineer.....Xen.......................
Date................17/3/10.................

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P62……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..17/3/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	**Monitor Connector**	**Parameter**	**Theoretical Value (+/- .1v)**	**Measured Value**	**Pass/ Fail**
1	Pin 2	Current Monitor	0.75v r.m.s	0.755	√
	Pin 1	RMS Current	0.75v dc	0.757	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.755	√
	Pin 4	RMS Current	0.75v dc	0.754	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.757	√
	Pin 7	RMS Current	0.75v dc	0.759	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.754	√
	Pin 10	RMS Current	0.75v dc	0.757	√

Unit……………..T_TOP_P62……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..17/3/10………………

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Unit…………….…T_TOP_P62……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..17/3/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..T_TOP_P62……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

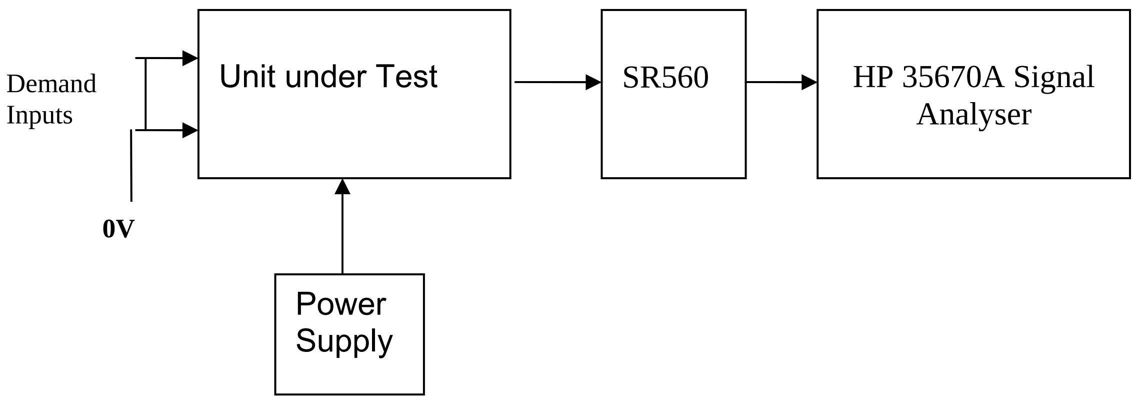
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	**CH1 IC1**	41.8	√
CH1 Negative		**CH1 IC5**	44.5	√
CH2 Positive	12.19	**CH2 IC1**	43.3	√
CH2 Negative		**CH2 IC5**	41.4	√
CH3 Positive	12.19	**CH3 IC1**	43.8	√
CH3 Negative		**CH3 IC5**	42.3	√
CH4 Positive	12.19	**CH4 IC1**	41.4	√
CH4 Negative		**CH4 IC5**	41.6	√

Unit………………………………….Serial No ………………………………
Test Engineer…………………
Date……………………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.6	-160.6
Ch2	-160dB	-99.7	-159.7
Ch3	-160dB	-99.0	-159.0
Ch4	-160dB	-101.6	-161.6

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P62……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..17/3/10……………..

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.34	85.0mA	120mA	84.8mA	√
2	39.4	3.35	85.0mA	120mA	84.8mA	√
3	39.3	3.33	84.7mA	120mA	84.8mA	√
4	39.4	3.34	84.8mA	120mA	84.8mA	√

15. Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	Output	/(Pre-amplifier gain)	Maximum value	Pass/Fail
1	17.2	1.72	2.9	Pass
2	18	1.8	2.9	Pass
3	21	2.1	2.9	Pass
4	15.8	1.58	2.9	Pass

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

16. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	
Driver board ID	
Driver board Drawing No/Issue No	
Driver board Serial Number	
Monitor board ID	
Monitor board Drawing No/Issue No	
Monitor board Serial Number	

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P63……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..17/3/10……………..

Drive Card ID……T_TOP63P………………..
Monitor Card ID…Mon126…..………………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

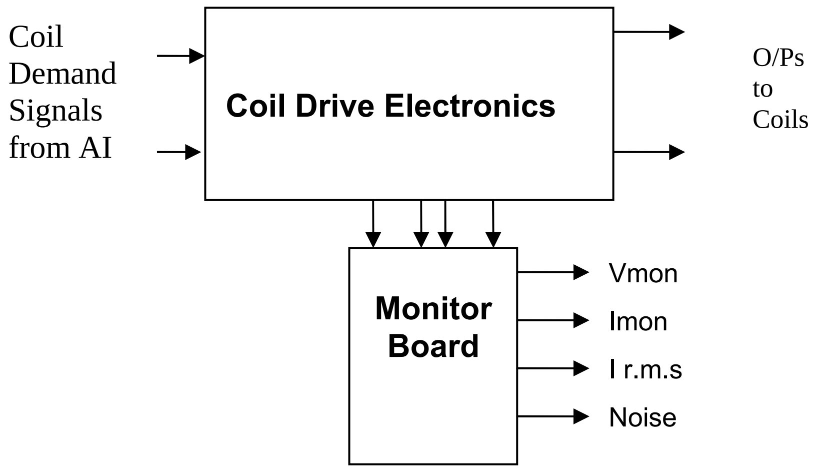

FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P63……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P63……………………Serial No ………………………………
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Date……………..17/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit………………T_TOP_P63……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P63……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

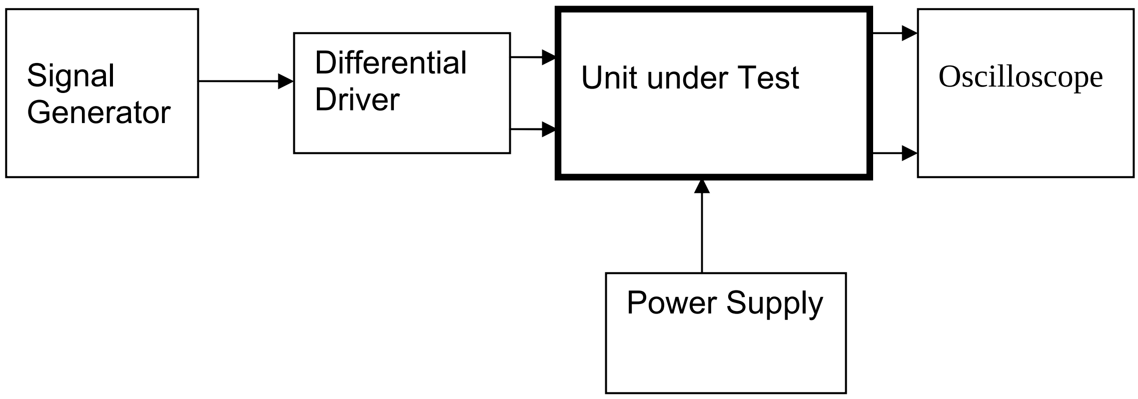
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P63……………………Serial No ………………………………
Test Engineer…..Xen……..……………
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6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	**- 16.5 supply current (mA)**
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	**Plus**	**Minus**
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P63……………………Serial No ………………………………
Test Engineer…..Xen…….………….
Date……………..17/3/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P63……………………Serial No ………………………………
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Date……………..17/3/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.752	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.755	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.753	√

Unit……………..T_TOP_P63……………………Serial No ………………………………
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Date……………..17/3/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.40	2.9μV√Hz	√
2		1.61	2.9μV√Hz	√
3		1.54	2.9μV√Hz	√
4		1.10	2.9μV√Hz	√

Unit………………T_TOP_P63……………………Serial No ………………………………
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10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.8		
10Hz	-30.8		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..T_TOP_P63……………………Serial No ………………………………
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11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

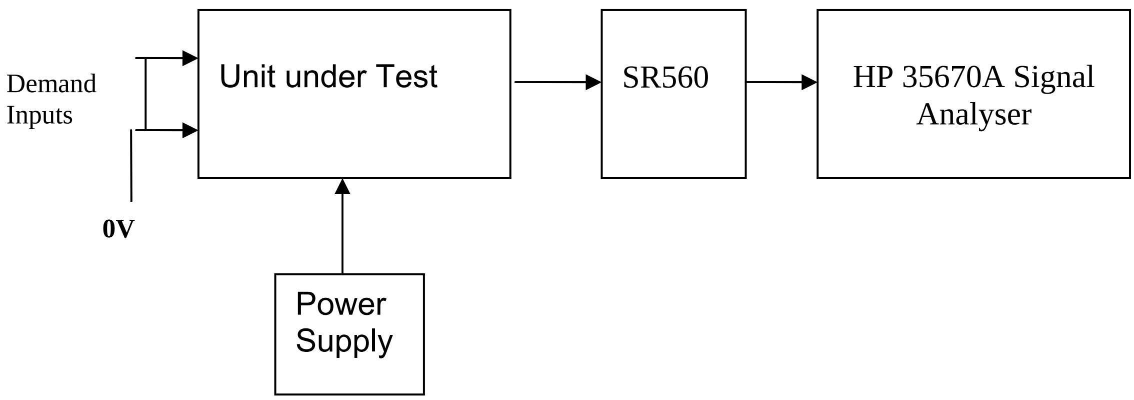
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	CH1 IC1	38.4	√
CH1 Negative		CH1 IC5	42.6	√
CH2 Positive	12.20	CH2 IC1	42.1	√
CH2 Negative		CH2 IC5	41.8	√
CH3 Positive	12.20	CH3 IC1	42.1	√
CH3 Negative		CH3 IC5	44.0	√
CH4 Positive	12.20	CH4 IC1	40.1	√
CH4 Negative		CH4 IC5	40.9	√

Unit.................T_TOP_P63.......................Serial No ....
Test Engineer.....Xen......................
Date................20/7/10..................

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.6	-160.6
Ch2	-160dB	-97.9	-157.9
Ch3	-160dB	-101.1	-161.1
Ch4	-160dB	-97.3	-157.3

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P63……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s) +/- 2.5mA	Pass?
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit.................TTOP63P.......................Serial No ....
Test Engineer....................RMC
Date...............................18/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP63P
Driver board ID	TTOP63P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP63P
Monitor board ID	MON126
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON126

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P64……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..21/7/10……………..

Drive Card ID……T_TOP64P…………………
Monitor Card ID…Mon68………………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

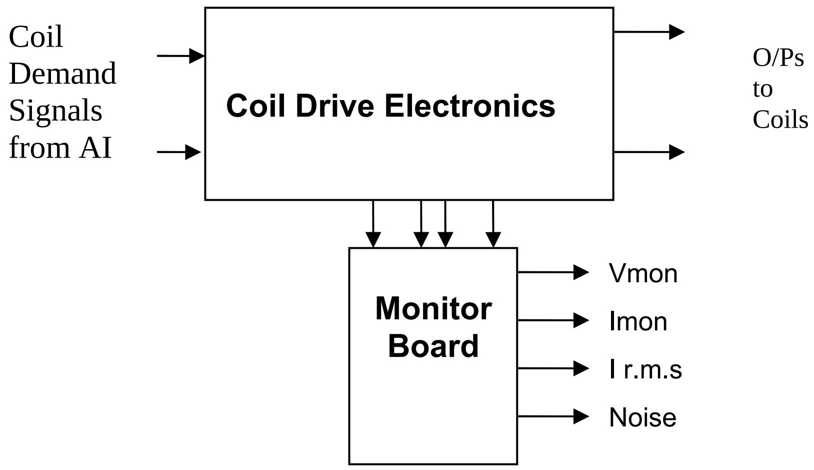

FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P64……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..21/7/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P64……………………Serial No ………………………………
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3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 1 & 2.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit.................T_TOP_P64.......................Serial No ....
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4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P64……………………Serial No ………………………………
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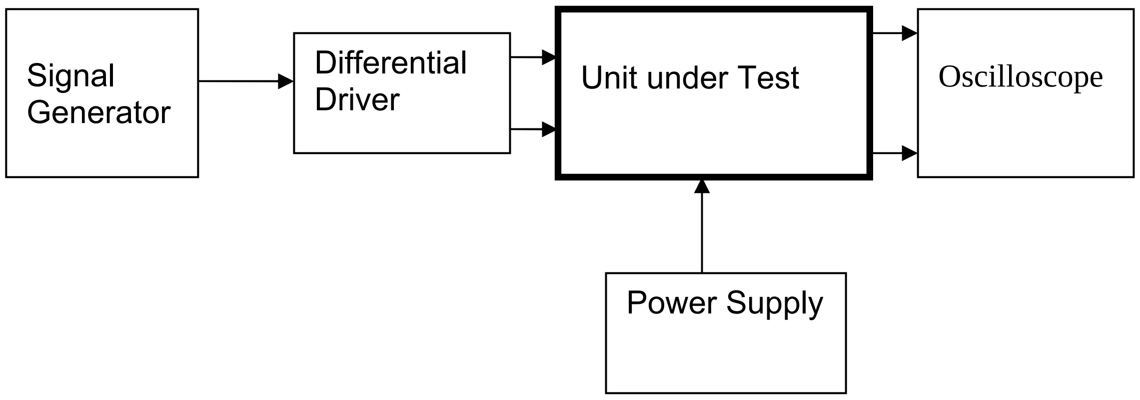
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P64……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….T_TOP_P64……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..17/3/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P64……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..17/3/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.752	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.753	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.752	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.752	√
	Pin 10	RMS Current	0.75v dc	0.751	√

Unit……………..T_TOP_P64……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..17/3/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		0.97	2.9μV√Hz	√
2		0.94	2.9μV√Hz	√
3		1.26	2.9μV√Hz	√
4		1.48	2.9μV√Hz	√

Unit……………..T_TOP_P64……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..17/3/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..T_TOP_P64……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..17/3/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

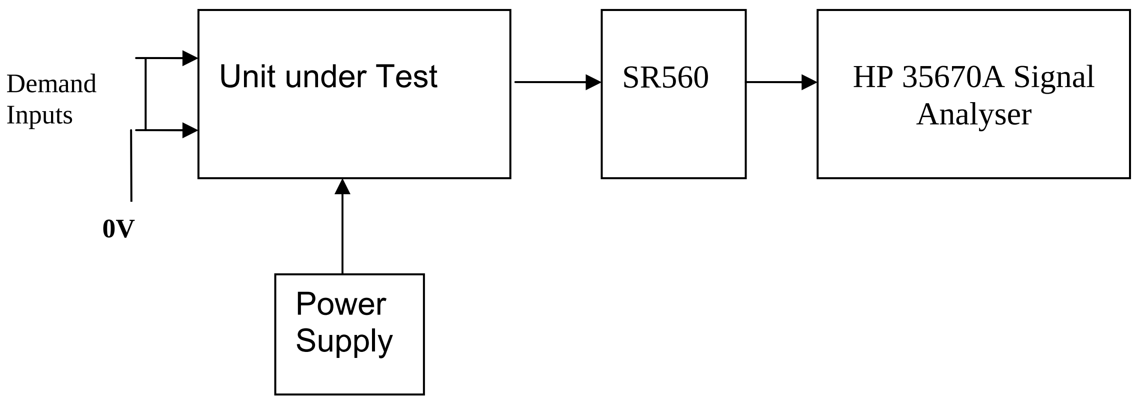
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	CH1 IC1	38.9	√
CH1 Negative		CH1 IC5	40.9	√
CH2 Positive	12.18	CH2 IC1	43.1	√
CH2 Negative		CH2 IC5	42.3	√
CH3 Positive	12.18	CH3 IC1	41.4	√
CH3 Negative		CH3 IC5	39.7	√
CH4 Positive	12.18	CH4 IC1	39.7	√
CH4 Negative		CH4 IC5	41.4	√

Unit……………..T_TOP_P64……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..21/7/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-101.8	-161.8
Ch2	-160dB	-101.9	-161.9
Ch3	-160dB	-101.3	-161.3
Ch4	-160dB	-98.9	-158.9

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P64……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..20/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s) +/- 2.5mA**	**Pass?**
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.0mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.25	82.5mA	120mA	84.8mA	√

Unit…………..TTOP64P……………………..Serial No ………………………………
Test Engineer…………………RMC
Date……………………………18/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP64P
Driver board ID	TTOP64P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP64P
Monitor board ID	MON68P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON68P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….T_TOP_P65……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..17/3/10……………..

Drive Card ID……T_TOP65P………………..
Monitor Card ID…Mon127…..………………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

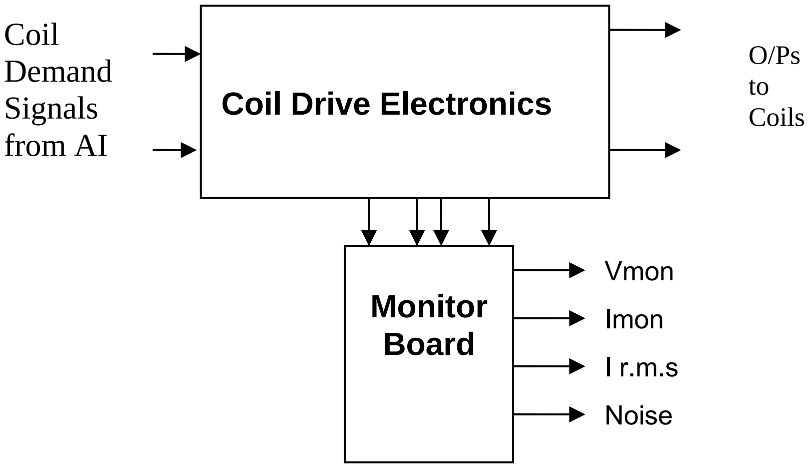


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit..................T_TOP_P65........................Serial No ....
Test Engineer.....Xen.......................
Date................17/3/10..................

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_P65…………………….Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..17/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit……………….T_TOP_P65…………………….Serial No ……………………………….
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	**SIGNAL**	**DESCRIPTION**	**Pd in from Sat**	**OK?**
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	**SIGNAL**	**Monitors:**	**In from Sat**	**OK?**
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	**SIGNAL**	**DESCRIPTION**	**DC in Connector**	**OK?**
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P65……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

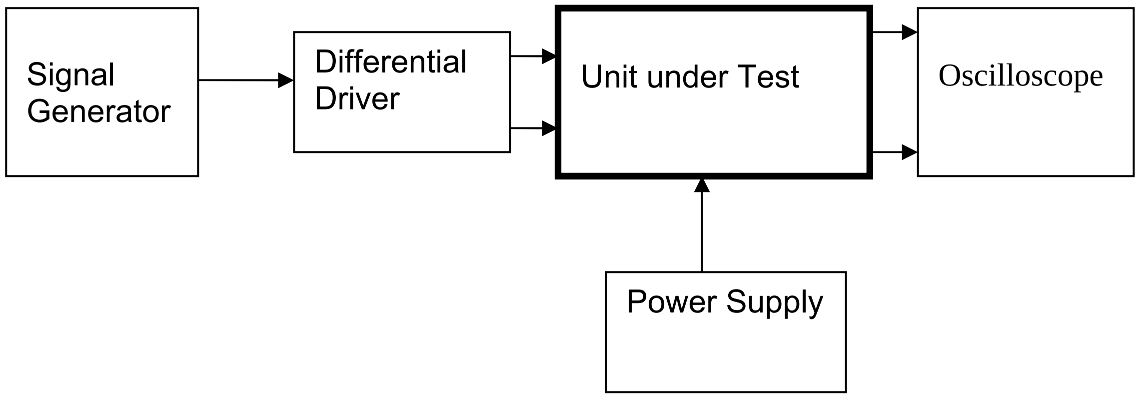
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P65……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P65……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………T_TOP_P65……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..17/3/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.750	√
	Pin 1	RMS Current	0.75v dc	0.752	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.750	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.748	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.750	√
	Pin 10	RMS Current	0.75v dc	0.755	√

Unit……………..T_TOP_P65……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..17/3/10……………..

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	**Output**	**/(Pre-amplifier gain)**	**Maximum value**	**Pass/Fail**
1	19.7	1.97	2.9	Pass
2	16.5	1.65	2.9	Pass
3	13.4	1.34	2.9	Pass
4	14.9	1.49	2.9	Pass

Unit……………..T_TOP_P65…………………..Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..17/3/10…………….

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..T_TOP_P65……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/3/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

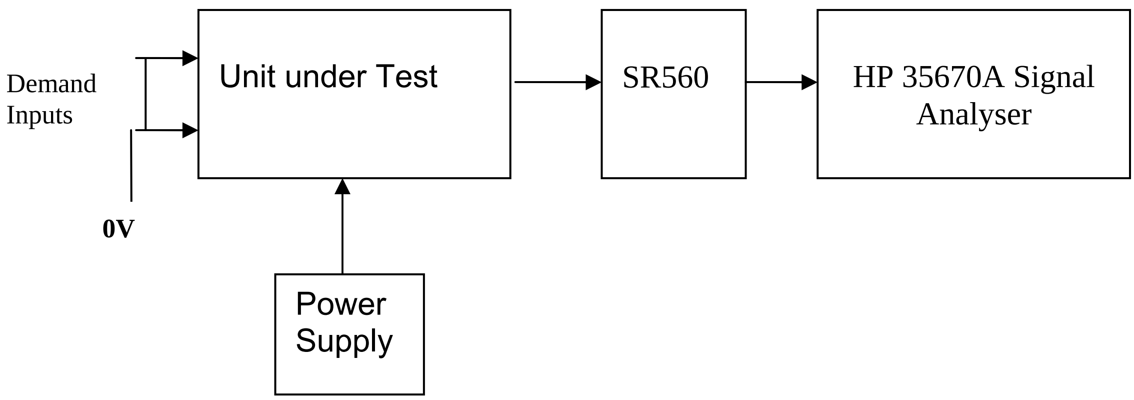
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	CH1 IC1	38.9	√
CH1 Negative		CH1 IC5	41.1	√
CH2 Positive	12.18	CH2 IC1	41.1	√
CH2 Negative		CH2 IC5	41.4	√
CH3 Positive	12.18	CH3 IC1	43.6	√
CH3 Negative		CH3 IC5	43.6	√
CH4 Positive	12.18	CH4 IC1	39.2	√
CH4 Negative		CH4 IC5	42.1	√

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	100.74	-160.74
Ch2	-160dB	-99.3	-159.3
Ch3	-160dB	-100.3	-160.3
Ch4	-160dB	-101.4	-101.4

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity)
and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P65……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..17/3/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.36	85.5mA	120mA	84.8mA	√
2	39.4	3.36	85.3mA	120mA	84.8mA	√
3	39.3	3.34	85.0mA	120mA	84.8mA	√
4	39.4	3.35	85.0mA	120mA	84.8mA	√

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP65P
Driver board ID	TTOP65P
Driver board Drawing No/Issue No	D0902747 V6
Driver board Serial Number	TTOP65P
Monitor board ID	MON127
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON127

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/3/10……………..

Drive Card ID………T_TOP66P……………..
Monitor Card ID……Mon170…..………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

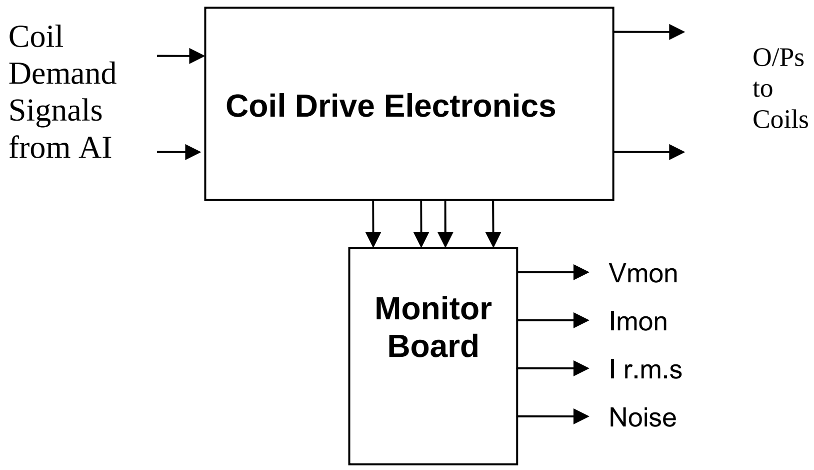


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit……………..T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

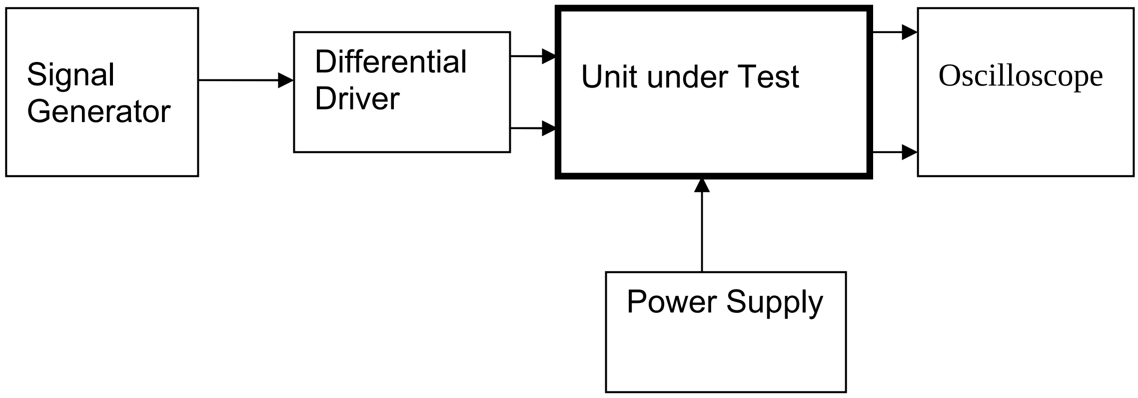
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	**- 16.5 supply current (mA)**
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	**Plus**	**Minus**
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit.................T_TOP_P66.......................Serial No ....
Test Engineer.....Xen.......................
Date................16/3/10..................

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/3/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.750	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.751	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.756	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.756	√

Unit……………..T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

9. Voltage Monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain.

Ch.	**Output**	**/(Pre-amplifier gain)**	**Maximum value**	**Pass/Fail**
1		1.65	2.9	Pass
2		2.28	2.9	Pass
3		1.72	2.9	Pass
4		1.38	2.9	Pass

Unit………………T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..16/3/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………...T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

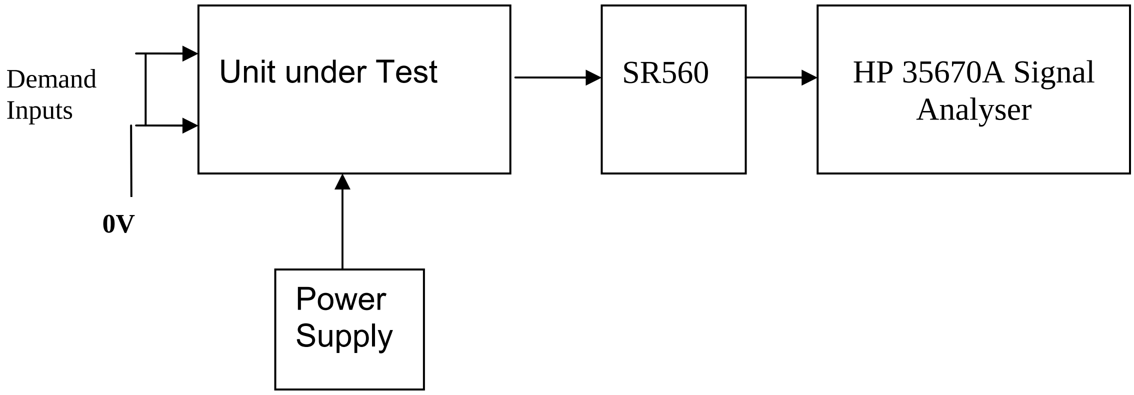
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	**CH1 IC1**	41.8	√
CH1 Negative		**CH1 IC5**	43.6	√
CH2 Positive	12.19	**CH2 IC1**	41.6	√
CH2 Negative		**CH2 IC5**	42.1	√
CH3 Positive	12.19	**CH3 IC1**	40.6	√
CH3 Negative		**CH3 IC5**	41.8	√
CH4 Positive	12.19	**CH4 IC1**	39.7	√
CH4 Negative		**CH4 IC5**	42.6	√

Unit………………………………….Serial No …………………………….
Test Engineer…………………
Date……………………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.5	-160.5
Ch2	-160dB	-100.5	-160.5
Ch3	-160dB	-98.0	-158.0
Ch4	-160dB	-98.3	-158.3

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P66……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..16/3/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	3.35	85.2mA	120mA	84.8mA	√
2	39.4	3.37	85.5mA	120mA	84.8mA	√
3	39.3	3.35	85.2mA	120mA	84.8mA	√
4	39.4	3.36	85.3mA	120mA	84.8mA	√

Unit……………………………………Serial No ………………………………
Test Engineer…………………RMC
Date……………………………

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP66P
Driver board ID	TTOP66P
Driver board Drawing No/Issue No	D0902747 V6
Driver board Serial Number	TTOP66P
Monitor board ID	MON 170
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON 170

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx	Advanced LIGO UK	11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date …………….13/8/10..…………….

Drive Card ID……T_TOP67P…………………
Monitor Card ID…Mon66………………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

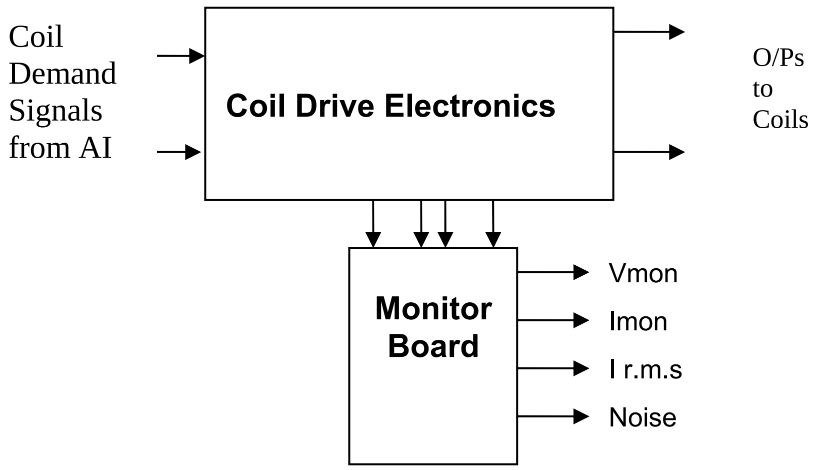


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date ……………13/8/10..……………..

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..16/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 3 & 4.

Four 0.39uF filter capacitors have been added to the driver board (C200). Visually checked for open circuit resistor joints and using the DVM checked for short circuits and double checked for open circuits.

Unit……………….T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/3/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

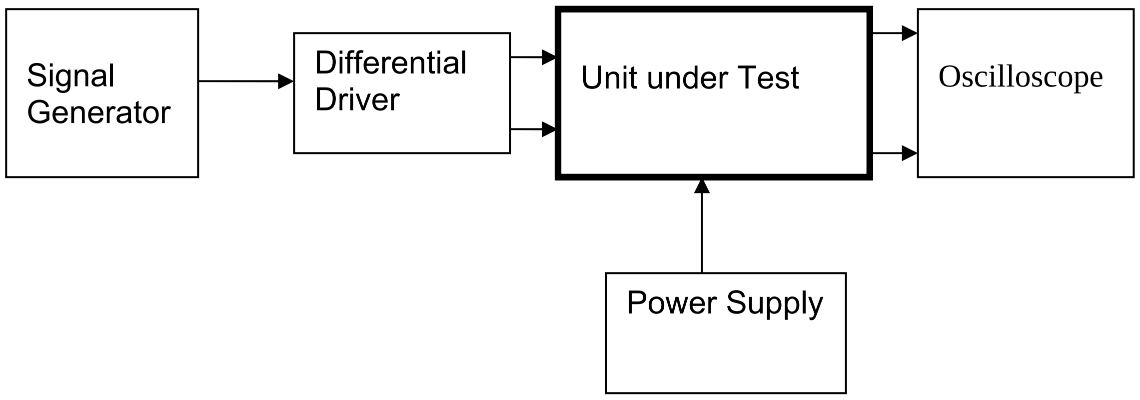
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..16/3/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	**- 16.5 supply current (mA)**
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	**Plus**	**Minus**
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..16/3/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to dc.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.751	√
	Pin 1	RMS Current	0.75v dc	0.755	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.751	√
	Pin 4	RMS Current	0.75v dc	0.753	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.751	√
	Pin 7	RMS Current	0.75v dc	0.7512	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.751	√
	Pin 10	RMS Current	0.75v dc	0.756	√

Unit……………..T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen……….…………
Date……………..16/3/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.67	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.67	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.67	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.48	2.9μV√Hz	√
2		1.46	2.9μV√Hz	√
3		1.15	2.9μV√Hz	√
4		1.63	2.9μV√Hz	√

Unit……………..T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..17/3/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………….T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..17/3/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

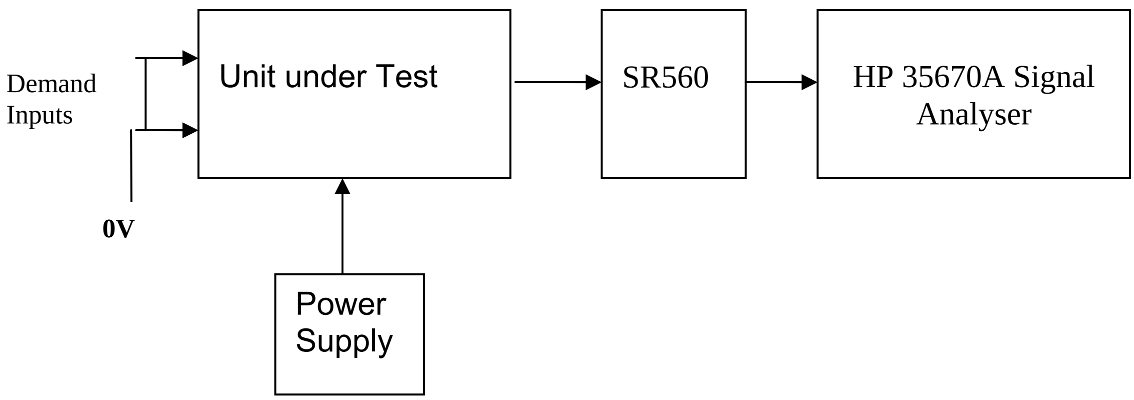
The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.19	**CH1 IC1**	37.5	√
CH1 Negative		**CH1 IC5**	39.9	√
CH2 Positive	12.19	**CH2 IC1**	40.4	√
CH2 Negative		**CH2 IC5**	44.0	√
CH3 Positive	12.19	**CH3 IC1**	38.2	√
CH3 Negative		**CH3 IC5**	39.7	√
CH4 Positive	12.19	**CH4 IC1**	37.0	√
CH4 Negative		**CH4 IC5**	41.6	√

Unit.................T_TOP_67P.......................Serial No ....
Test Engineer.....Xen.....................
Date..................28/7/10..................

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-99.3	-159.3
Ch2	-160dB	-102.2	-162.2
Ch3	-160dB	-101.3	-161.3
Ch4	-160dB	-101.5	-161.5

Notes:
Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)
Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_67P……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..19/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s) +/- 2.5mA**	**Pass?**
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.26	82.7mA	120mA	84.8mA	√
3	39.3	3.25	82.7mA	120mA	84.8mA	√
4	39.4	3.26	82.7Ma	120mA	84.8mA	√

Unit....................TTOP67P....................Serial No ....
Test Engineer....................RMC
Date................................23/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP 67P
Driver board ID	TTOP 67P
Driver board Drawing No/Issue No	D0902747 V6
Driver board Serial Number	TTOP 67P
Monitor board ID	MON66
Monitor board Drawing No/Issue No	D070480_04_K
Monitor board Serial Number	MON66

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0xxx

Advanced LIGO UK

11 November 2009

Triple TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

TRIPLE TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..21/7/10………………

Drive Card ID……T_TOP69P…………………
Monitor Card ID…Mon171…..…………………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Triple assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

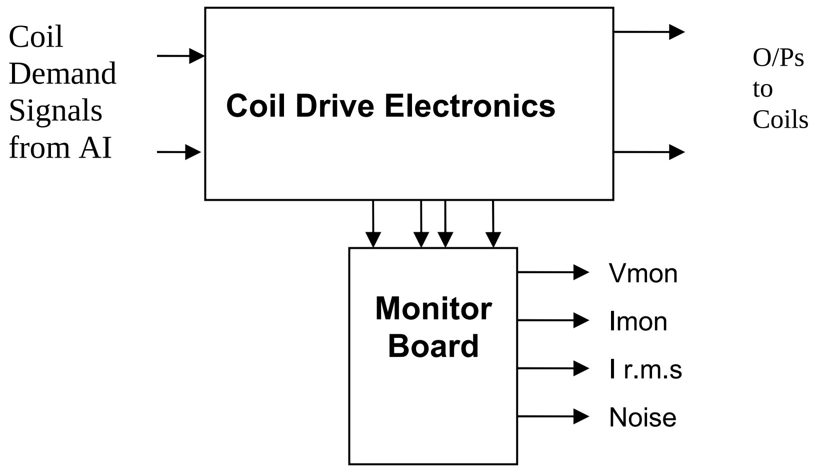


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..21/7/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..15/3/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Capacitors C102 and C103 have been replaced by a 33pF polypropylene capacitor on all channels.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH2.

Added the four 0.39uF filter capacitors C200, and checked for short circuits and open circuit resistor joints. Visually inspected the joints on the Mantis microscope.

Unit………………T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/3/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit……………….T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen……..………….
Date……………..15/3/10………………

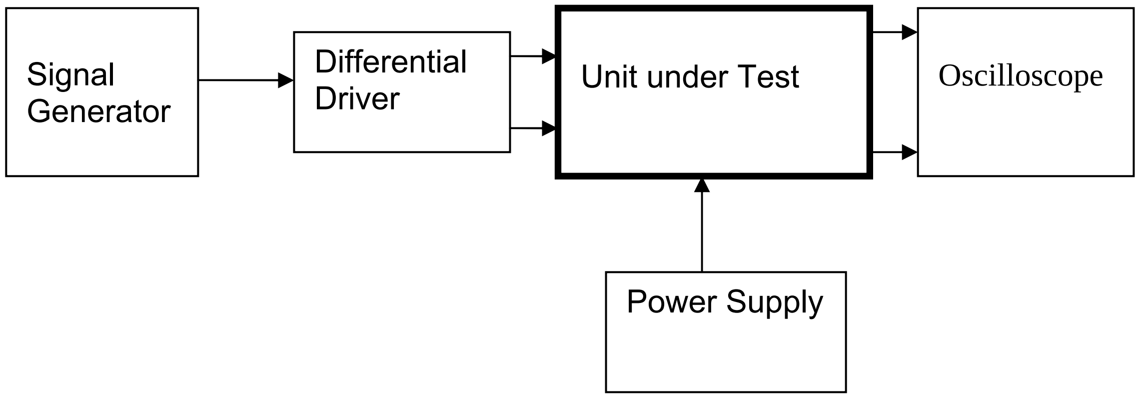
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

OL = Overload

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	R.M.S Current 1
2	Current Monitor 1
3	Voltage Monitor 1
4	R.M.S Current 2
5	Current Monitor 2
6	Voltage Monitor 2
7	R.M.S Current 3
8	Current Monitor 3
9	Voltage Monitor 3
10	R.M.S Current 4
11	Current Monitor 4
12	Voltage Monitor 4
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen…….……………
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6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	**- 16.5 supply current (mA)**
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	**Plus**	**Minus**
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..15/3/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..15/3/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c..

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	0.75v r.m.s	0.754	√
	Pin 1	RMS Current	0.75v dc	0.754	√
2	Pin 5	Current Monitor	0.75v r.m.s	0.752	√
	Pin 4	RMS Current	0.75v dc	0.757	√
3	Pin 8	Current Monitor	0.75v r.m.s	0.753	√
	Pin 7	RMS Current	0.75v dc	0.753	√
4	Pin 11	Current Monitor	0.75v r.m.s	0.753	√
	Pin 10	RMS Current	0.75v dc	0.759	√

Unit……………..T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..15/3/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 5v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	1.66	1.6v to 1.7v	√
2	Pins 3,11	Pin 6	1.66	1.6v to 1.7v	√
3	Pins 5,13	Pin 9	1.66	1.6v to 1.7v	√
4	Pins 7, 15	Pin 12	1.66	1.6v to 1.7v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.09	2.9μV√Hz	√
2		1.51	2.9μV√Hz	√
3		0.93	2.9μV√Hz	√
4		1.09	2.9μV√Hz	√

Unit……………..T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..15/3/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Using the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/3/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 5v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	DRIVER	Temperature	<60°C?
CH1 Positive	12.20	**CH1 IC1**	40.6	√
CH1 Negative		**CH1 IC5**	41.4	√
CH2 Positive	12.20	**CH2 IC1**	41.4	√
CH2 Negative		**CH2 IC5**	40.6	√
CH3 Positive	12.20	**CH3 IC1**	41.6	√
CH3 Negative		**CH3 IC5**	40.1	√
CH4 Positive	12.20	**CH4 IC1**	39.2	√
CH4 Negative		**CH4 IC5**	38.9	√

Unit……………..T_TOP_P69…………………..Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..21/7/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.

Replace the lid of the box, and replace screws.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode

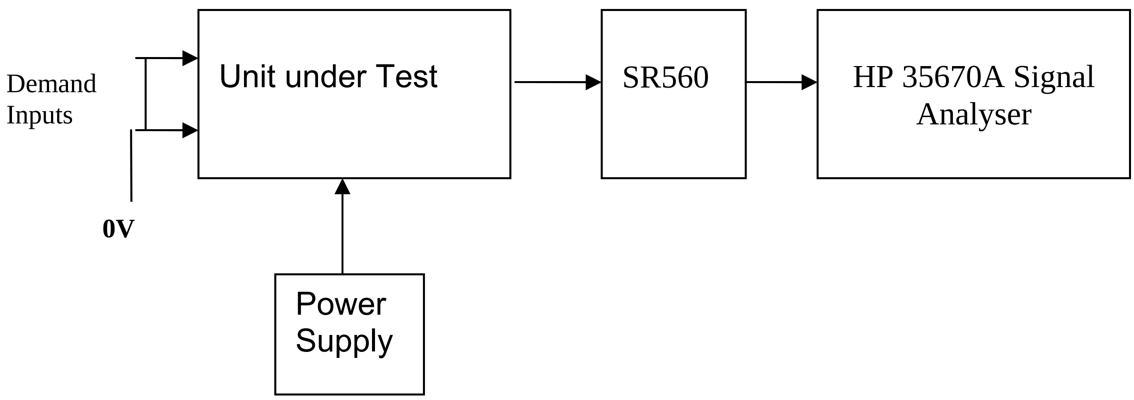
Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.

Switch the filters in.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-160dB	-100.7	-160.7
Ch2	-160dB	-102.1	-162.1
Ch3	-160dB	-101.2	-161.2
Ch4	-160dB	-102.2	-162.2

Notes:

Specified noise output current at 10 Hz = 100 pA/√Hz (IMC & cavity) and 3nA /√Hz (BS & FM). Total output resistance = 100 Ohms (BOSEM)

Amplifier noise voltage should therefore < 10nA/√Hz (tightest spec) or -160dB

Unit……………..T_TOP_P69……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..19/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 5v peak sine wave input on each channel, which should measure 3.353 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification.

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s) +/- 2.5mA**	**Pass?**
1	39.3	3.26	83.0mA	120mA	84.8mA	√
2	39.4	3.27	83.2mA	120mA	84.8mA	√
3	39.3	3.26	83.0mA	120mA	84.8mA	√
4	39.4	3.26	82.7mA	120mA	84.8mA	√

Unit……………..TTOP69P…………………..Serial No ……………………………..
Test Engineer…………………RMC
Date……………………………18/8/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TTOP69P
Driver board ID	TTOP69P[
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	TTOP69P
Monitor board ID	MON171P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON171P

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √