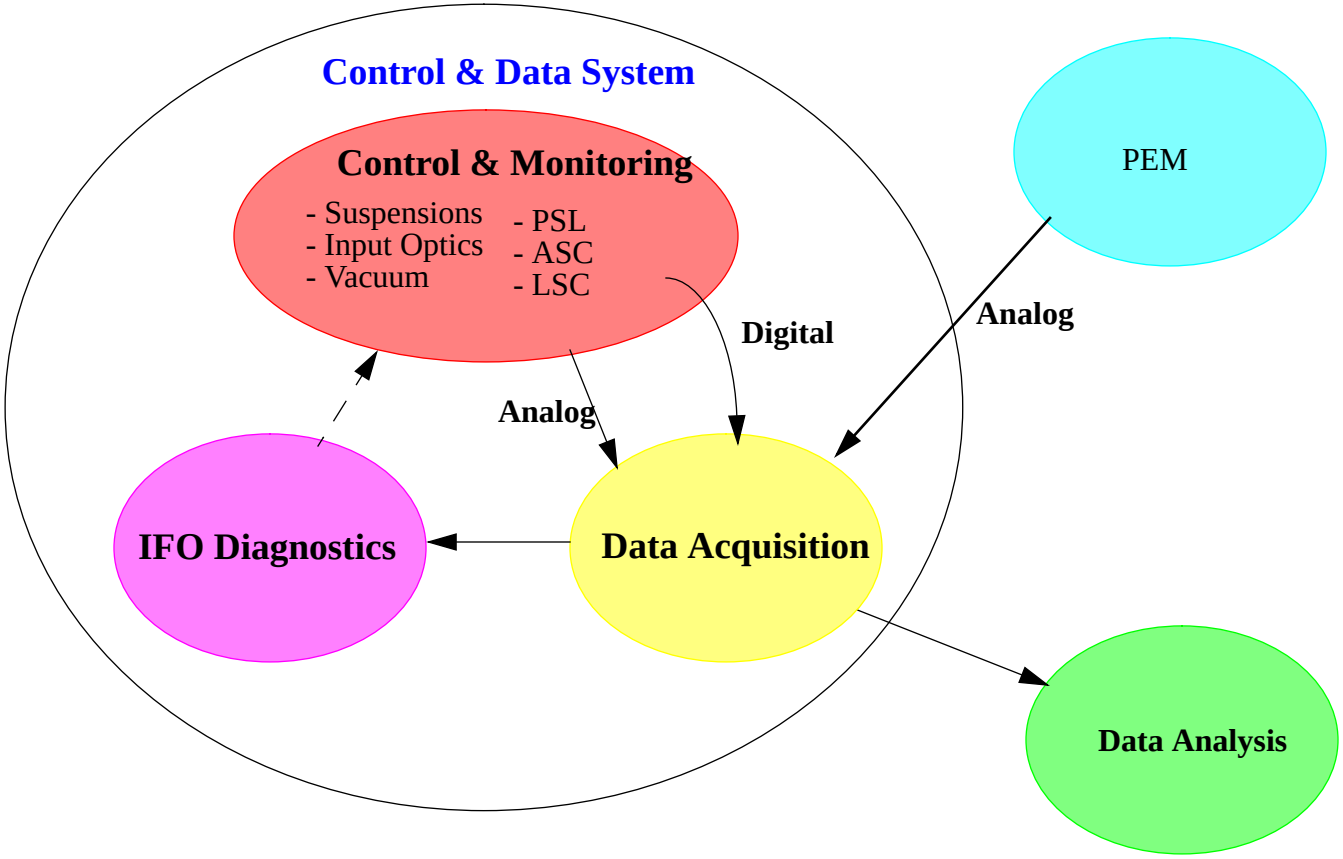
LIGO Data Acquisition System
Final Design Review

- Scope
- General Requirements
- Basic System Overview
- Data Networking
- Data Collection
- Data Formatting
- Data Storage
- Data Presentation

CDS Components



General Requirements

- Acquire analog signals provided by control and monitoring sub-systems at rates from 256 to 16384 samples/sec.
  - Provide anti-alias filtering
  - 16 bit digitization (minimum)
- Acquire signals which have been digitized by control and monitoring subsystems at rates from 1Hz to 16384Hz
- Format acquired data into LIGO/VIRGO standard frame formats.
- Save formatted data to short term storage.
- Provide system control and data display capabilities
- Provide limited data distribution capabilities (to CDS networks only)

Data Channel Count / Rate Estimates

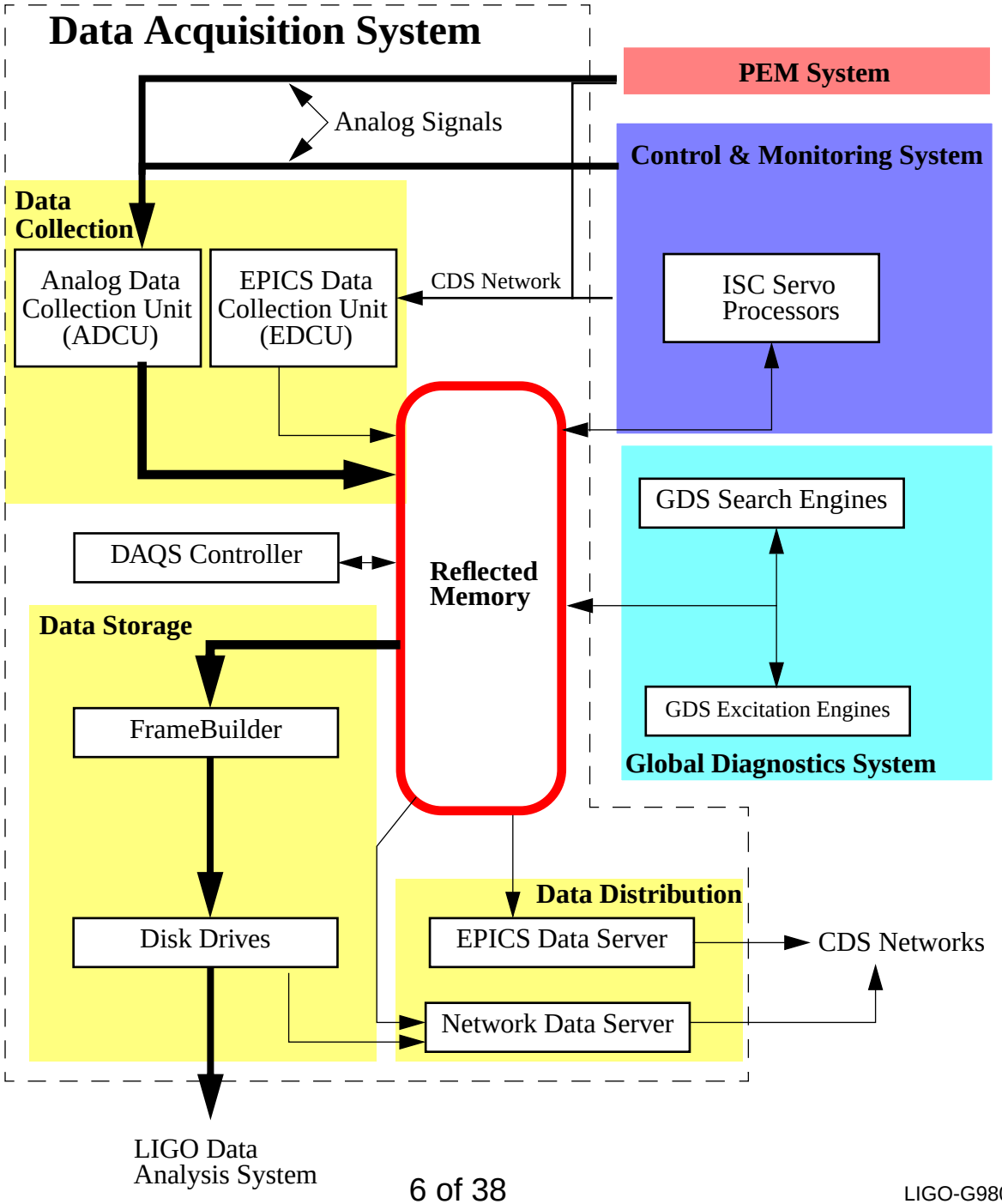
Table 1: DAQS Data Channels / Rates

System	*DAQS Network*		*Data Storage*	
	Channels	*Rate (MByte/sec)*	*Channels*	*Rate (MByte/sec)*
LHO-4K	510	4.22	300	1.88
LHO-2K	548	4.37	332	1.99
LHO-PEM	204	0.89	204	0.89
LHO-VAC	500	0.01	500	0.01
LHO-GDS (Stimulus)	133	2.45		
LLO-4K	515	4.22	305	1.89
LLO-PEM	95	0.46	95	0.46
LLO-VAC	300	0.01	300	0.01
LLO-GDS (Stimulus)	76	0.89		

Noteable Design Changes Since PDR

- Direct connection of ISC and GDS to data acquisition network
  - Allows direct acquisition of digital data from ISC servo processors ie does not require redundant ADC in DAQS
  - Provides GDS direct, real-time access to DAQS data and allows GDS to introduce data into DAQS in time for data framing
  - Allows for digital stimulation signals from GDS to directly connect into CDS digital servos
- DAQS will provide for the disk storage at the sites for data acquisition; LDAS will provide the long term storage capabilities
- Formatting of data into frames has been moved from VME processors to Sun Ultra stations
- Actual data acquisition and frame building have been decoupled

DAQS Block Diagram

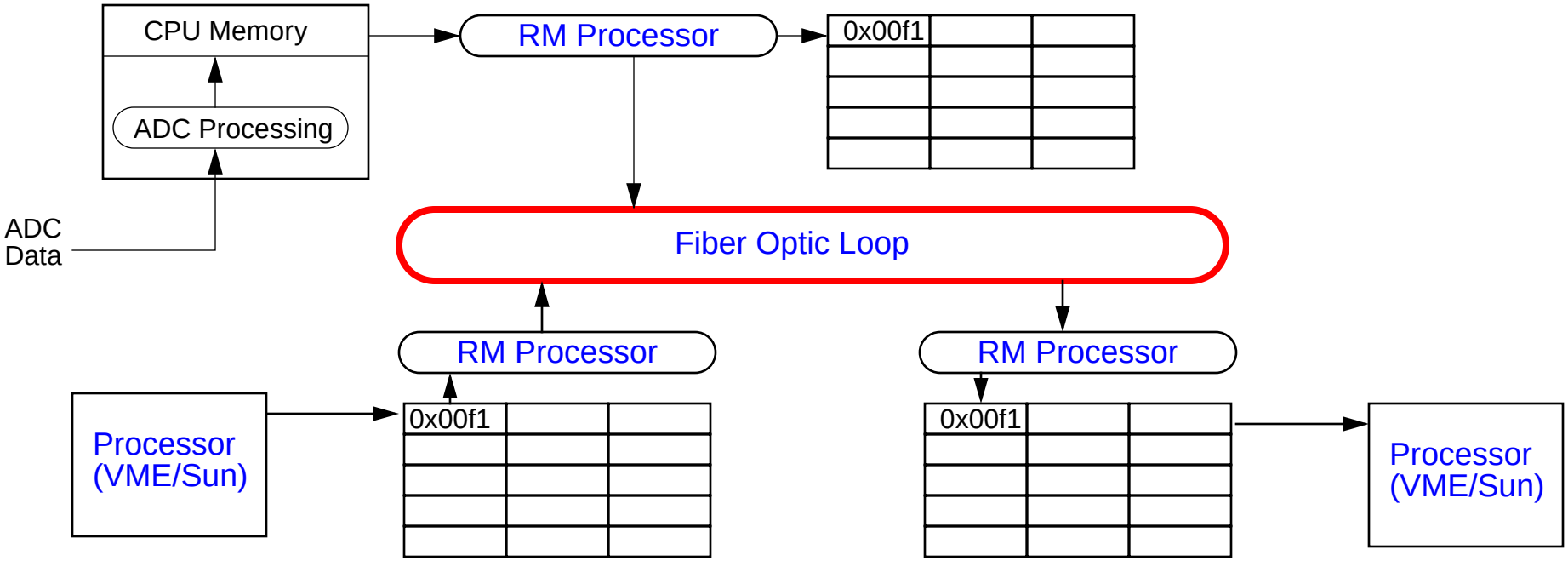


DAQS Network (1)

- Requirements
  - High bandwidth (>11MByte/sec Hanford)
  - Provide copies of data to multiple processors
  - Deterministic data delivery
- DAQS network to be Reflected Memory Network
  - High data thoughput (30MBytes/sec)
  - No software driver development (DAQS will provide API library)
  - Bus Master capabilities, DMA, Remote Interrupts
  - Deterministic
  - Long distance
    - 1km w/multi-mode fiber
    - 10km w/single mode fiber
  - Up to 255 nodes per network loop
  - DAQS will use 2MByte and 4MByte versions (Max. size = 16MBytes)

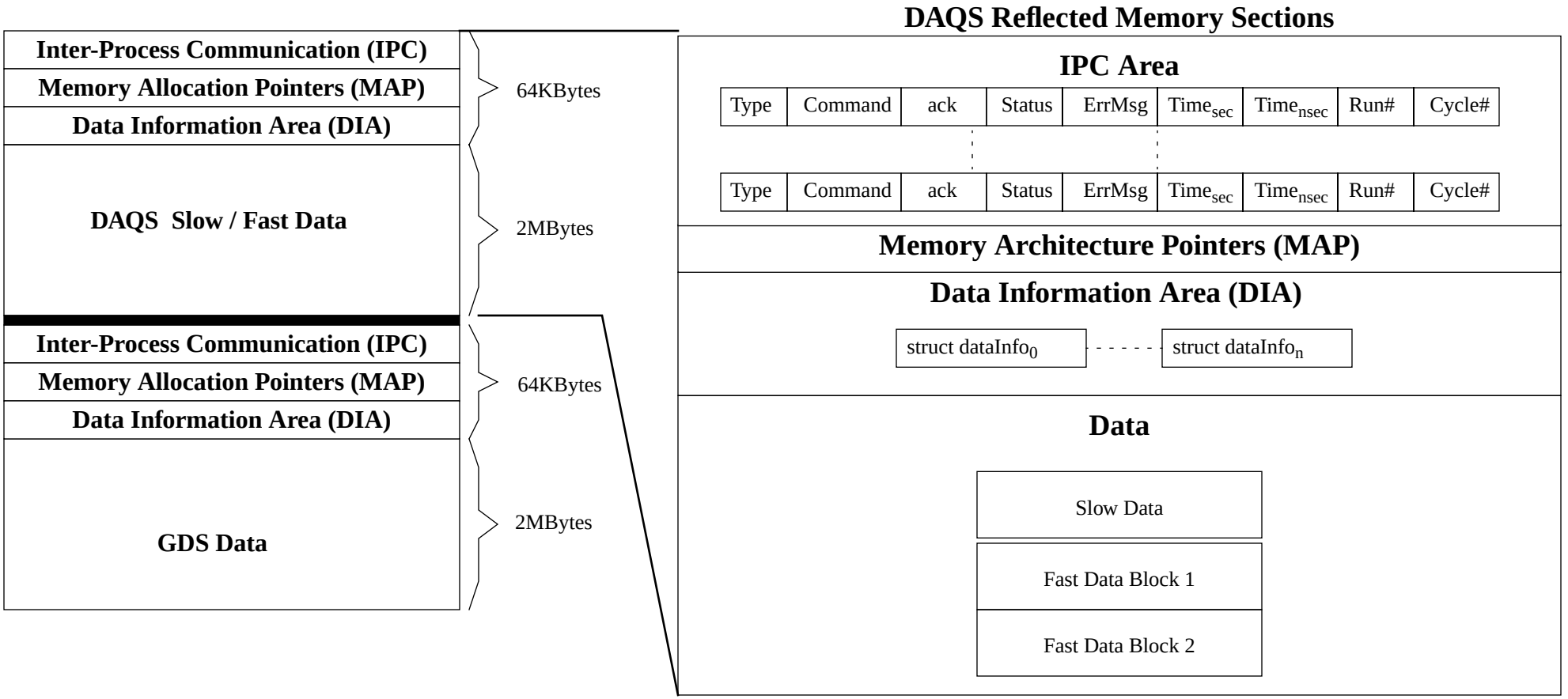
DAQS Network (2)

- Any data written to a reflected memory location at one node is automatically transferred to the same memory location in all nodes on network
- With DMA, reflected memory module can directly copy data from a memory segment in a CPU to all nodes of reflected memory ie main CPU is free to do other tasks as it need not be involved in data transfers



DAQS Network (3)

- 2MBytes assigned for DAQS / 2MBytes assigned to GDS
- Analog DCU only contain upper to 2MByte Partition
- Data will be aligned by ADCU to allow block data transfers (required to meet data rates)



DAQS Network (4)

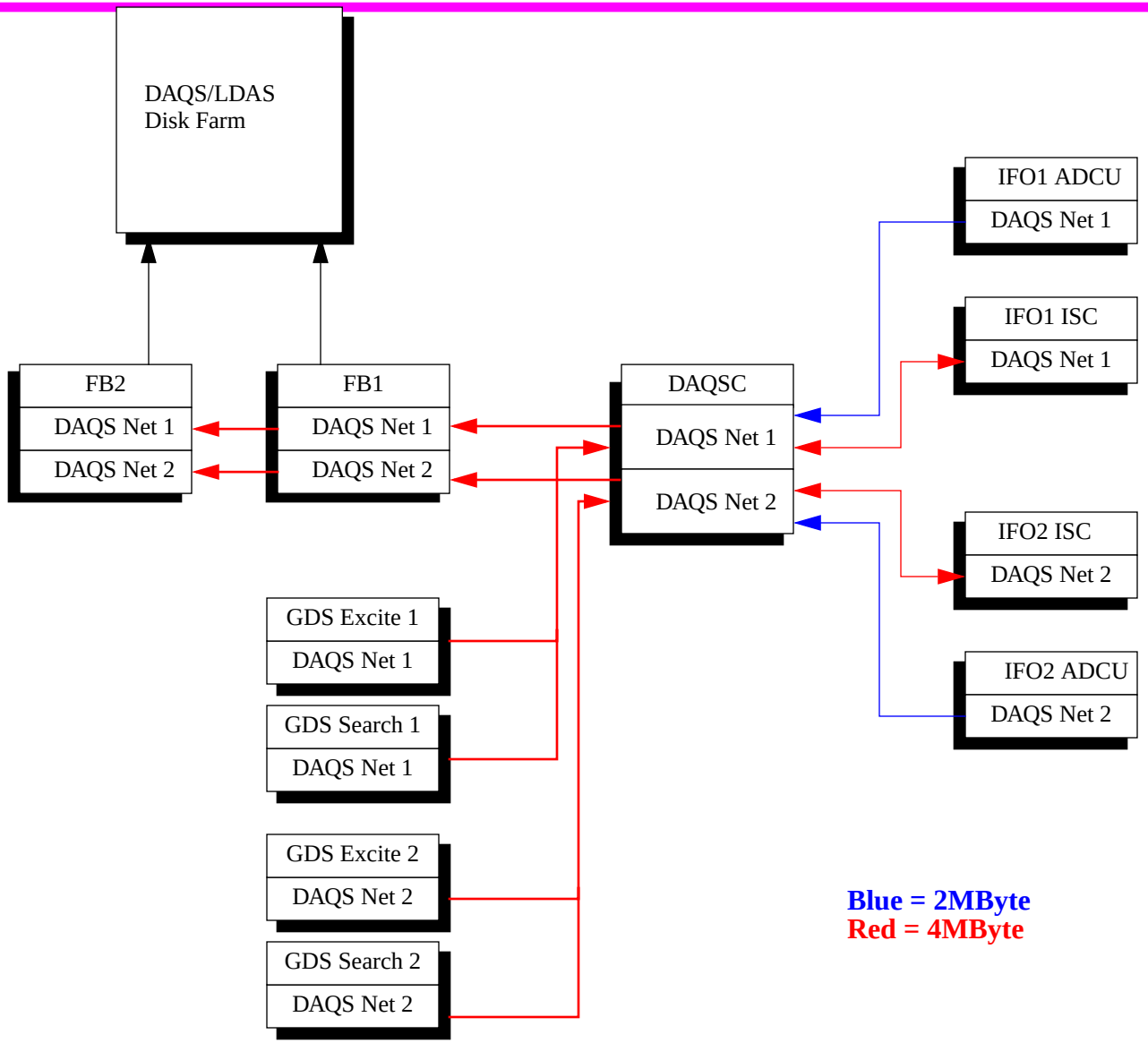
- dataInfo Structure

Data class	*Variable Name*	*Descriptor & Comments*
int	dcuID	Number of dcu which contains this channel
int	chNum	ADC channel number within dcu
char[64]	chName	Name of data channel
char[32]	type	Data type (Short, Float, Double, etc.)
char[32]	dataBlock	Which memory block data is in: Fast/Slow
int	rate	Data rate for this channel
char *	dataPtr	Pointer to data location within first data block of reflected memory

- fastData Structure

Data class	*Variable Name*	*Descriptor & Comments*
int	status	Data status; bit0 = valid/invalid, bit1 = in range/overrange
short	data	Data rate / 16 data points/block

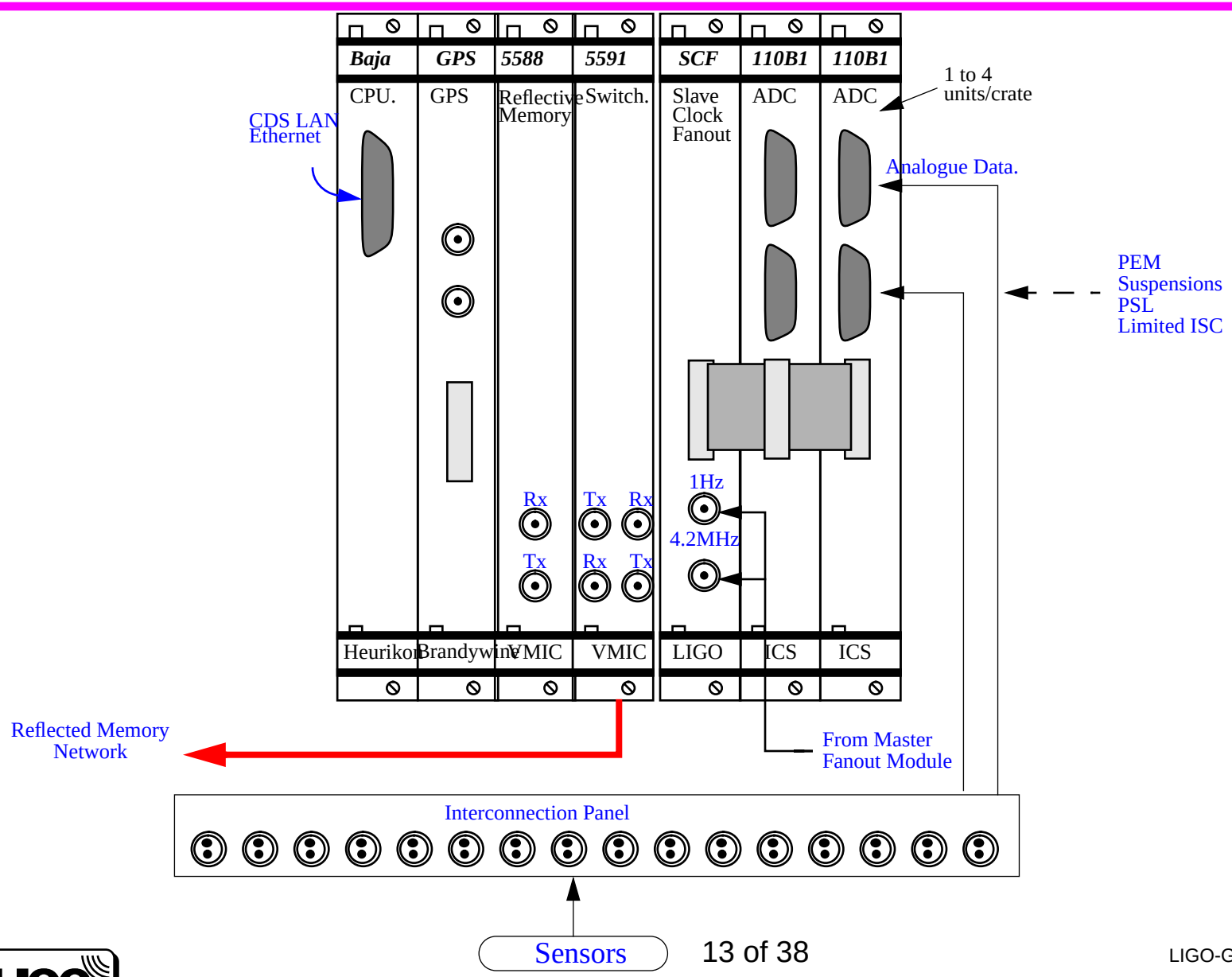
Reflected Memory
Hanford Network Layout



Analog Data Collection Units (ADCU) Requirements

- Requirements
  - Digitize analog signals w/16bit resolution, various rates to 16384Hz
  - Provide anti-alias filtering
  - Accurately time data (10usec accuracy, 1usec resolution)
  - Transfer data to DAQS network at 16Hz

ADCU
Typical Configuration

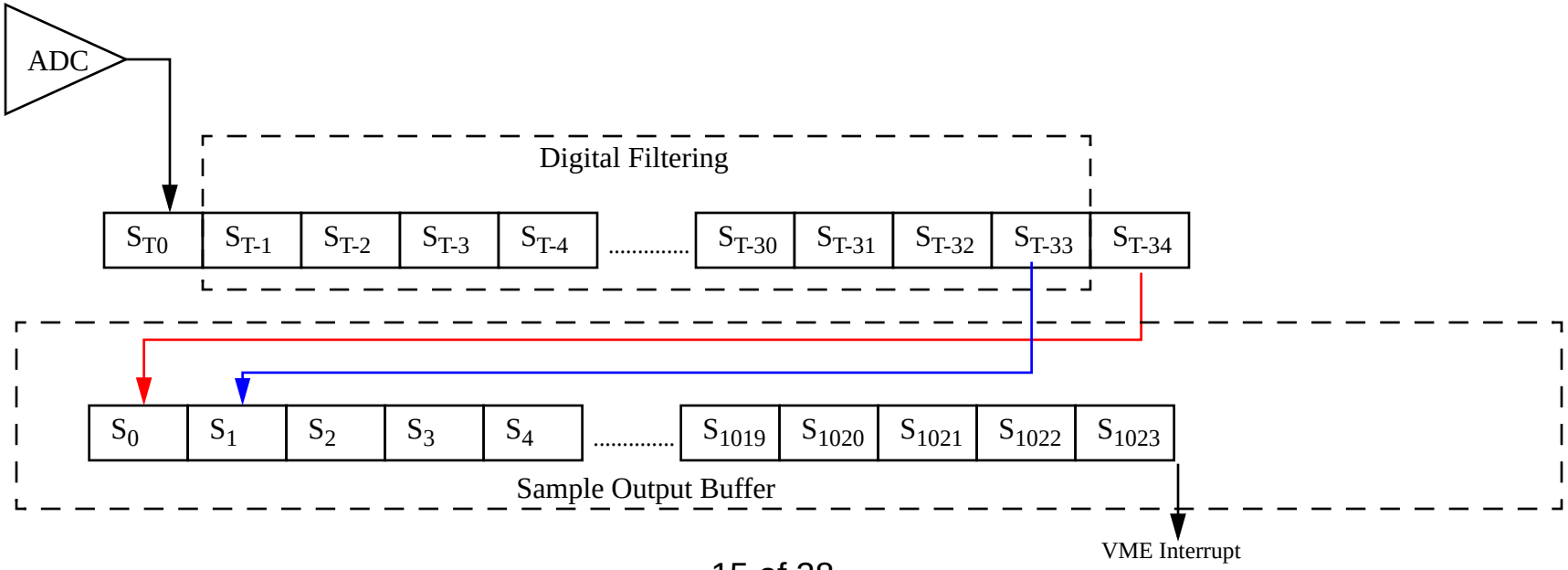


Anti-alias Filtering and Analog-Digital Conversion (1)

- 32 Channel, 100K sample/sec output, 24 bit sigma delta with built in anti-aliasing and programmable gain (will be run in 16 bit mode)
- Dynamic Range: > 105dB (114db typical)
- Anti-aliasing filter: 2-pole Butterworth, fixed frequency (user specified F_c)
- Programmable Gain: -95.2dB to +31.5dB in 0.5dB steps
- Cal/Test: Programmable test signals (8 sequences of 32Ksamples)
- FPDP and VSB bus interfaces for connection to VME DSP modules

Anti-alias Filtering and Analog-Digital Conversion (2)

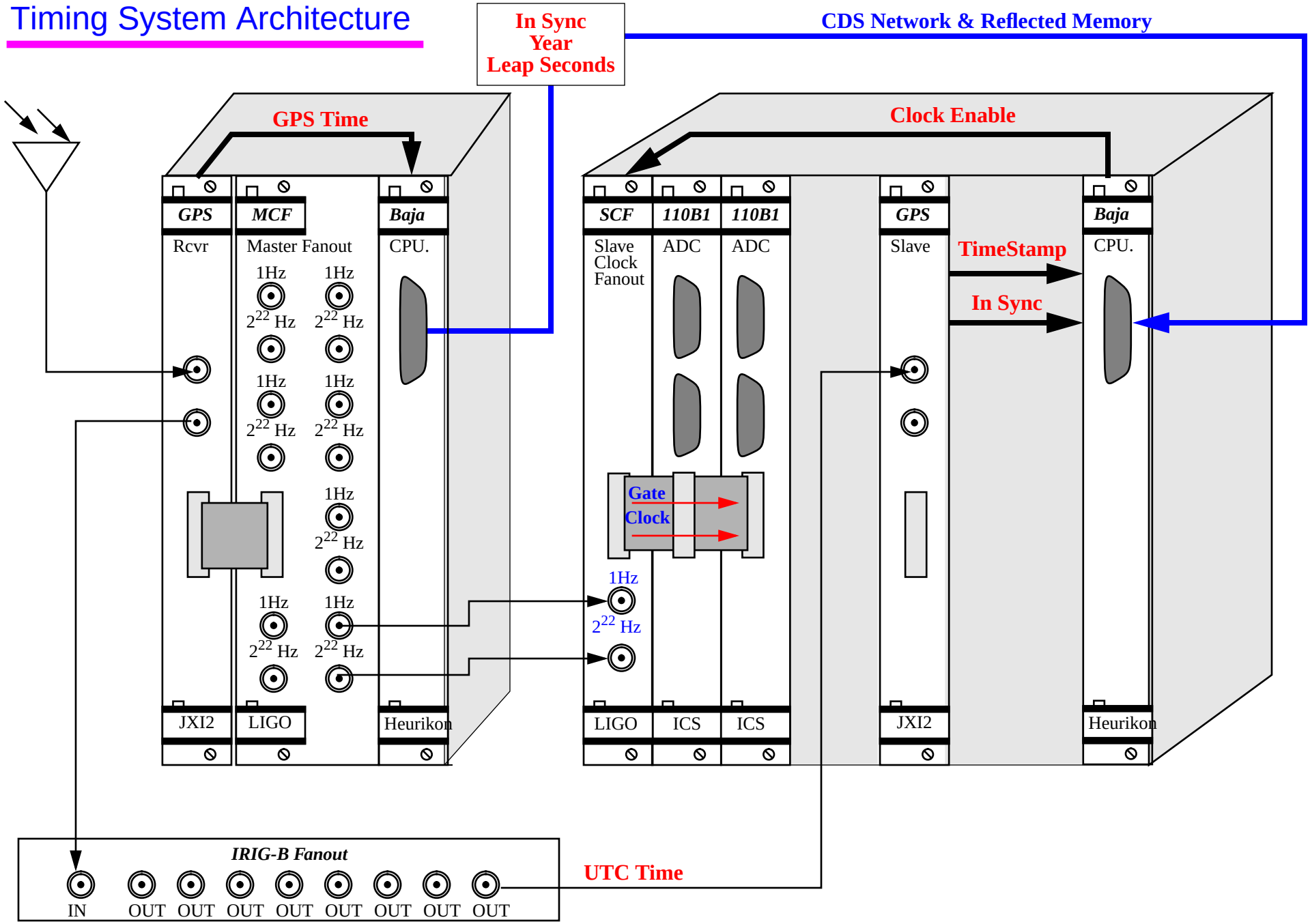
- Generates interrupt on output buffer half full (1024 samples)
- 34 sample gate delay; removed by reading and deleting 34 samples on ADC startup
- Gate delays and time alignment to all data clients at 16Hz drive requirement that all DAQS ADC modules acquire at 16KHz and processors provide decimation



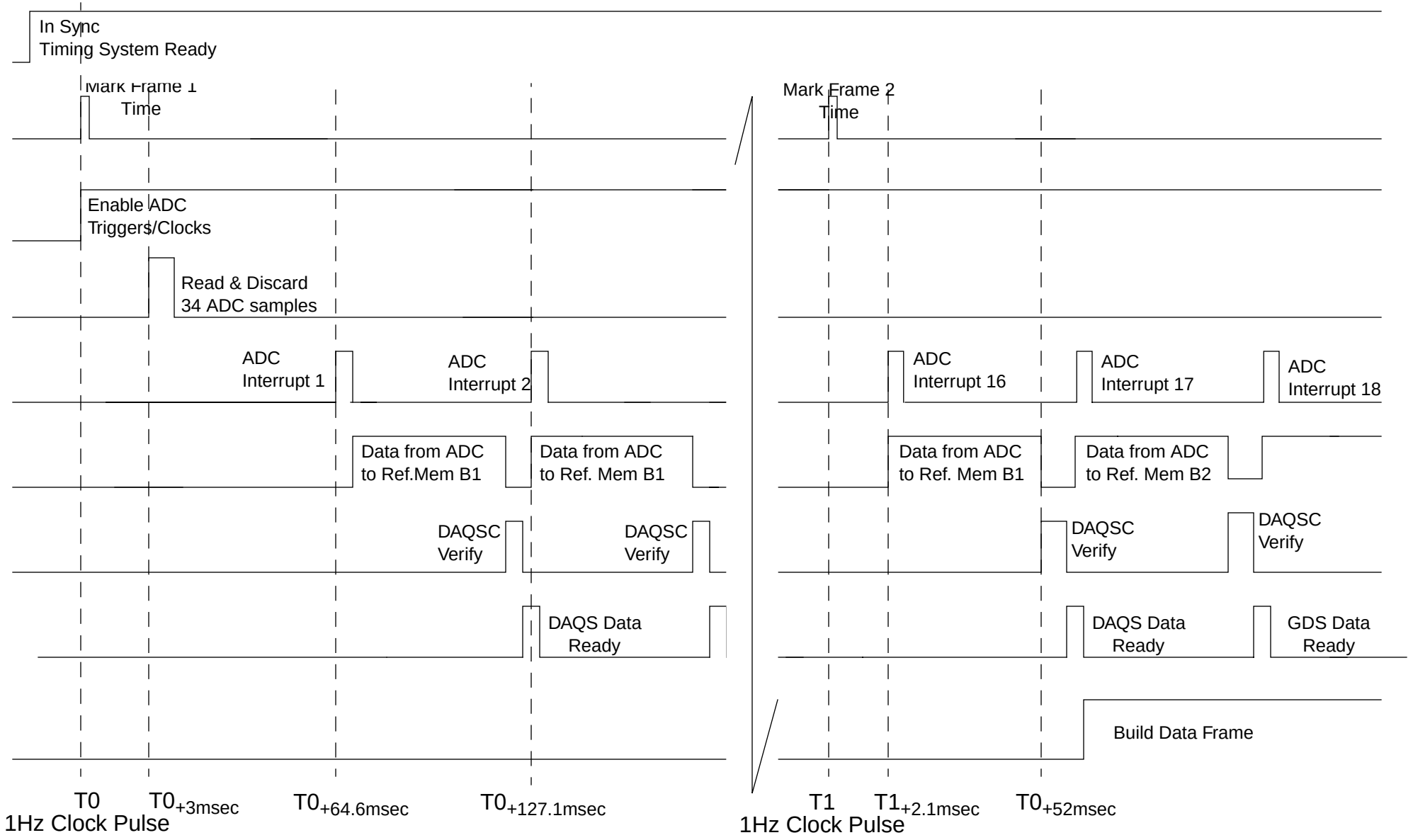
Data Clock and Trigger

- GPS antenna and receiver at each LIGO building (2 at Hanford corner station)
  - JXI-2 VME-Syncclock 32
  - Time resolution of 1usec and timing synchronization of +/- 300nsec (receiver)
  - Built in timing clocks phase locked to GPS signal (4MHz clock jitter 15nsec)
  - Time read from GPS receiver is GPS time in format YMMDDHHMMSS.mmmuuu and converted by code in processor to two long words (seconds nanoseconds) for data timestamping
  - GPS slave units read out in same format except in UTC (no year info)
  - DAQS will provide year, leap second and 'In Sync' information in reflected memory and on CDS networks via EPICS data channels
- Master fanout modules will distribute 1Hz and 2^{22} Hz clocks
- Slave fanout modules will provide clock enable (via software) and 1Hz, 2^{22} Hz, 2^{21} Hz and 2^{14} Hz clock outputs

Timing System Architecture

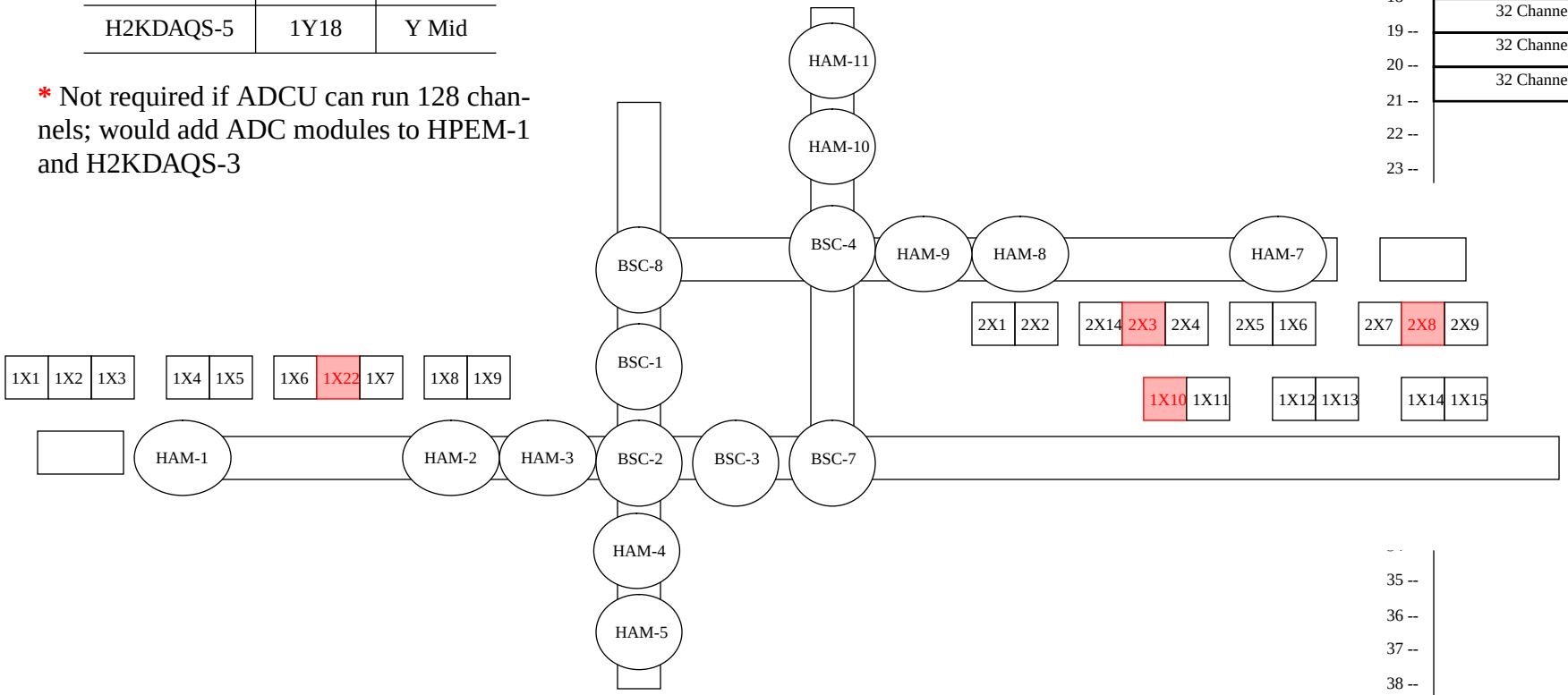


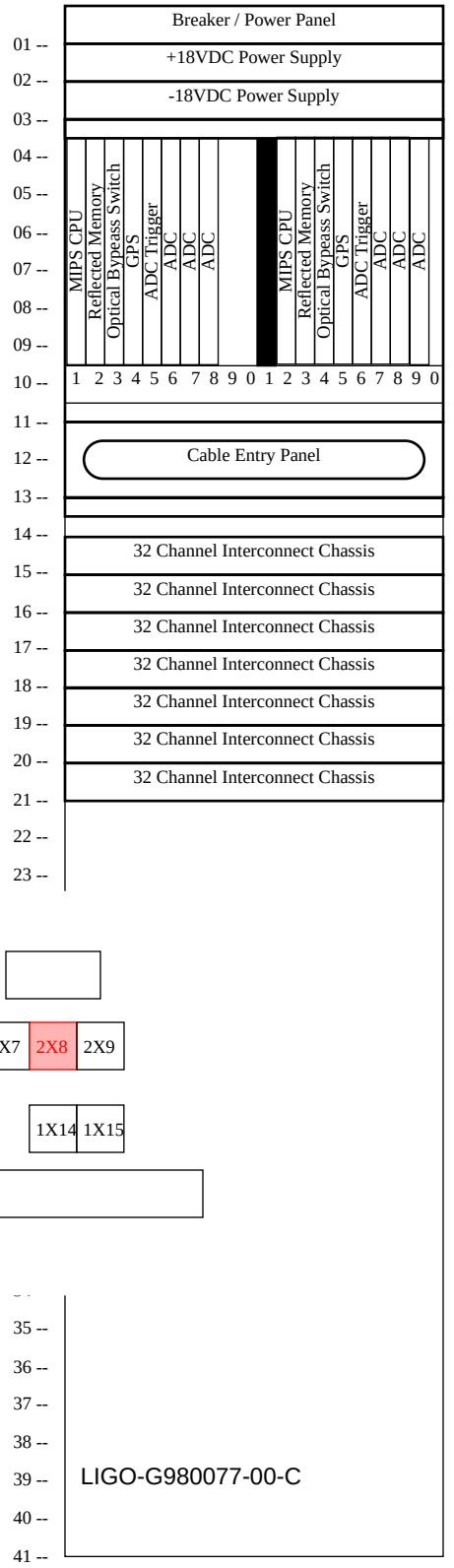
DAQS Timing Diagram

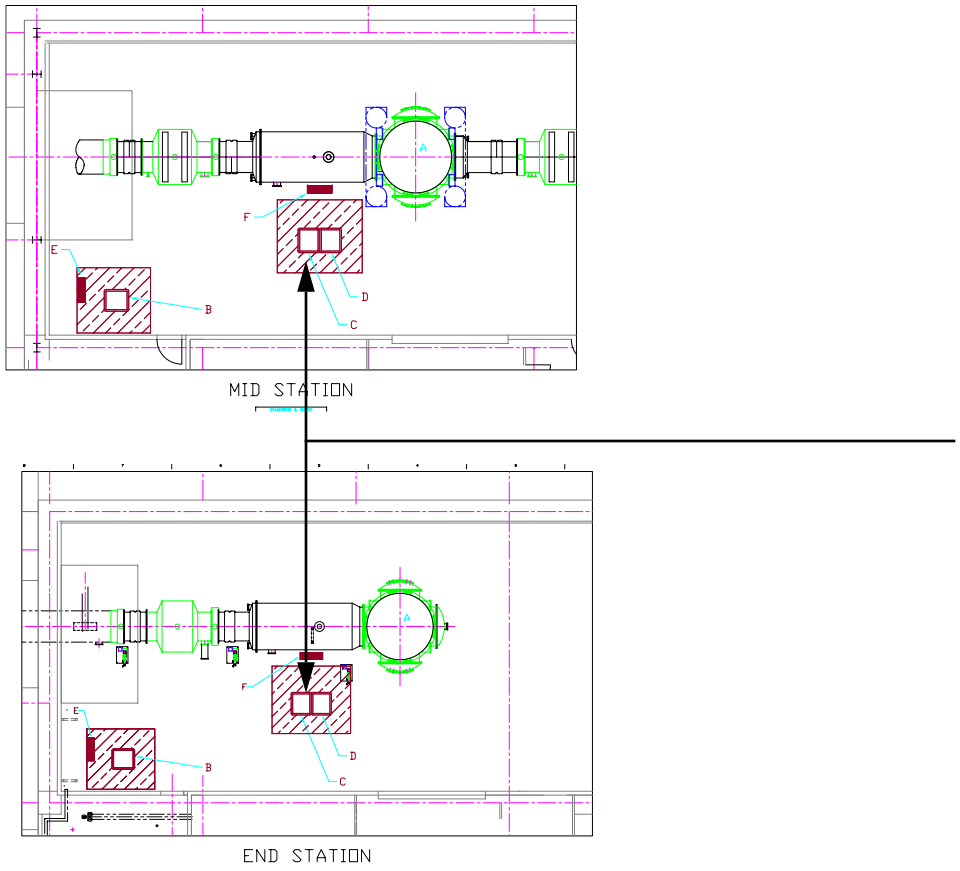


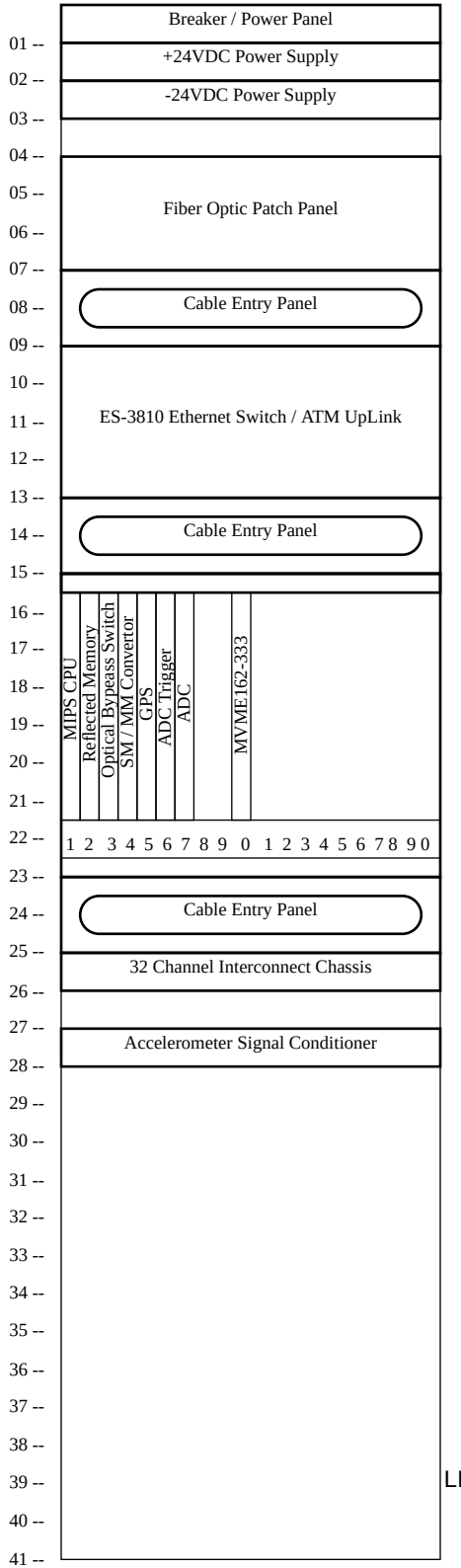
DCU	*Rack*	*Bldg*
H4KDAQS-1	1X22	LVEA
H4KDAQS-2	1X22	LVEA
H4KDAQS-3	1X20	X End
H4KDAQS-4	1Y21	Y End
HPEM-1	1X10	LVEA
HPEM-2*	1X10	LVEA
H2KDAQS-1*	2X8	LVEA
H2KDAQS-2	2X3	LVEA
H2KDAQS-3	2X3	LVEA
H2KDAQS-4	1X17	X Mid
H2KDAQS-5	1Y18	Y Mid

* Not required if ADCU can run 128 channels; would add ADC modules to HPEM-1 and H2KDAQS-3



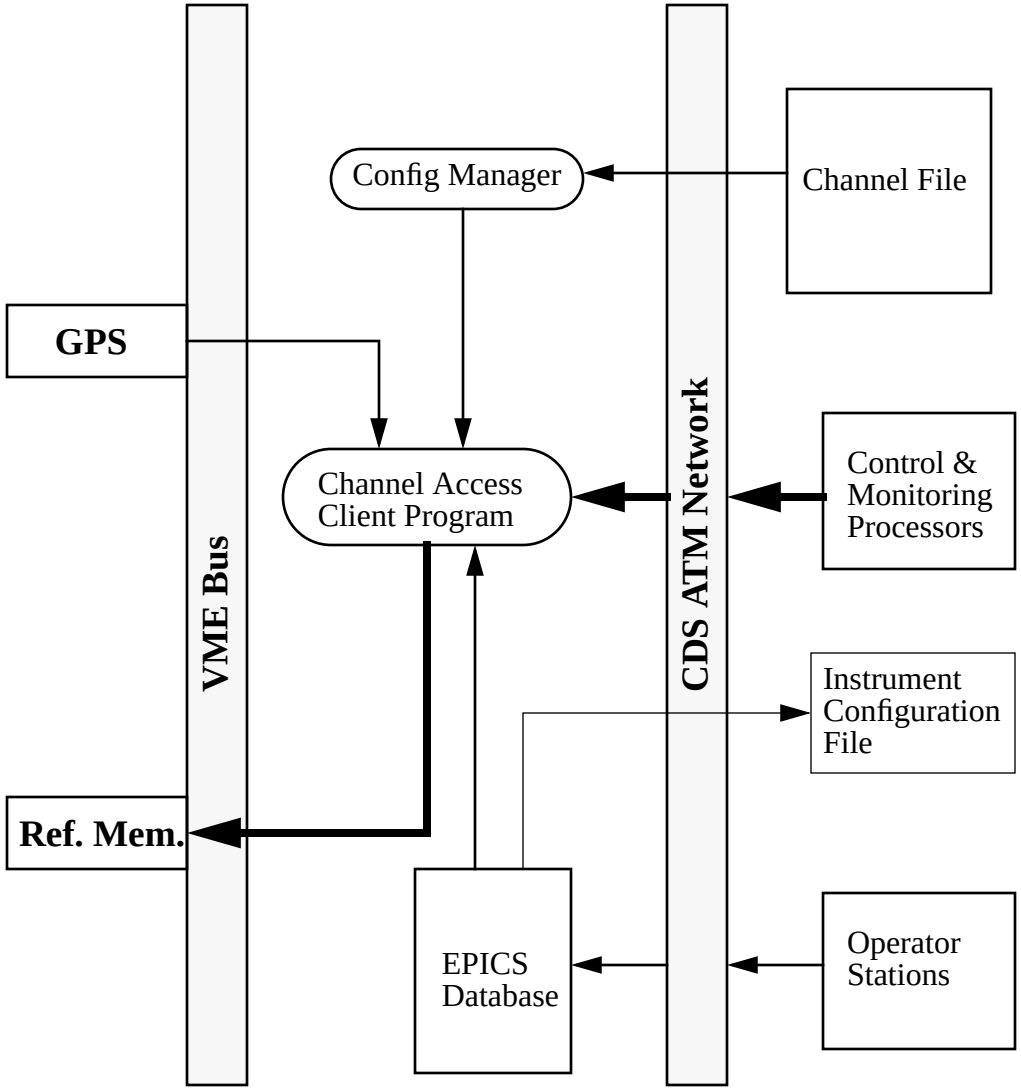



MID STATION
END STATION


Breaker / Power Panel
+24VDC Power Supply
-24VDC Power Supply
Fiber Optic Patch Panel
Cable Entry Panel
ES-3810 Ethernet Switch / ATM UpLink
Cable Entry Panel
MIPS CPU
Reflected Memory
Optical Bypeass Switch
SM / MM Convertor
GPS
ADC Trigger
ADC
MVME162-333
1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0
Cable Entry Panel
32 Channel Interconnect Chassis
Accelerometer Signal Conditioner

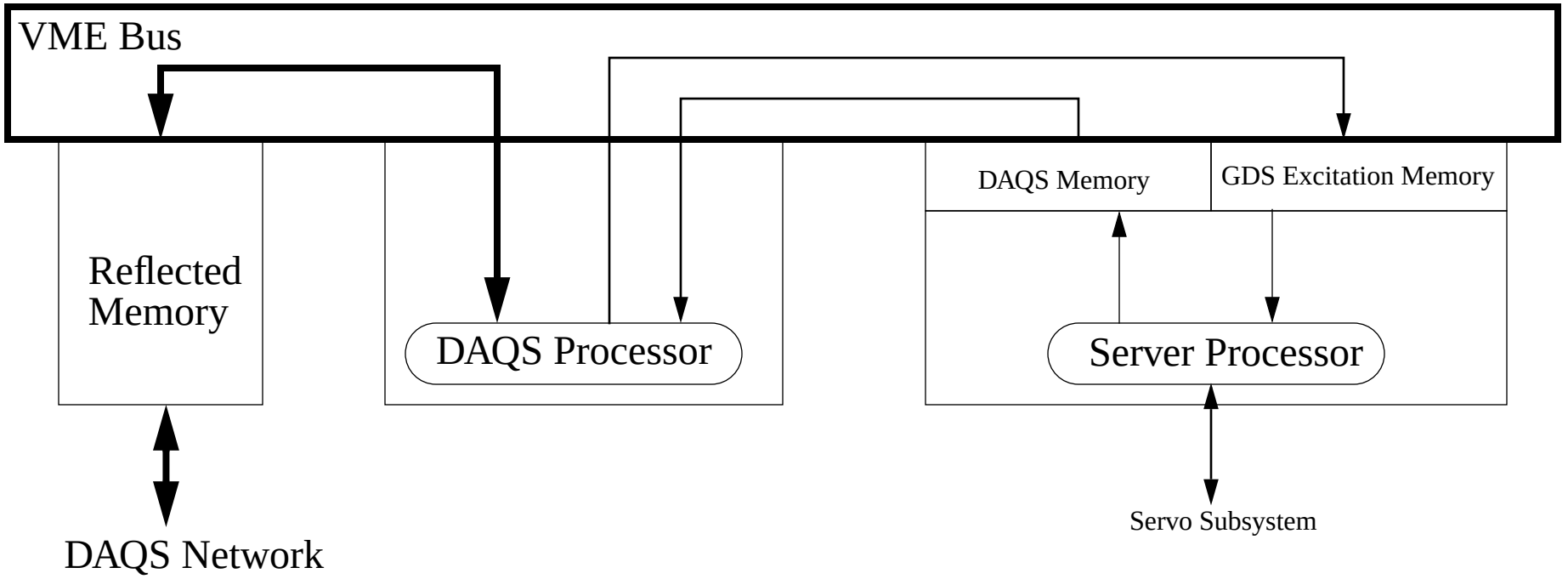
EPICS Data Collection Unit (EDCU)

- Functions:
  - Collects slow (1Hz) data from CDS control systems
  - Collects data from operators on parameters which cannot be read directly from sensors
  - Collects/writes LIGO configuration information (TBD)
- Implementation
  - Single MIPS processor
    - Runs EPICS software to access data via CDS ATM backbone
    - Writes data to Reflected Memory in same fashion as ADCUs on 1Hz trigger from GPS
  - All slow channels are stored in frame as a single array



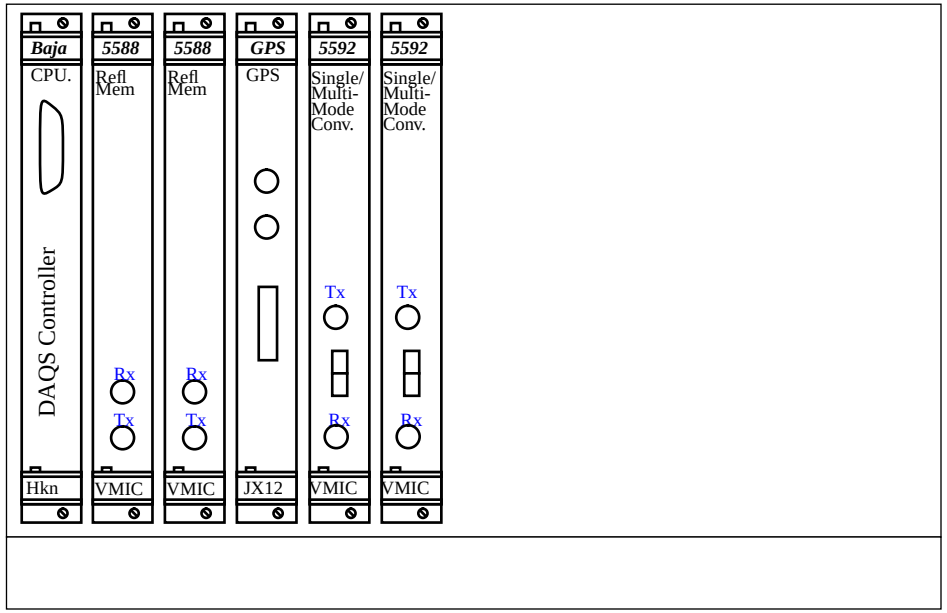
ISC Data Collection
Basic Concept

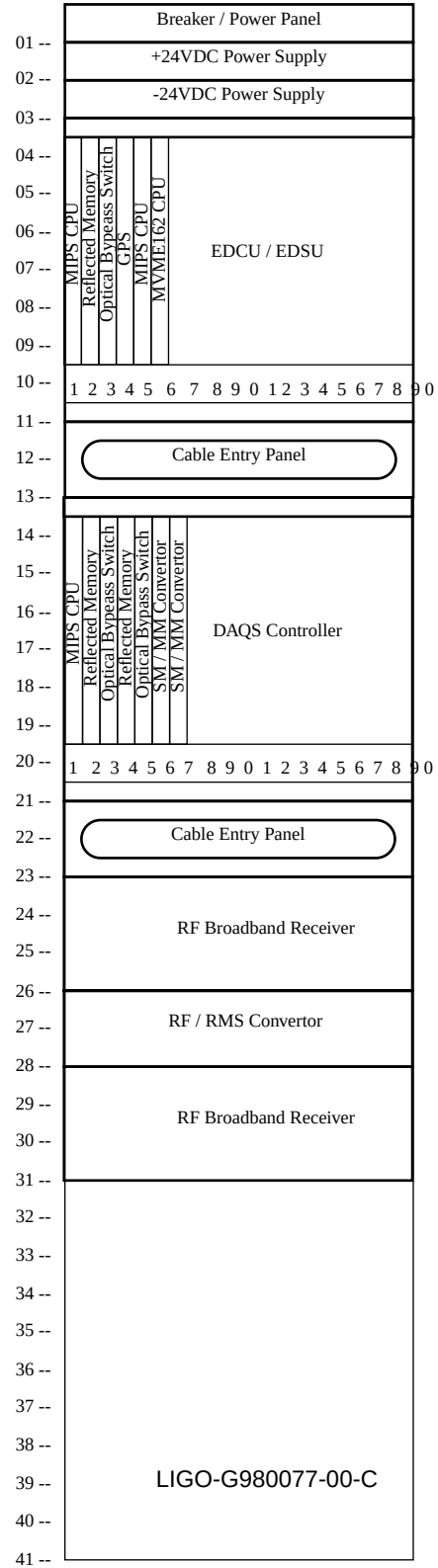
- Two MIPS processors (or MIPS + DSP)
- Decouple servo operation from DAQS/GDS to maximum extent ie servo must be able to operate without DAQS/GDS
- Servo systems use 2^n clocks from GPS to synch with DAQS/GDS



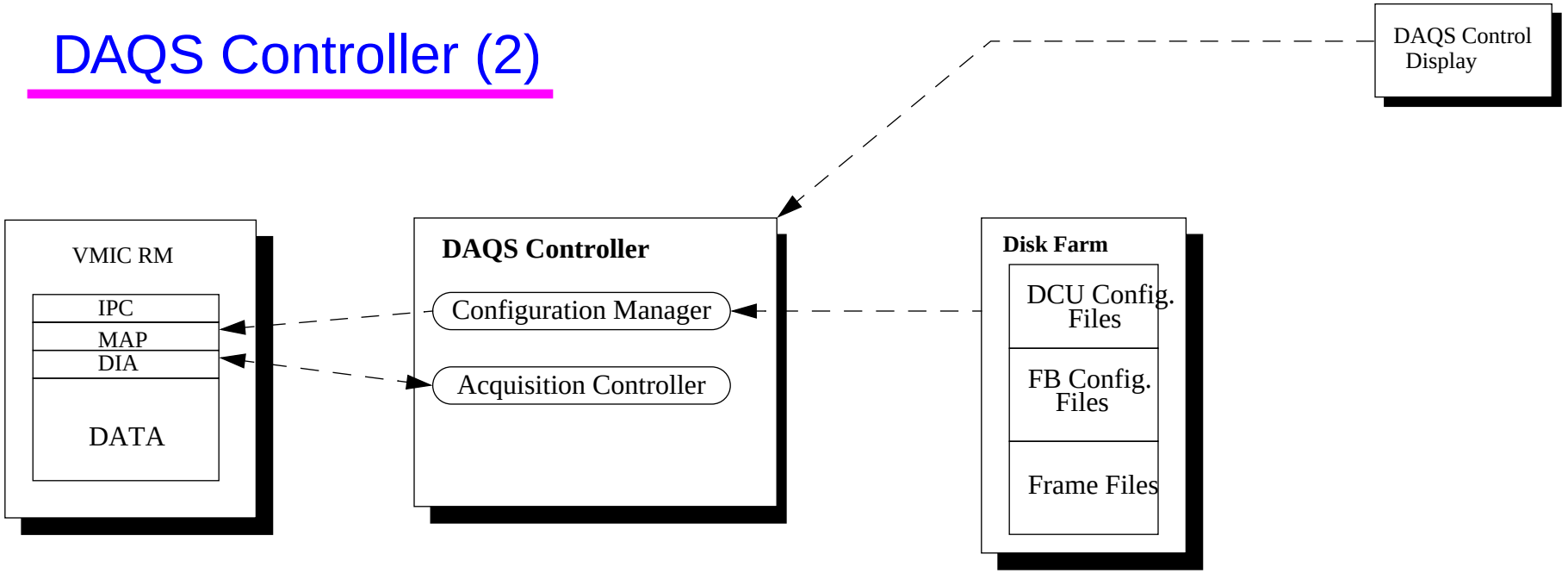
DAQS Controller (1)

- Configures and controls data acquisition via reflected memory
- From system configuration files, creates the MAP and DIA sections of reflected memory
- Verifies system integrety every 1/16 second
  - ›› All DCU responded w/data
  - ›› All DCU timing correct
  - ›› No system error messages
- Signals system processors when data is available





DAQS Controller (2)



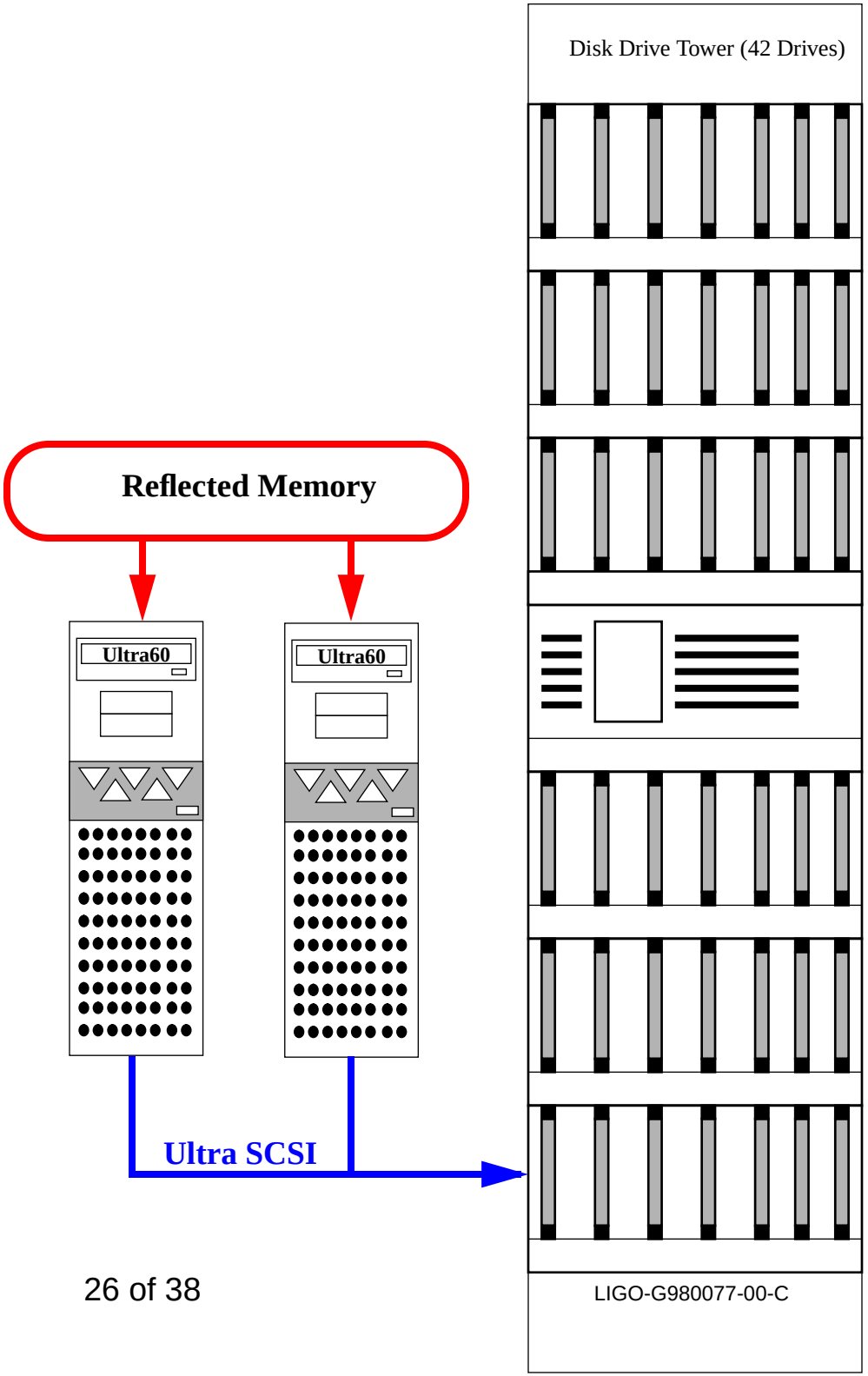
- Operator selects configuration file from browser.
- Operator selects load command.
- DAQS controller changes status in reflected memory, indicating that the MAP/DIA is undergoing changes (this is to flag new processes requesting information on reflected memory pointers that the system configuration is not valid).
- The MAP/DIA are changed to reflect the new data collection configuration.
- Commands are sent to all DCU that there is a new configuration pending.
- DCU search MAP/DIA for new configuration information and perform their setup routines to accomodate the new configuration. Each then sets their status to indicate when they are ready to comply.

DAQS Controller (3)

- Once DAQS controller receives ready indication from all DCU, it will command DCU to switch to new configuration on next 1Hz GPS pulse. It will also notify the frame-builders and other client tasks that they need to check the MAP/DIA for new data pointers.
- Note:
  - Data collection process is not suspended during a reconfiguration cycle. Each DCU still collects data in accordance with the previous configuration until such time as the controller commands them to switch to the new configuration.
  - DAQS controller does not change what data is being stored by the frames; in essence, the actual acquisition of data is independent from data storage.

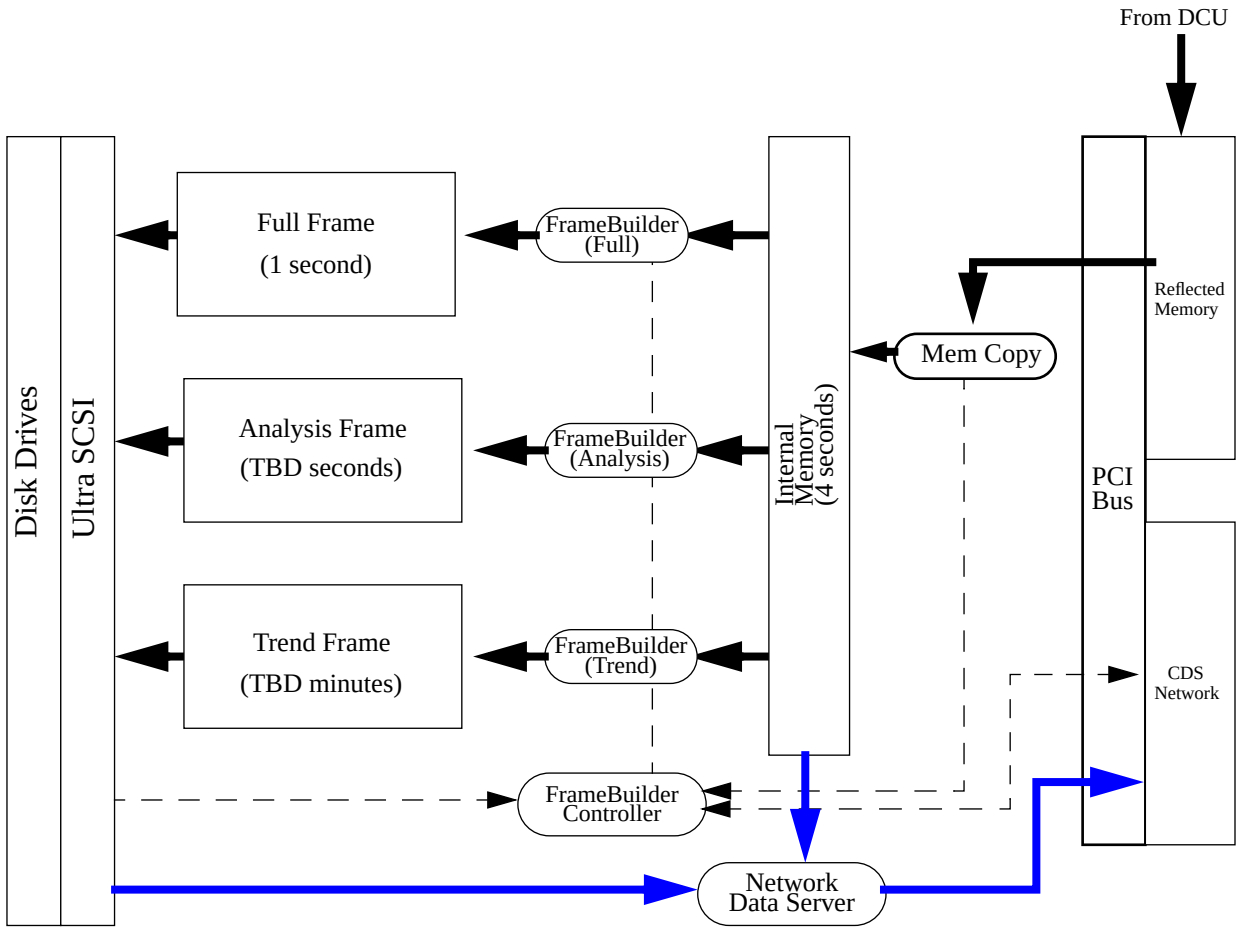
DAQS Server System

- Two Sparc Ultra 60
  - Two SparcIIi, 300MHz processors in each unit
  - 512MByte RAM
  - Two, 4MByte PCI Ref. Memory
  - ATM network interface
- RAID storage array
  - 42 Drive Slots
  - Minimum 372GByte (dependent on availability/price of 24G drives
  - 35MByte/sec transfer rates
  - 4 Ultra SCSI ports (2 DAQS / 2 LDAS)
- NOTE: LDAS will provide long term storage system



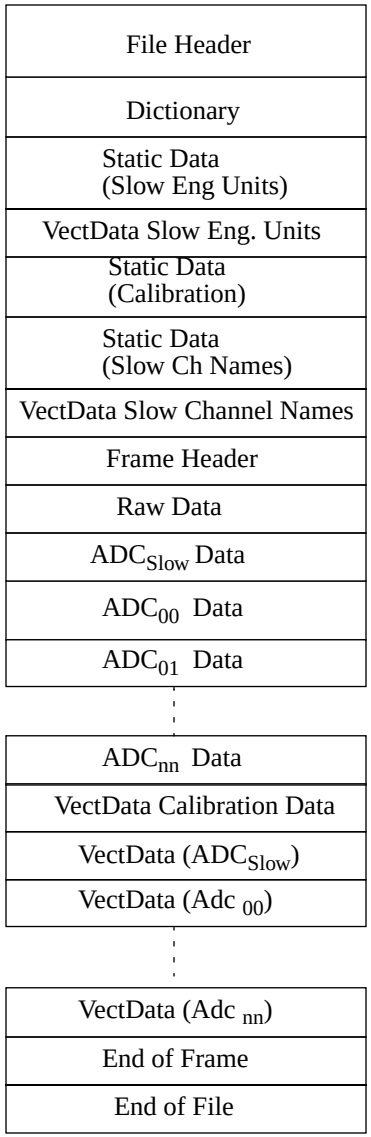
Server Software

- FrameBuilder Controller: Controls operation of the unit, including configuration information for the data to be stored.
- Mem Copy: This process, on interrupt from the DAQS controller each 1/16 second, copies data from the reflected memory into a larger (4 second) internal memory block.
- FrameBuilder (3): Performs the function of formatting the data into frames and storing that data to disk.

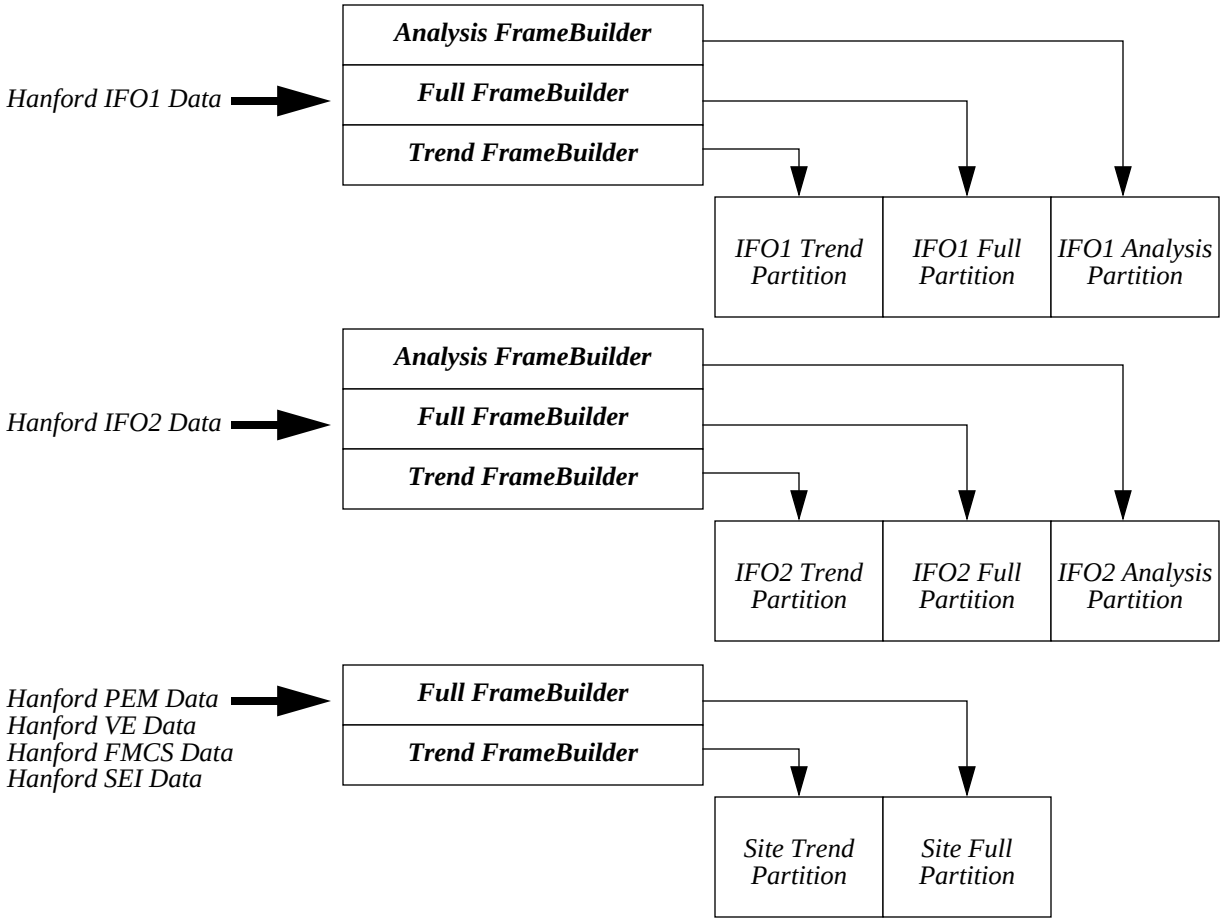


Frame Types and Structure

- Full Frame - contains any and all data neces-sary for on-line and off-line analysis of data
- Analysis Frame - contains set of data which is first to be processed by on-line LDAS
- Trend Frame - Contains statistics of each data channel at 1Hz + Slow Data
  - Max / Min value
  - Average value



Frame Processing / Storage



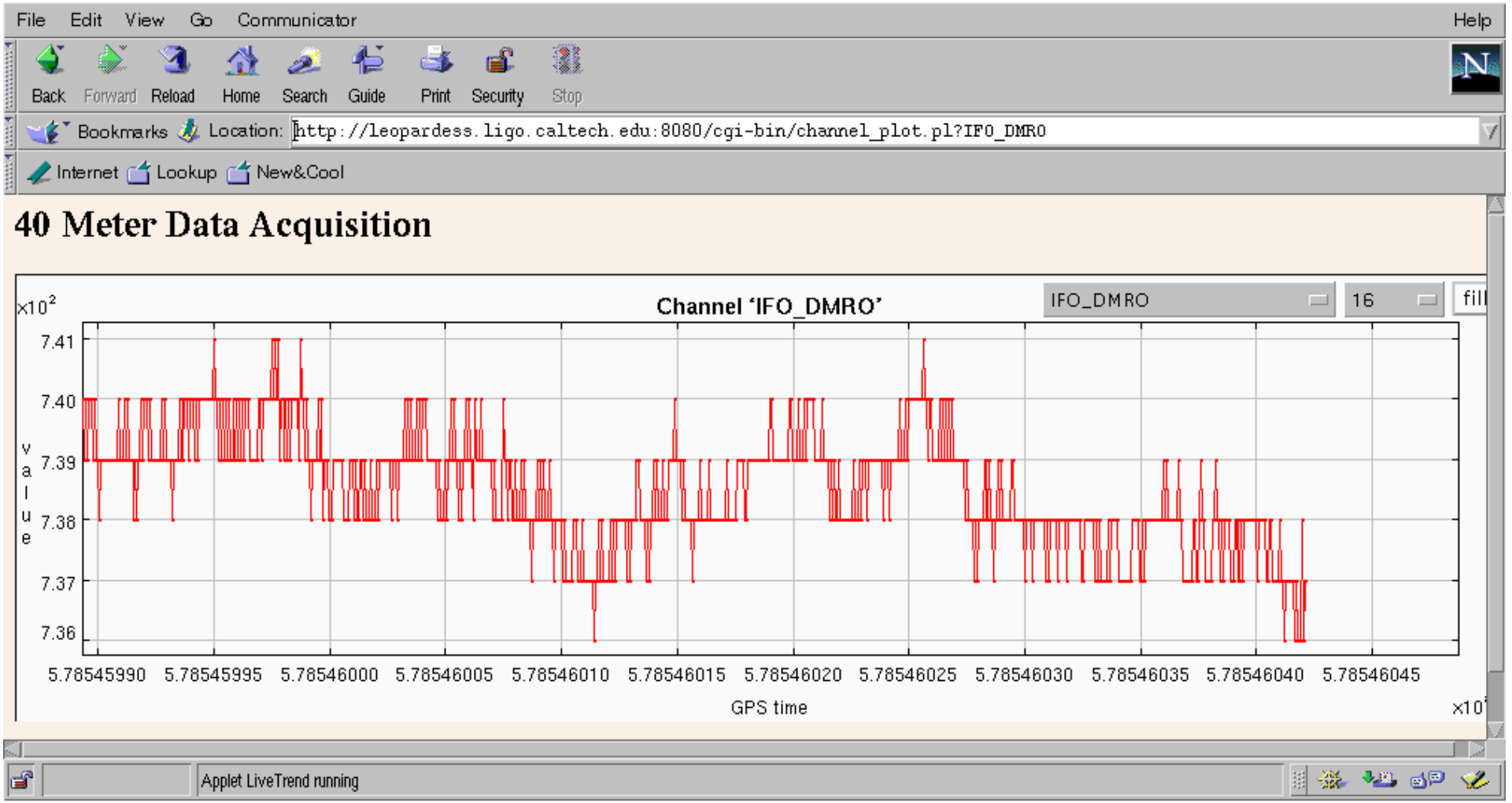
Data Servers

- Network Data Server
  - TCP/IP Server running on Ultra Sparc w/ATM connection
  - Real-time data updates at selectable rates to 16Hz
  - Selectable decimation
  - Data by time frame from disk (Long playback)
  - API library provided (to be reviewed w/GDS May 27)
  - Presently operational on 40m prototype
- EPICS Data Server Unit (EDSU)
  - Single MIPS processor w/access to reflected memory and CDS networks
  - Reads GDS flags / triggers and formats them to EPICS records
  - Allows use of EPICS alarm manager software for user interface

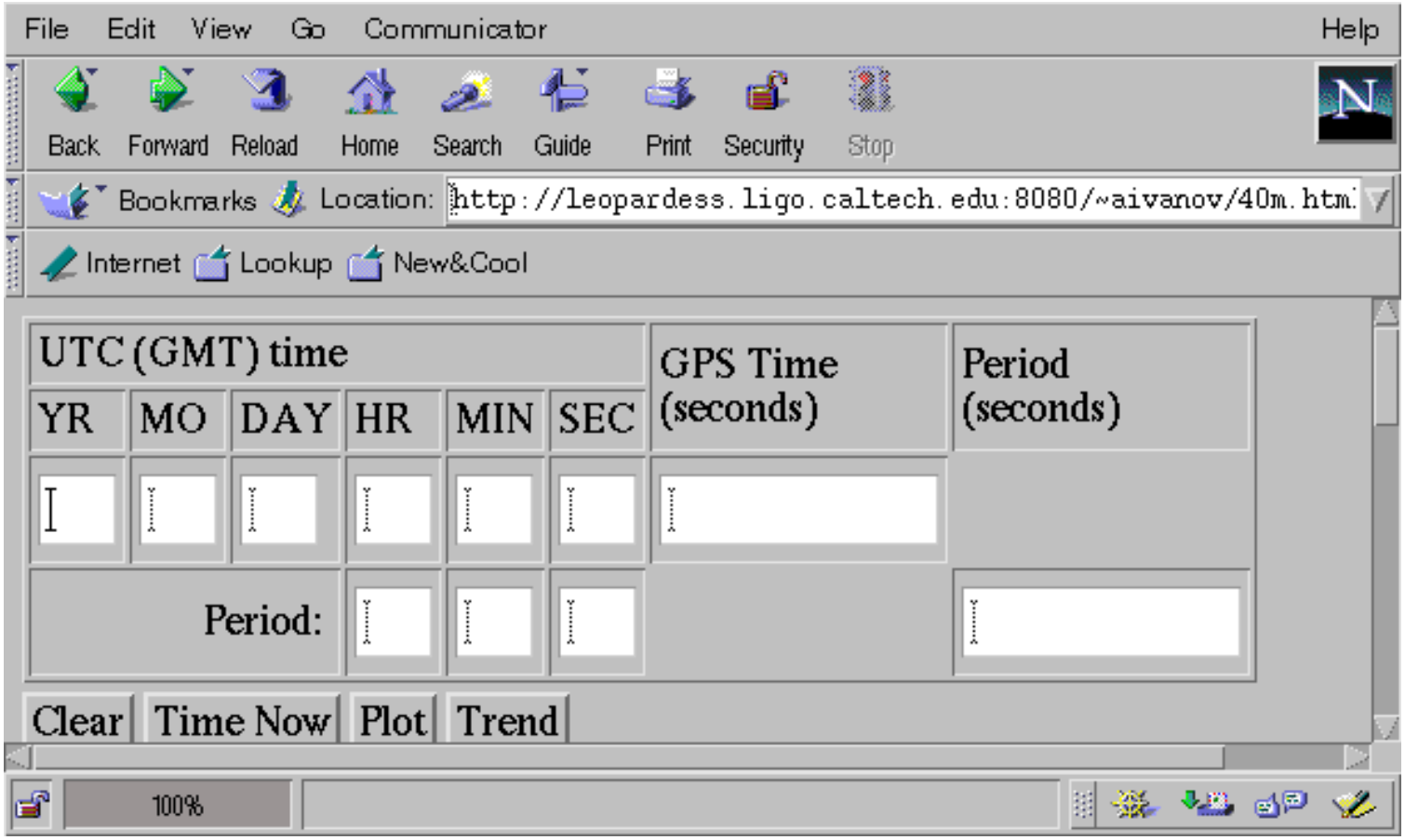
User Interface Software

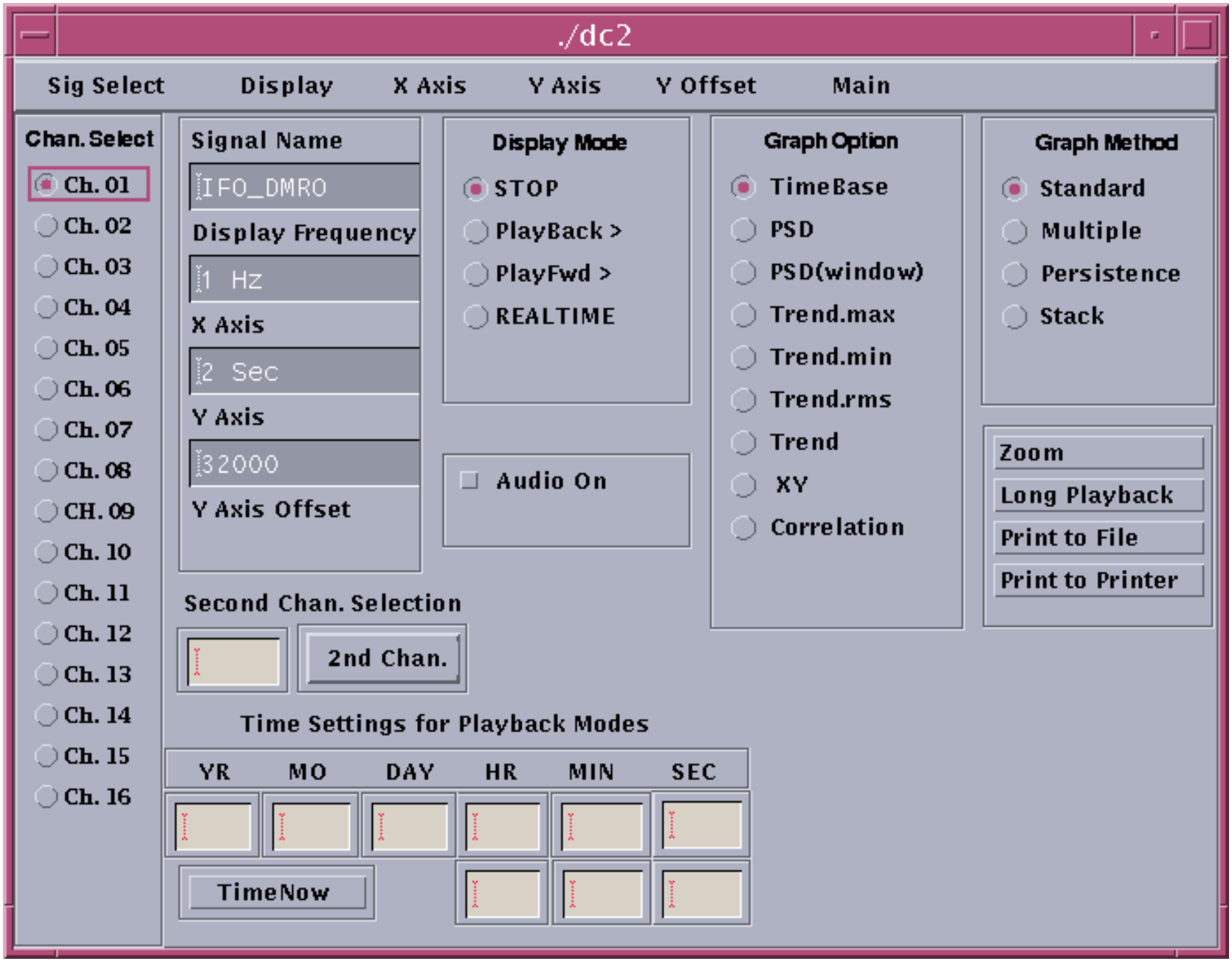
- System configuration, control and status
  - Code written in Java for display in Java-enabled web browsers
  - Sun Java Server will be used for connections
- Real-time and Stored Data Display
  - Limited performance via Java and web browser
  - Real-time performance via Xmgr (present prototype) and/or XRT Graph; being developed to meet the requirements as set in the GDS design document

Prototype Java Live Data Display



Prototype Java Data Playback Screen

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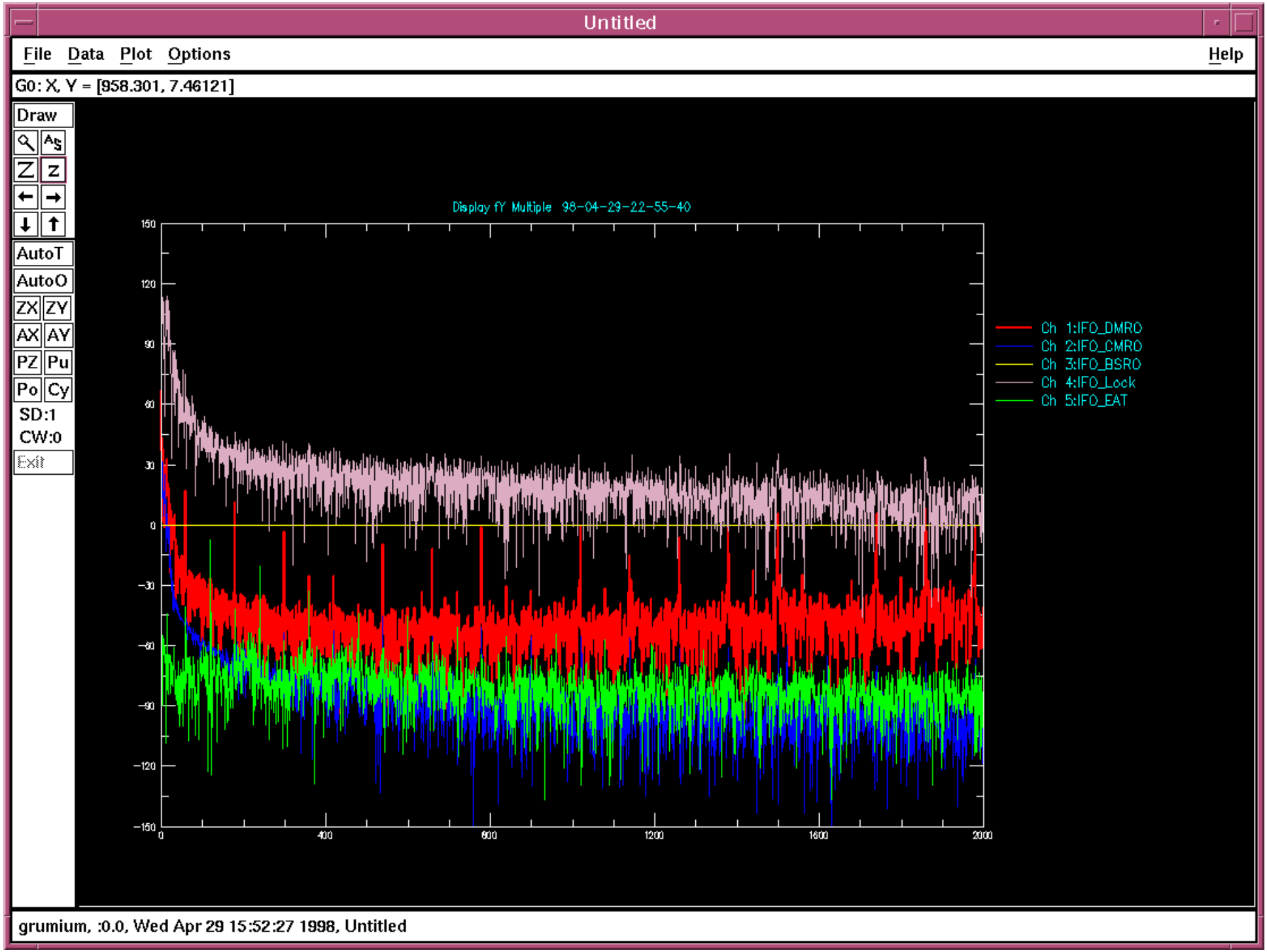
Sig Select
Display
X Axis
Y Axis
Y Offset
Main
Chan. Select
Ch. 01
Ch. 02
Ch. 03
Ch. 04
Ch. 05
Ch. 06
Ch. 07
Ch. 08
CH. 09
Ch. 10
Ch. 11
Ch. 12
Ch. 13
Ch. 14
Ch. 15
Ch. 16
Signal Name
IFO_DMRO
Display Frequency
1 Hz
X Axis
2 Sec
Y Axis
32000
Y Axis Offset
Display Mode
STOP
PlayBack >
PlayFwd >
REALTIME
Audio On
Graph Option
TimeBase
PSD
PSD(window)
Trend.max
Trend.min
Trend.rms
Trend
XY
Correlation
Graph Method
Standard
Multiple
Persistence
Stack
Zoom
Long Playback
Print to File
Print to Printer
Second Chan. Selection
2nd Chan.
Time Settings for Playback Modes
YR
MO
DAY
HR
MIN
SEC
TimeNow


Untitled
File Data Plot Options
Help
G0: X, Y = [958.301, 7.46121]
Draw
AutoT
AutoO
ZX ZY
AX AY
PZ Pu
Po Cy
SD:1
CW:0
Exit
Display fY Multiple 98-04-29-22-55-40
Ch 1:IFO_DMRO
Ch 2:IFO_CMRO
Ch 3:IFO_BSRO
Ch 4:IFO_Lock
Ch 5:IFO_EAT
150
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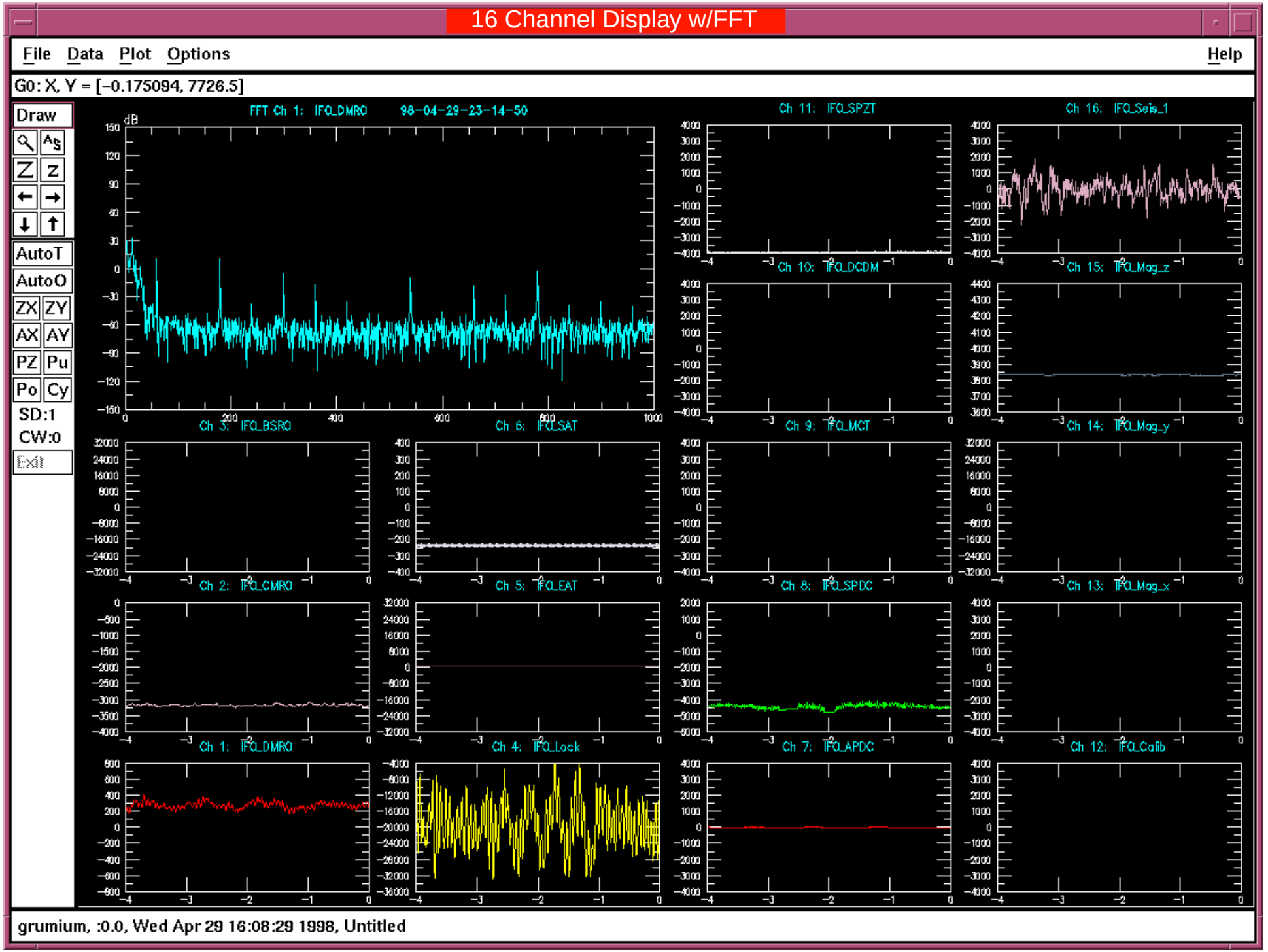
16 Channel Display w/FFT



DAQS Cost Estimate

DAQS Subsystem	*Location*	*Cost*
Hanford DAQS / PEM		
H4KDAQS1 & H4KDAQS2	LVEA	$137,950
H4KDAQS3	Right End	$50,850
H4KDAQS4	Left End	$50,850
H2KDAQS1	LVEA	$55,350
H2KDAQS2 & 3	LVEA	$121,950
H2KDAQS4	Right Mid	$50,850
H2KDAQS5	Left Mid	$50,850
DAQS Cntrl / EDCU / EDSU	OSB MSR	$74,250
Server System	OSB MSR	$157,770
LSC/ASC support	LVEA	$57,600
HPEM1 & HPEM-2	LVEA	$140,850
Hanford DAQS/PEM EAC		**$949,120**
Hanford DAQS/PEM Baseline		$1,125,000
Hanford Baseline - EAC		$175,880

DAQS Subsystem	*Location*	*Cost*
Livingston DAQS / PEM		
L4KDAQS1 & 2	LVEA	$137,950
L4KDAQS3	Right End	$50,850
L4KDAQS4	Left End	$50,850
DAQS Cntrl / EDCU / EDSU	OSB MSR	$57,450
Server System	OSB MSR	$157,770
LSC/ASC Support	LVEA	$28,800
LPEM-1	LVEA	$76,850
Livingston DAQS/PEM EAC		**$560,520**
Livingston DAQS/PEM Baseline		$723,700
Livingston Baseline - EAC		$163,180

Schedule

- Phase 1A - Data Collection (Hanford 6/19/98)
  - ADCU
  - DAQS Controller
  - Reflected Memory setup and API
  - EPICS DCU
- Phase 1B - Data Storage, Distribution, Display (Caltech 6/19/98)
  - Framebuilders
  - Sun Reflected Memory
  - Java based user interfaces for system control/monitoring
- Phase 2 - System Integration (Hanford 7/1/98 to 8/31/98)
  - Final software development for Rev. 1 system based on integration testing
  - Initial interface connections with GDS
- Phase 3 - Hanford DAQS Installation (8/1/98 to 11/1/98)
  - All server equipment and basic infrastructure installed by end of August
  - Modular design allows system to be installed / commissioned in sections
- Phase 4 - Livingston DAQS Installation (2/1/99 to 5/1/99)