LIGO – Hanford

Timing Distribution System

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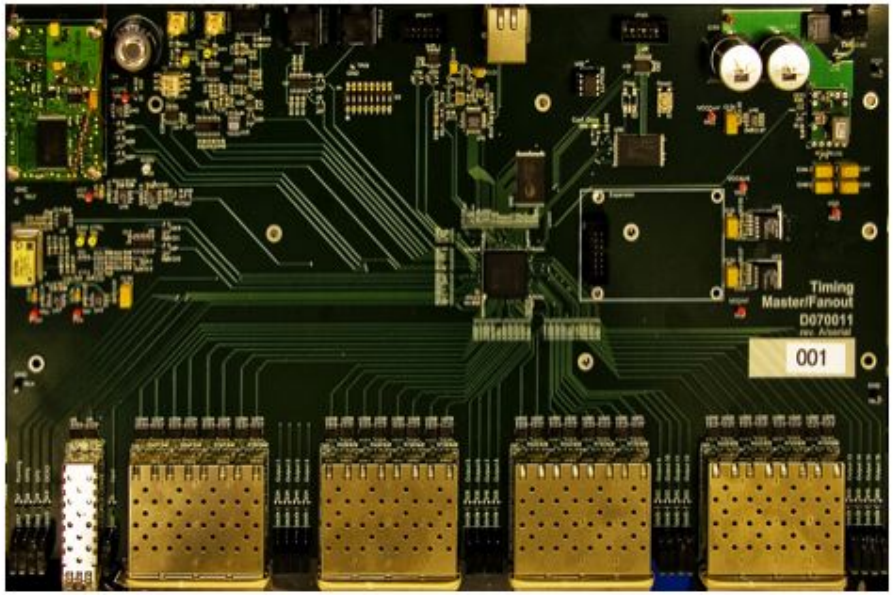

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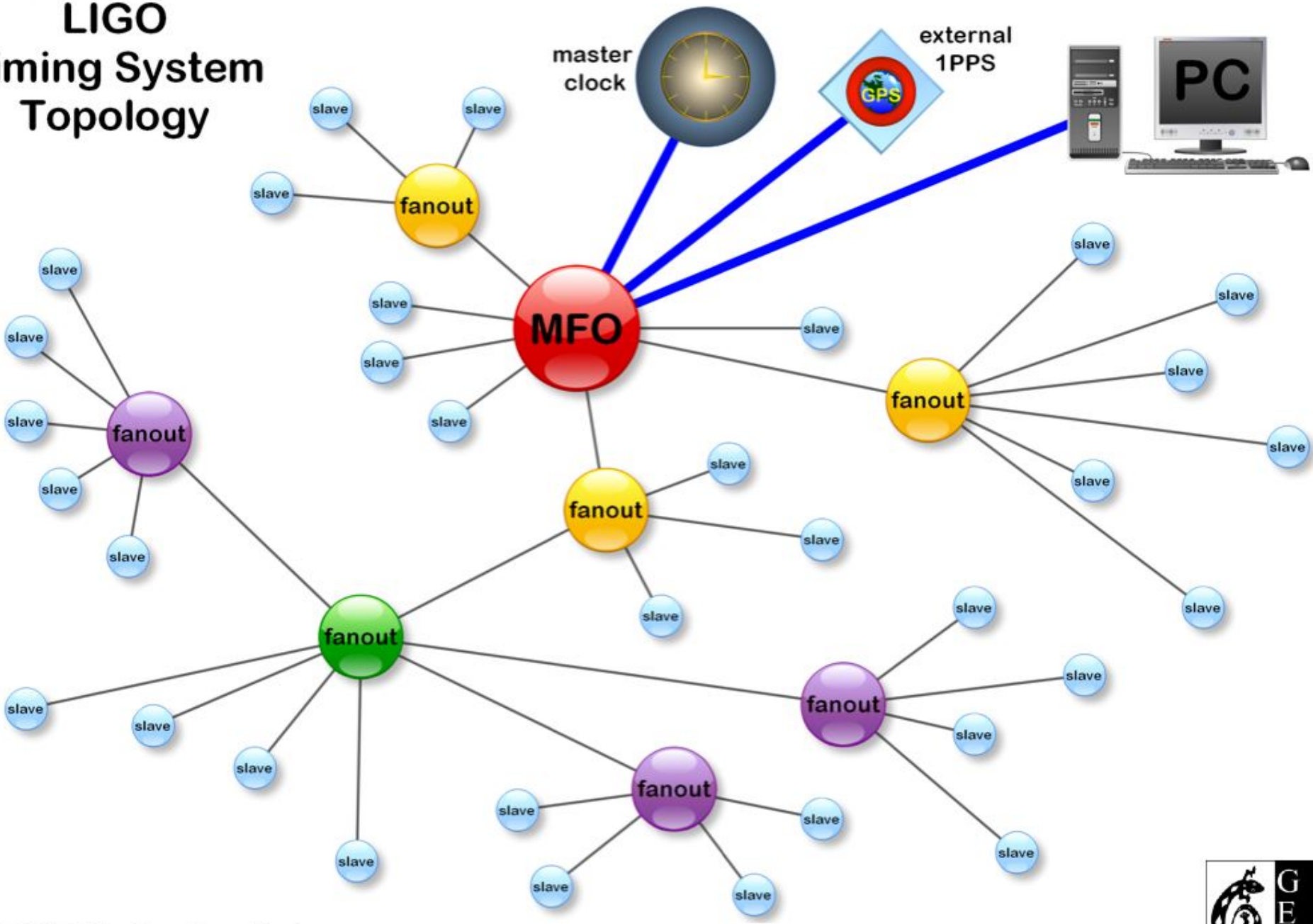
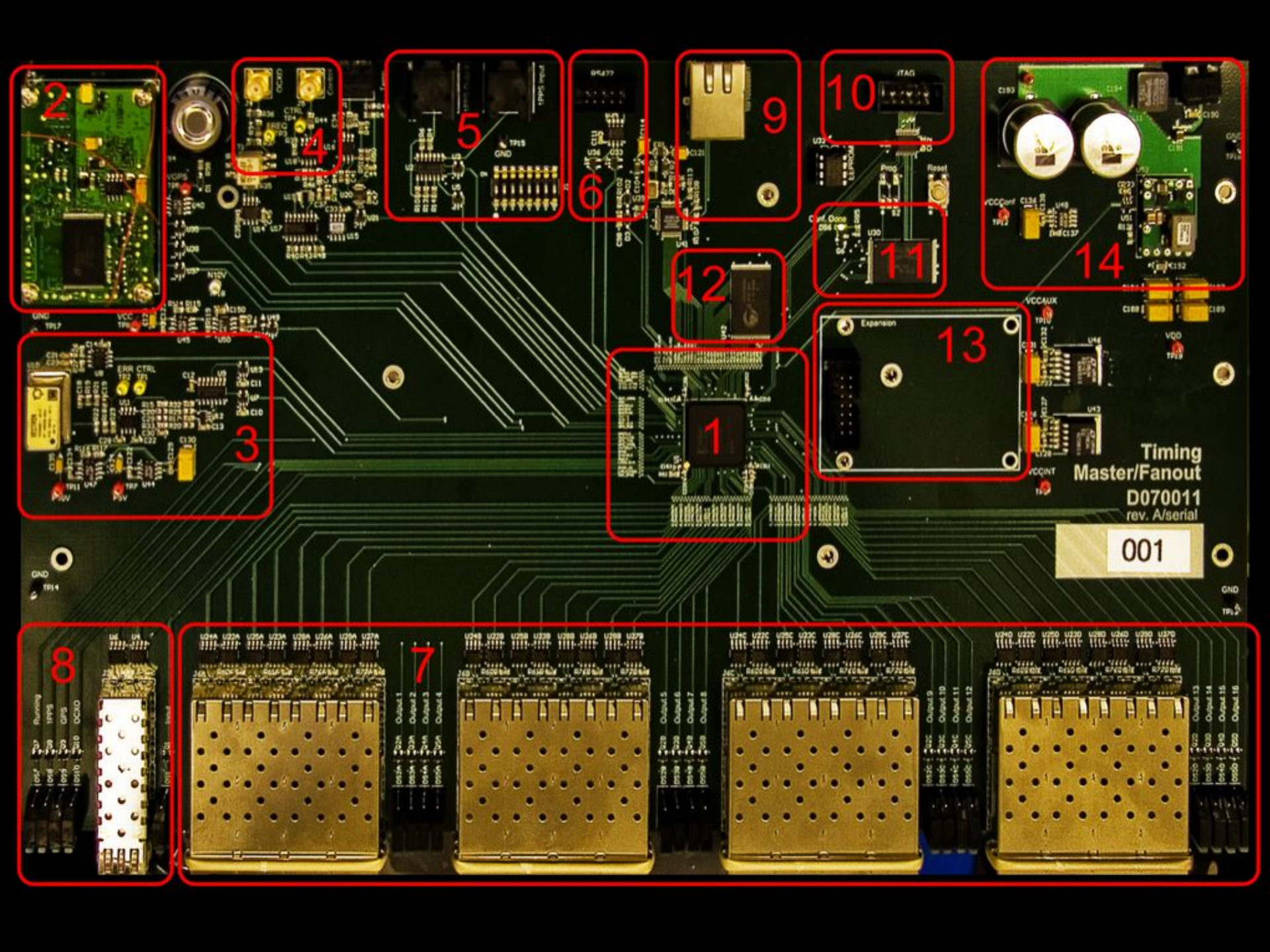
LIGO

LIGO Timing System Topology



*MFO ≡ Master Fan-Out


1
2
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Timing
Master/Fanout
D070011
rev. A/serial
001

LIGO

- Main Goal:
  - To achieve overall synchronization with better than 1μs uncertainty
- Secondary Goals:
  - To distribute complete timing information (GPS second count)
  - To develop a “generic” data transfer protocol and be able to communicate between the networking units

*Note: hot-swapping must be allowed

Primary Synchronization

1 – the MFO uses phase-locking loop (PLL) to lock the phase of the internal voltage-controlled oscillator VCO to the master clock.

2 – the VCO then has exactly 2^{26} cycles per second

3 – the VCO is used to generate 2^{23}Hz signal (down by factor of 8) this signal gets transmitted through the fanout channels

4 – the unit on the other end reads this signal and synchronized to it its VCO frequency and phase.

5 – the remote unit regenerates the 2^{23}Hz and sends it further downstream

6 – eventually the entire network gets synchronized to the master clock, except for the phase shift due to the propagation delays

Secondary Synchronization

1 – the MFO starts sending out the 1PPS packet

2 – the first receiver synchronizes *its own* 1PPS counter to the packet received from the MFO

3 – the receiver starts sending back to the MFO its *own* generated 1PPS packets

4 – the MFO calculates the time interval between sending the 1PPS and receiving it back

5 – this interval equals to the double-magnitude of the propagation delay

6 – the MFO then advances the 1PPS packets ahead of time, for the half-interval in (5)

7 – the receiver checks for simultaneity of incoming and outgoing 1PPS packets; once it fails, an error is registered

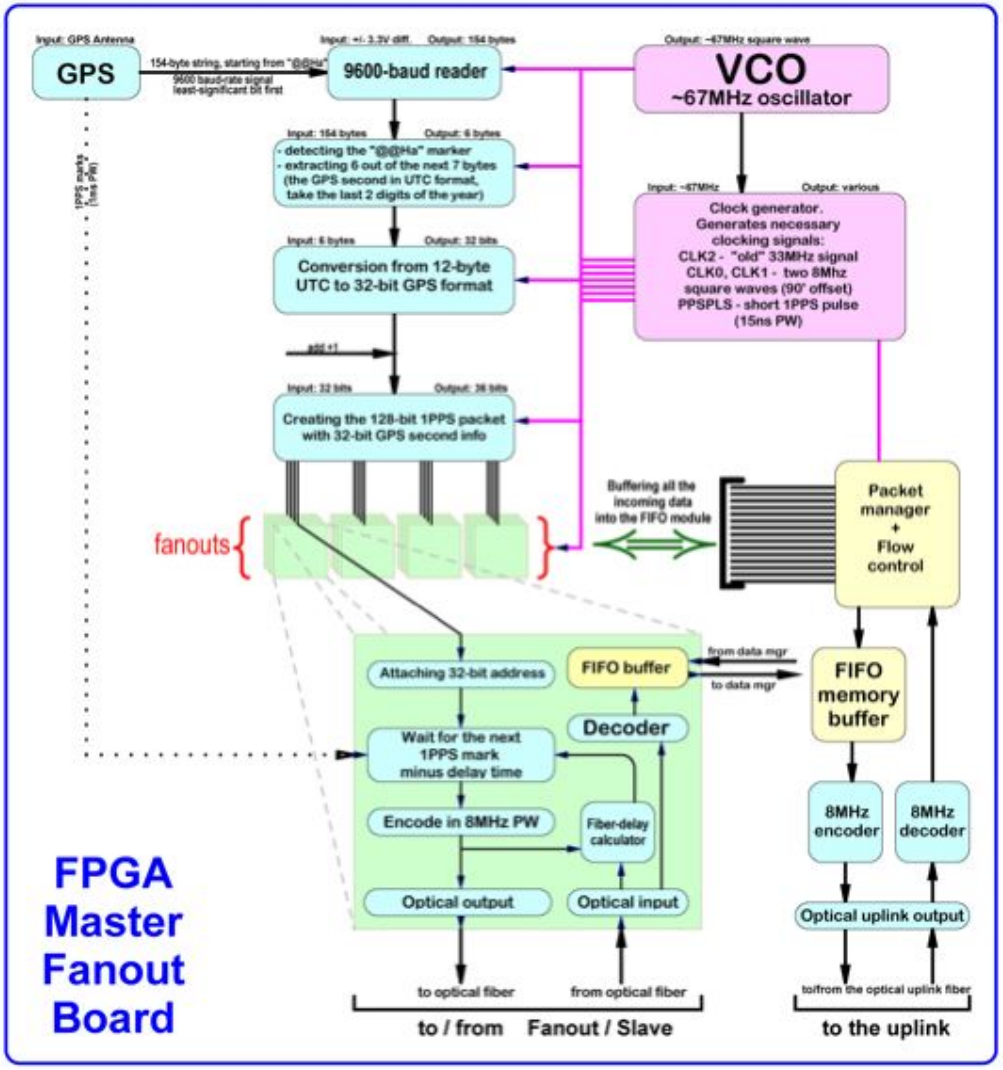
8 – the receiver gets resynchronized once it encounters a series of 8 consecutive sync errors

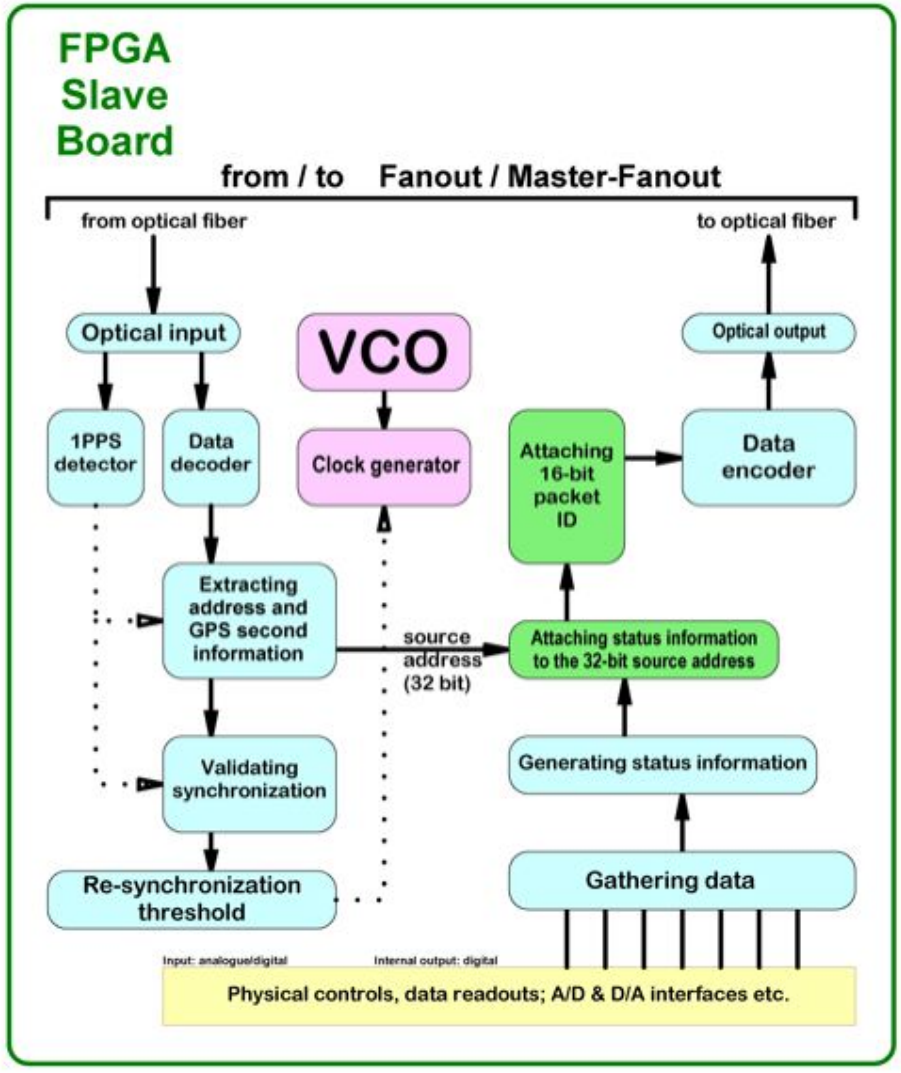
9 – eventually, all propagation delays become adjusted for as well

Final synchronization – GPS-second

- Problem:
  - The time is counted by the # of VCO cycles since the beginning of the current second
  - The count is reset every second
  - E.g., events separated by exactly 1s will be “stamped” with the same counter value
- Solution:
  - Every second the GPS receiver sends out complete date, time and position
  - The MFO reads it, extracts the GPS-second info, converts it (if necessary) to the standard 32-bit GPS format, inserts the 32-bit GPS-second into the 1PPS packet and sends it downstream
  - Once the network absorbs the GPS-second, every 14.5ns time interval is assigned a unique 64-bit time-stamp.

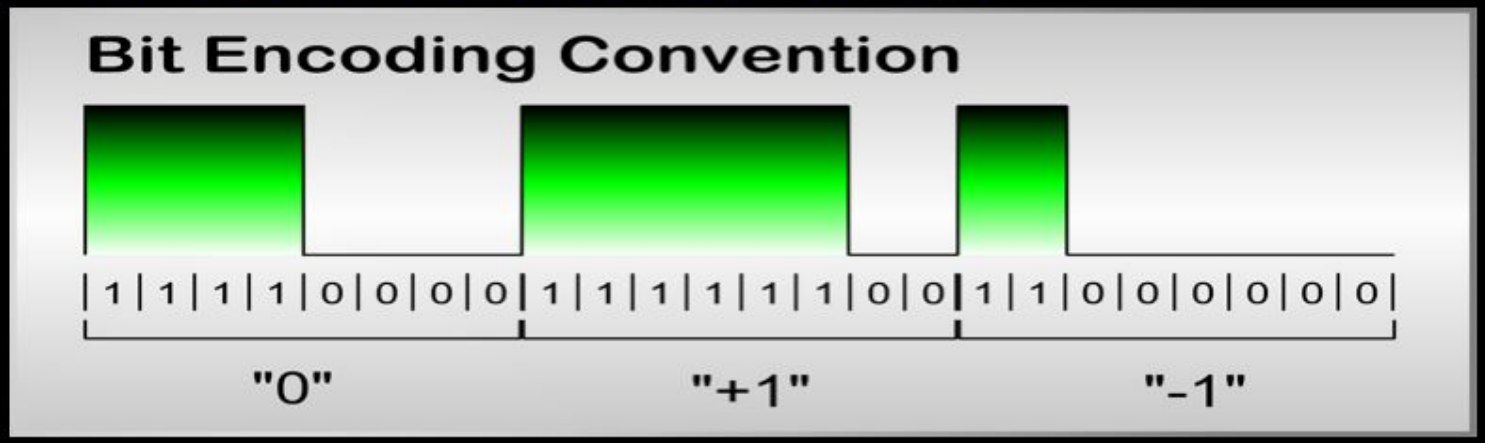
Process flow: Fanouts and Slaves

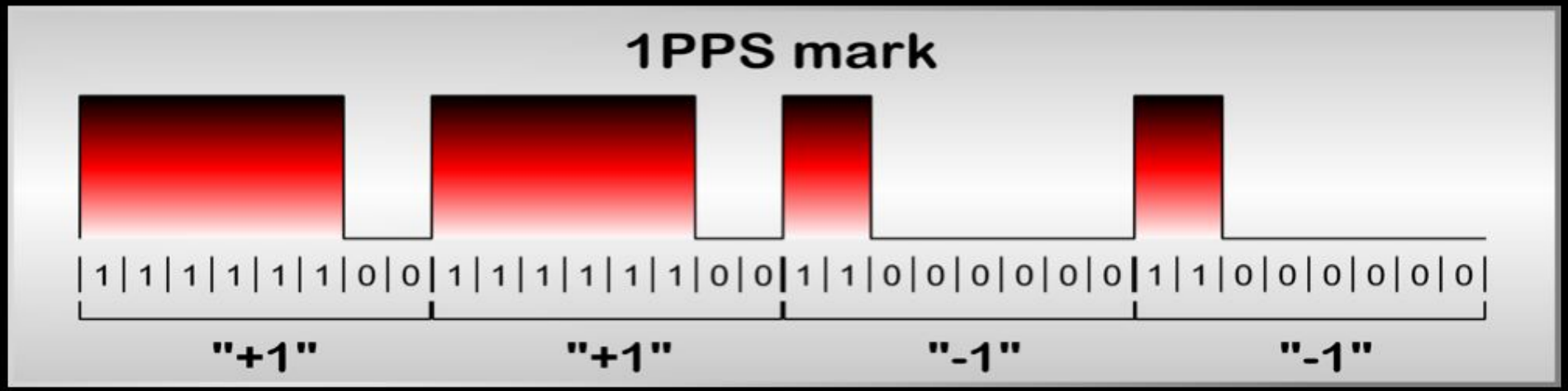




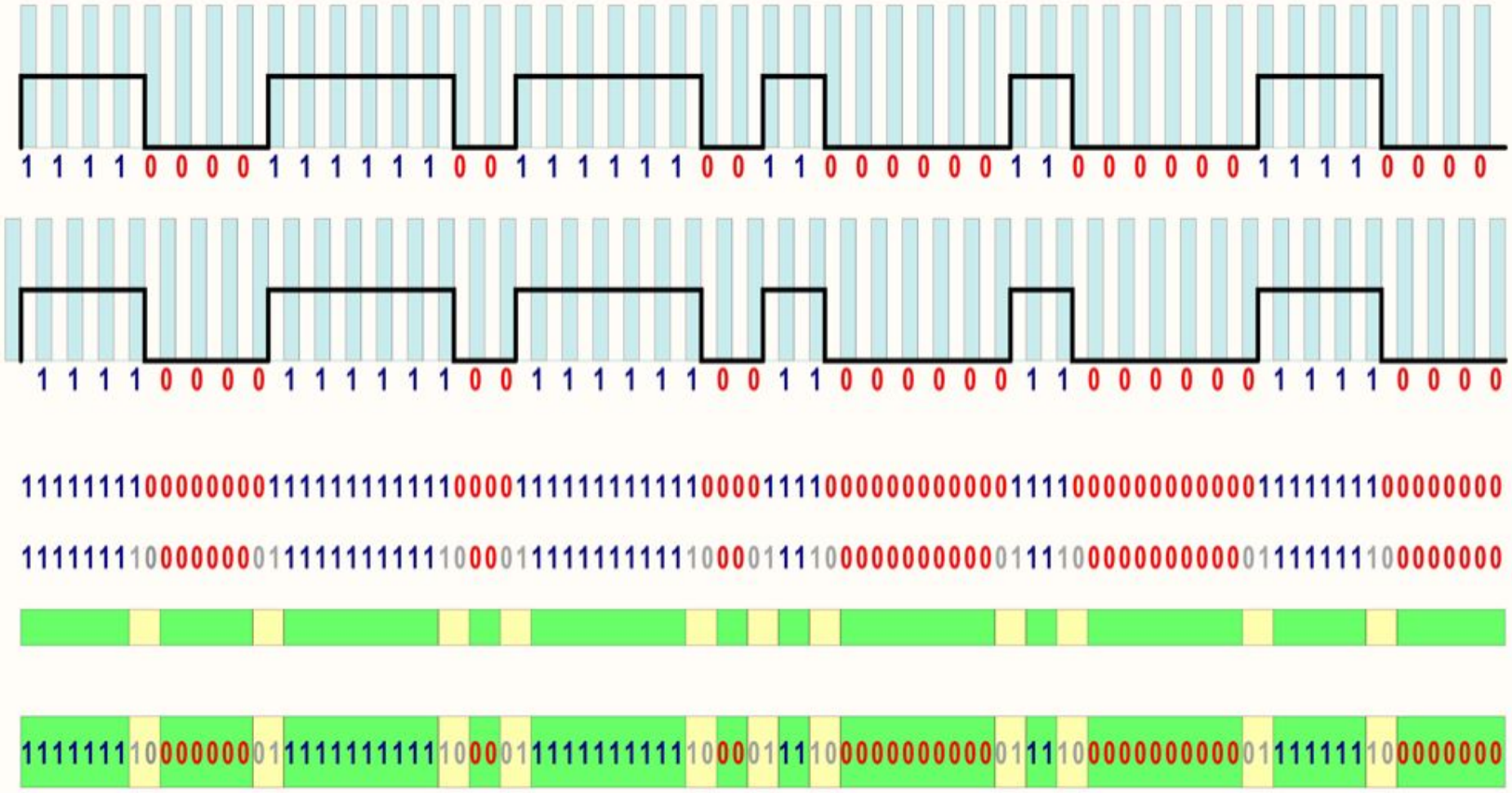
Encoding Conventions

- Positive edges are used for phase-locking the VCO to the master-clock, and hence unmovable
- Negative edges can be shifted to encode binary values
- The DC-balance must be preserved





Decoding the data



- Must allow for the signal jitter
- Must account for the logic setup time
- It is best to use both clock edges, to achieve the oversampling ratio of 16

Time Slots

- Assuming, there are no synchronization errors:
  - Every second VCO has exactly 67,108,864 cycles
  - It is equivalent 8,388,608 bits of data, based on oversampling ratio of 8
- We agree to send data in packets
- We also agree to have fixed packet length of 128 bits
- 65,536 consecutive packets will occupy the whole second interval

➔ therefore, it is convenient to subdivide each second into 2^{16} = 65,536 time-slots, counted from -1 to 65,534

- The 0^{th} time-slot starts at the beginning of each second
- A packet can only be sent within a time-slot; the 1PPS packet occupies the -1^{st} slot

Data packets

***Convention: Most Significant Bit first (is the year 2007 or 7002?)

Standard data packet

128 bits total

- Bit 127 – the flow control bit
- Bits 126..124 – 3-bit address offset
- Bits 123..96 – 28-bit address
- Bits 95..32 – 64-bit "payload"
- Bits 31..16 – 16-bit packet identifier
- Bits 15..0 – 16-bit CRC checksum

1PPS packet

128 bits total

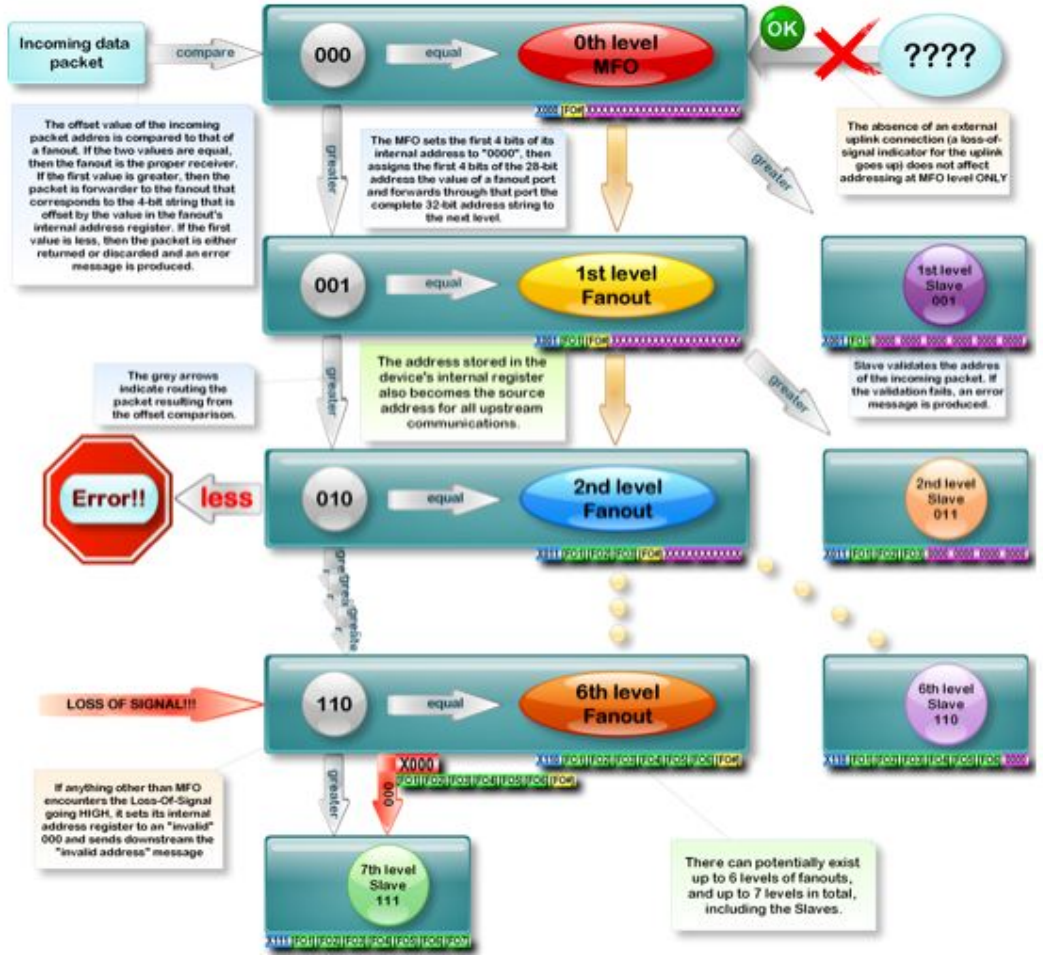
- Bit 127 – the flow control bit
- Bits 126..124 – 3-bit address offset
- Bits 123..96 – 28-bit address
- Bits 95..64 – 32-bit GPS second
- Bits 63..32 – unused
- Bits 31..28 – 4-bit 1PPS marker
- Bits 27..16 – unused
- Bits 15..0 – 16-bit CRC checksum

Dynamic Address Recovery

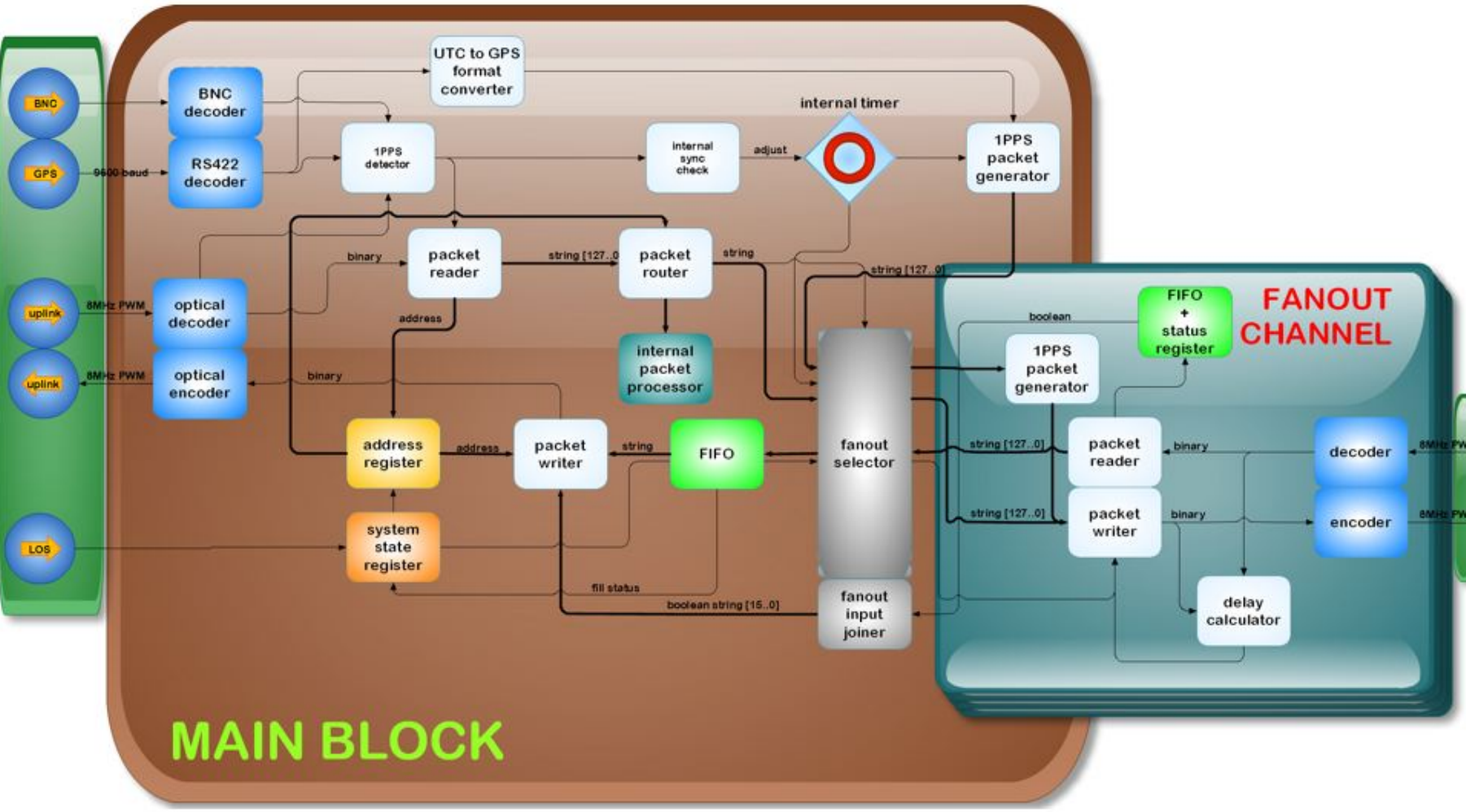
32-bit address double-word

	offset 0..7	address block 1	address block 2	address block 3	address block 4	address block 5	address block 6	address block 7

Offset, binary	Offset, decimal	Bits Modified
000	0	None (MFO) or Invalid!!
001	1	27..24
010	2	23..20
011	3	19..16
100	4	15..12
101	5	11..8
110	6	7..4
111	7	3..0



Master / Fanout Board



- Main block – logic that has only single implementation and is shared by all I/Os. Contains all common functions.
- Fanout channel – there are 16 identical replicas of the same logic. Each is used exclusively by single fanout I/O channel.

- end -