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Electronics Infrastructure for advanced LIGO

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G070491-00-D

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Outline

- **Converter Design**
  - Commercial baseline: Currently runs the prototypes
  - New design: Low noise ADC/DAC/uplink boards
- **Timing System** (with U of Columbia)
  - New design based on fiber distribution/FPGA
- **Power Supplies**
  - Baseline: 48VDC distribution with local voltage regulators
- EMI Plan (Huh?)
- Thermal Management
  - Possibility for water cooling
- Slow Controls
  - Epics based, no VME based systems

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Some Basic Design Guidelines

- Digital controls whenever possible
  - X86 architecture for controls; No VME
- Stay with the current software infrastructure as much as possible
  - Online digital filter code
  - Frame builder & archival code
  - Diagnostics and DMT software
- No change in slow controls interface, i.e., EPICS
  - No VME; maybe no dedicated slow controls hardware
- In-vacuum detection benches

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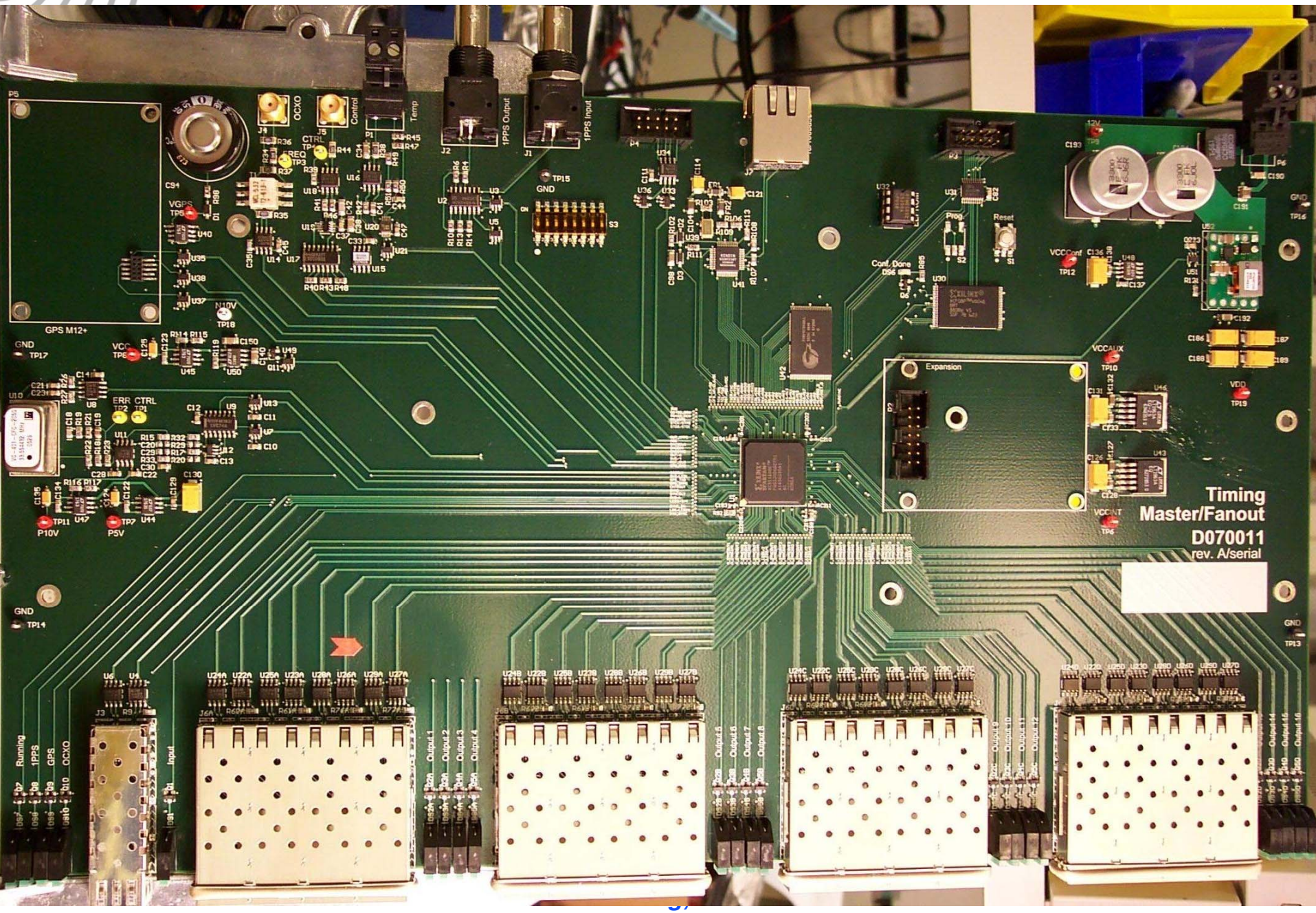
Timing System

- *"The ability to reconstruct the arrival time of a gravitational wave signal with infinite signal-to-noise ratio shall be within 10 μs of UTC."*
- Distribution
  - Fiber based; bidirectional links for diagnostics and status
  - Timing derived from GPS
  - Master/fanout units & Slave units
  - Full timestamp to ADC/DAC
- Atomic clock
  - Separate system for diagnostics
  - Time-interval counters in each building
- DuoTone
  - (Two) sine waves for time encoding in data stream
  - Hardware locking for DAC


Timing
Master/Fanout
D070011
rev. A/serial
GPS M12+
Expansion
Reset
Prog.
Conf. Done
OCXO
Control
Temp
1PPS Output
1PPS Input
Running
1PPS
GPS
OCXO
Input
Output 1
Output 2
Output 3
Output 4
Output 5
Output 6
Output 7
Output 8
Output 9
Output 10
Output 11
Output 12
Output 13
Output 14
Output 15
Output 16

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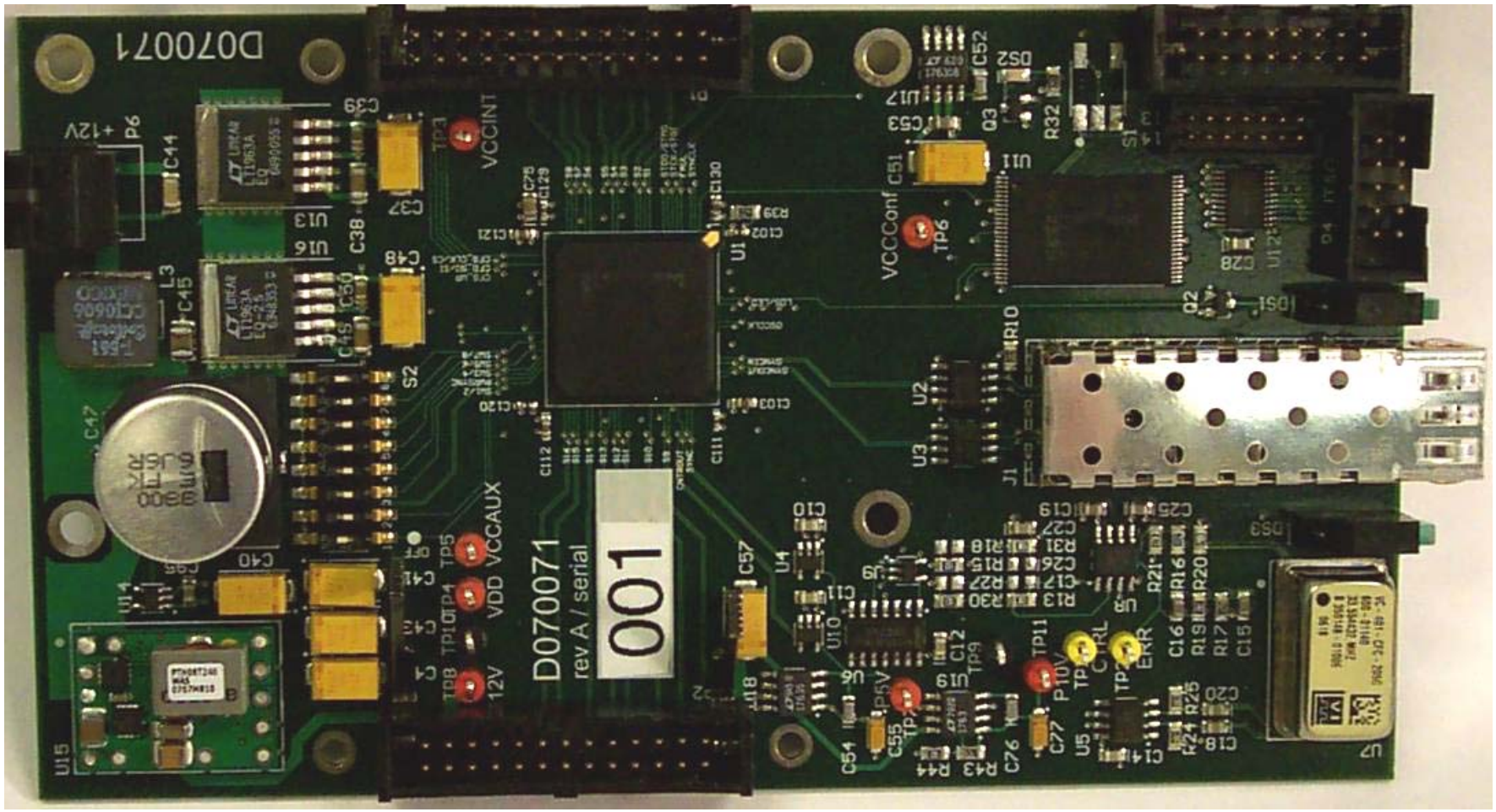
Timing Slave (6” x 3.5”)



Converter Design
Features we like to address (I)

- Co-location of analog and digital
  - New design uses fiber links between computer and converter
    - PCI-E for commercial
    - Gigabit ethernet for in-house design
  - All computers in mass storage room and out of LVEA
- Poor noise performance
  - Use over-sampling
  - Better analog input circuits and cleaner power supplies
- Limited Timing Support
  - Ideally samples are time stamped at front-end
  - Timing accuracy should be guaranteed in hardware

Converter Design
Features we like to address (II)

- Inadequate throughput
  - Eliminate the VME backplane
  - Replace with PCI-E or dedicated serial link (gigE)
- Convoluted data paths
  - No reflective memory
  - Myrinet/10GE switched network between computers
- High costs
  - Better with PCI-E & in-house

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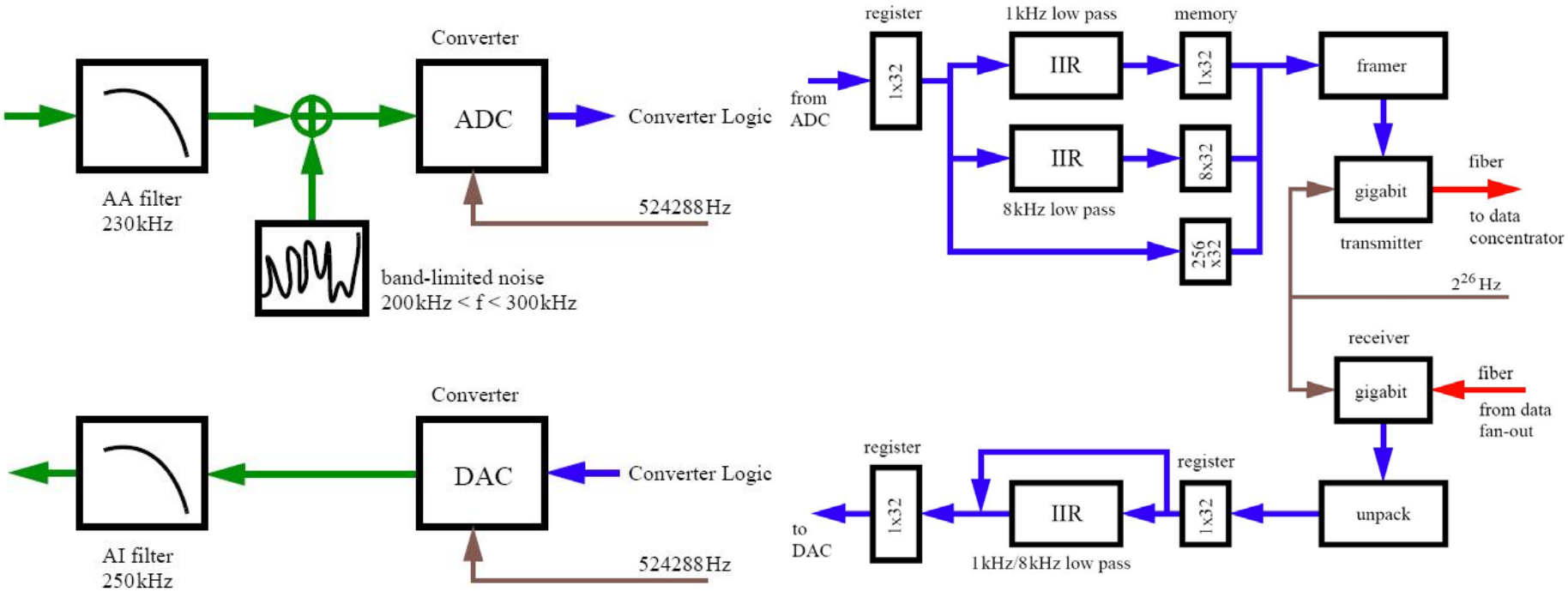
Basic Requirements for In-House Development

- Absolute timing precision relative to UTC: 1μs
- Converter range: ±10V
- Converter noise: 100–300nV/√Hz (best effort)
- Latency between converter and processor: < 5μs
- No restriction on converter location
- No electrical connection between converters and processors (fiber links)
- Detection of transmission and timing errors
- Support for diagnostics

Converter Design Diagram



- Use an FPGA to implement a digital IIR filter

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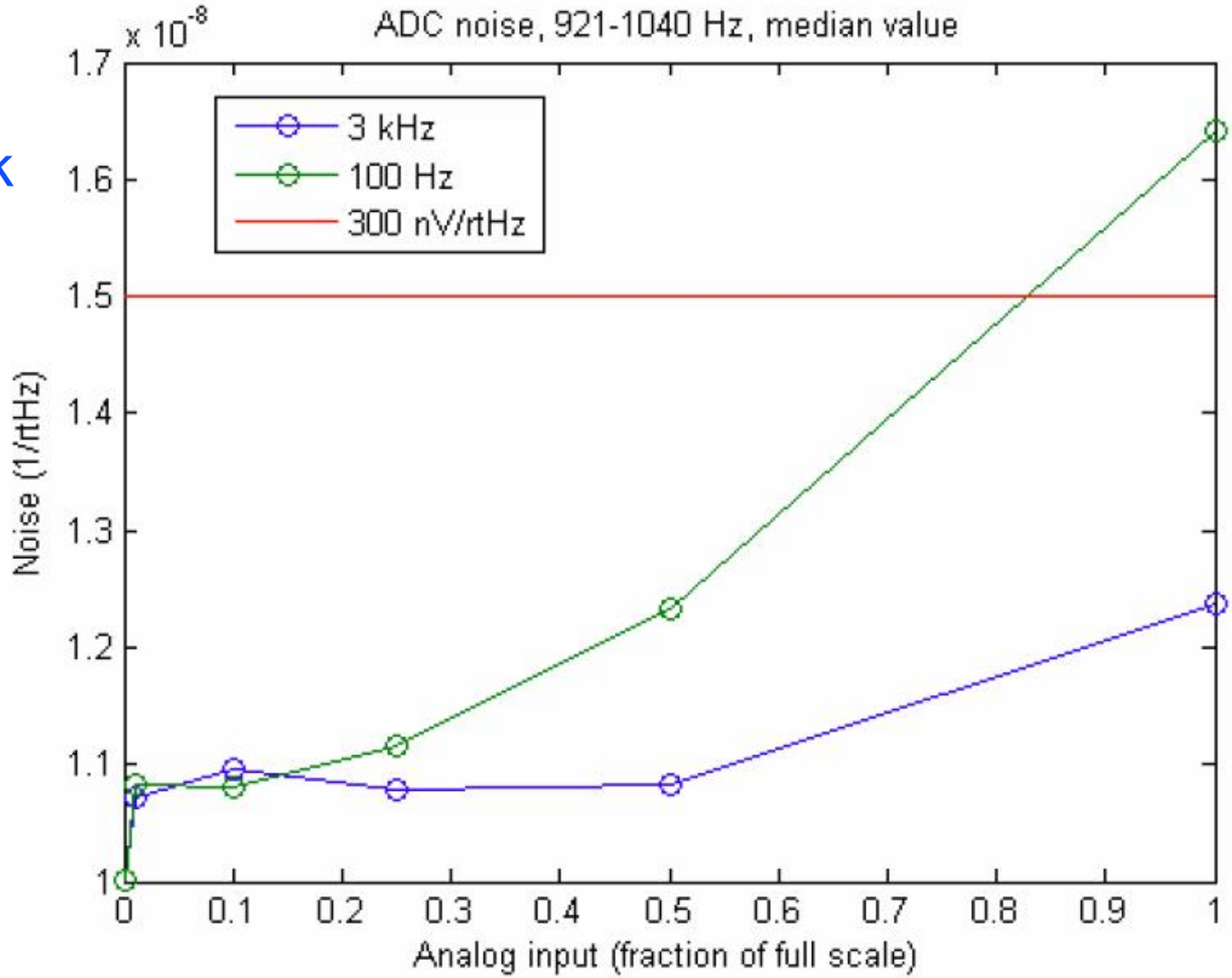
Converter Design
Results from Test Board

- ~35x better than Pentek
- Known problems with reference voltage



Converter Design
New Boards

- 16 channels
- 6U x 280mm eurocrate form factor
- Differential signaling to uplink board (LVDS)
- ADC: Analog Devices AD7634
  - Fabricated and in testing
- DAC: Texas Instruments (Burr-Brown) PCM1794A
  - Design finished
- Uplink for single converter board
  - In design phase
  - Xilinx Virtex 4 FX series (most likely)

Ch. 1
Ch. 2
Ch. 3
Ch. 4
Ch. 5
Ch. 6
Ch. 7
Ch. 8
Ch. 9
Ch. 10
Ch. 11
Ch. 12
Ch. 13
Ch. 14
Ch. 15
Ch. 16
J1
J2
DV1
DGND
+3.3V
DGND
+5V
GND
+15V
GND
-15V
GND
GND
GND
GND
+AV3
-AV3
+AV2
-AV2
+AV1
C53
LIGO PROJECT
ADC Test Board
D060535
Rev B-
S/N:

Converter Design Summary

- Oversampling to achieve better noise performance
  - Interface with computer at 16kHz or slower
- IIR filter in FPGA works down to 16 kHz
  - SURF student working on a higher precision implementation
- Final AA filter is now in digital domain
  - Only limited analog low pass filtering at 200kHz required
  - Same for anti-image filtering
- Much larger dynamic range
  - may make switchable whitening and dewhitening obsolete or at least reduce its requirements

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Power Supplies

- Avoid 110V/60Hz in the (L)VEAs
- 48VDC power bus
- Regulation to intermediate voltages in rack
  - ±6.5V, ±16.5V, ±24V (analog systems) and +12V (digital systems)
  - Synchronous switchers locked to GPS
  - High frequency switchers with filtering
  - Backup: DC supplies
- Final regulation on board
  - Low drop-out low noise linear regulators
  - Noise Eater
  - Synchronous point-of-load regulators for digital systems

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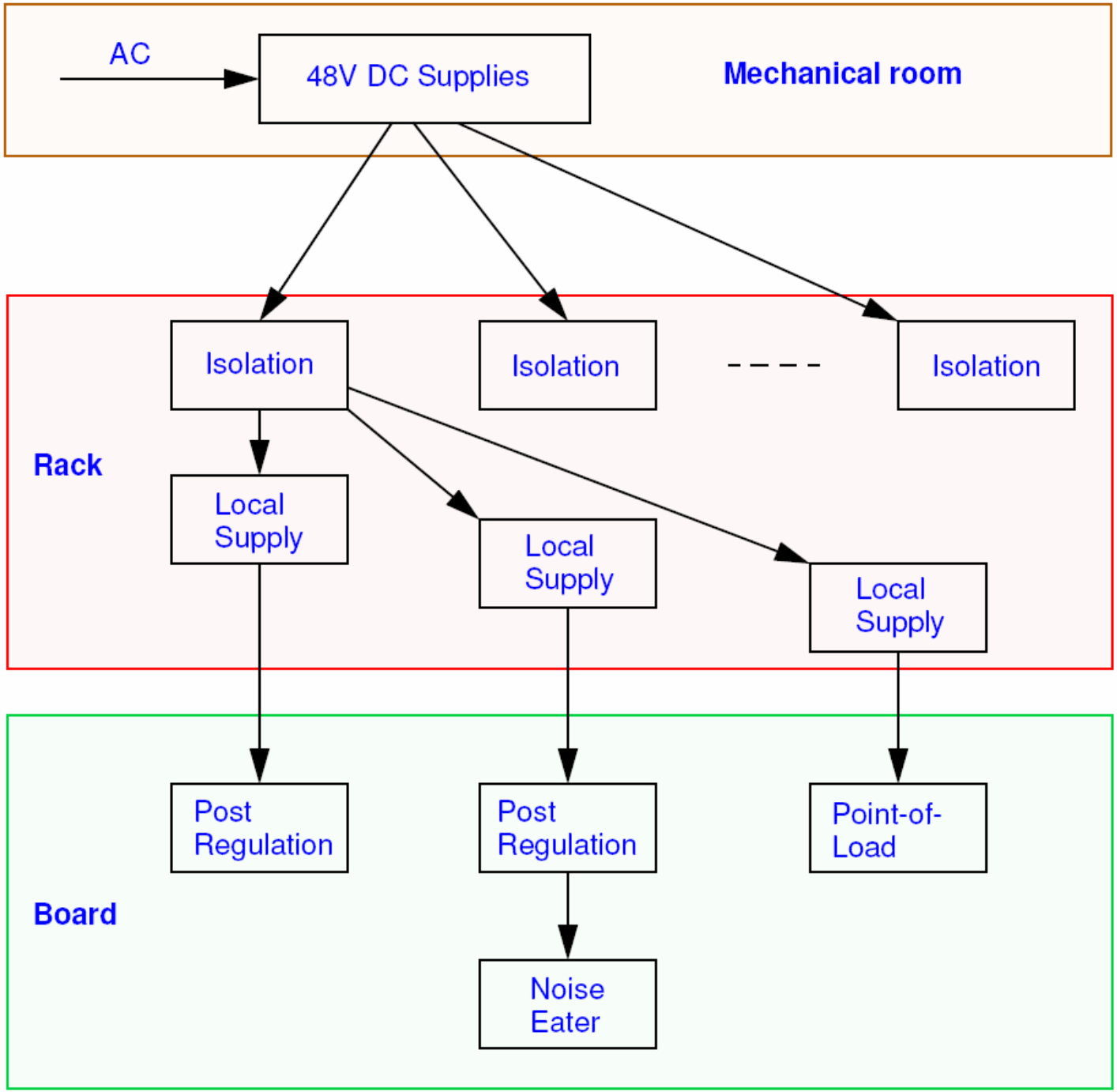
No 60Hz

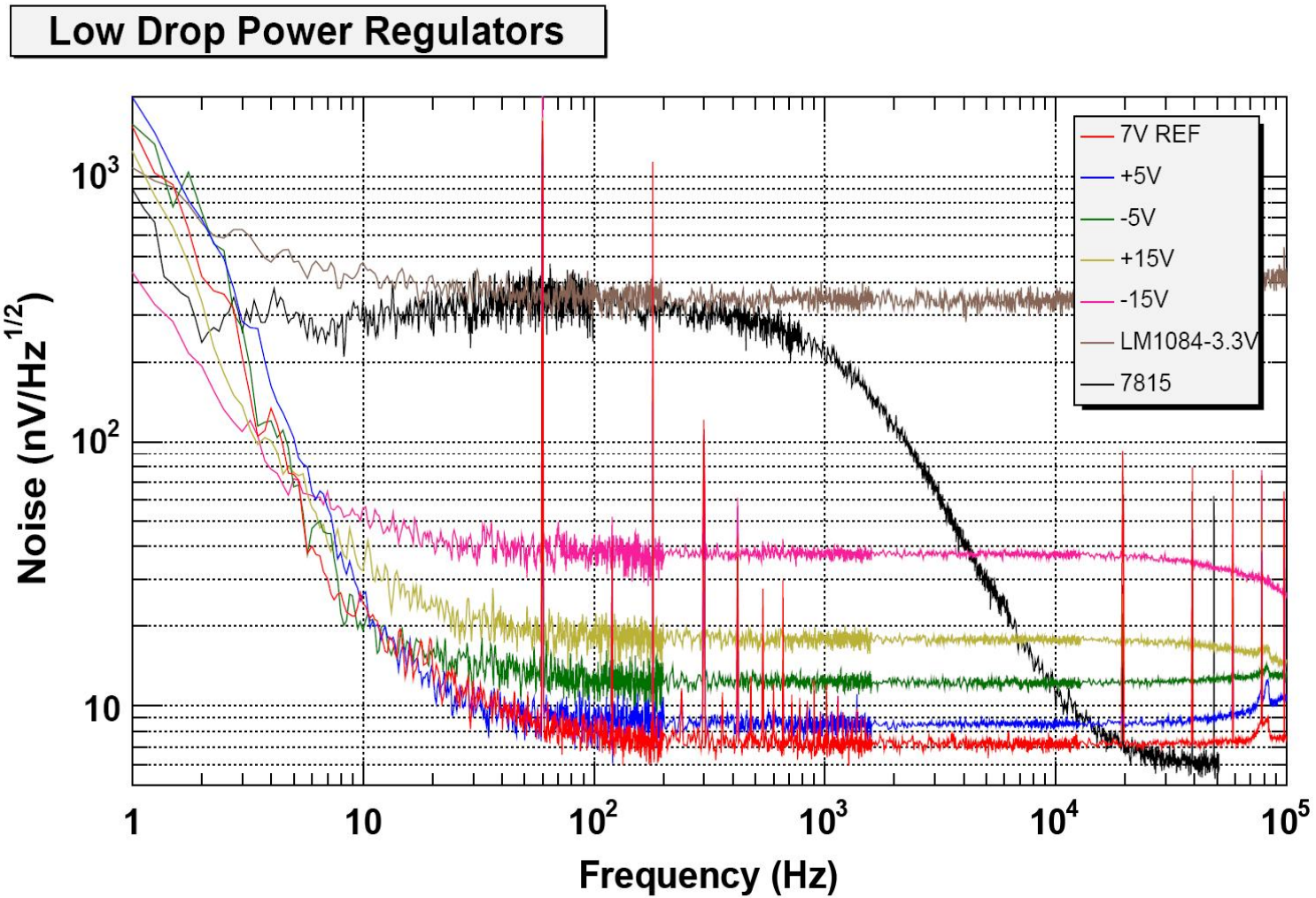
Water cooling



Linear Post Regulation

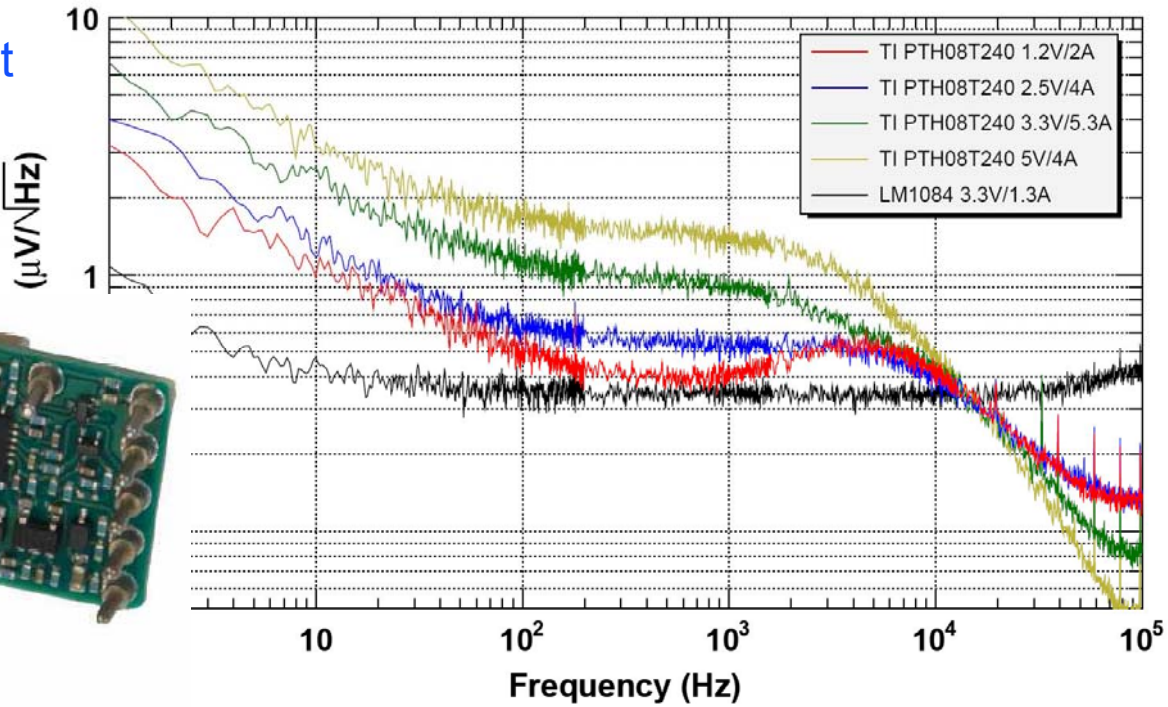
~10x lower noise

~160mV voltage drop at 1A



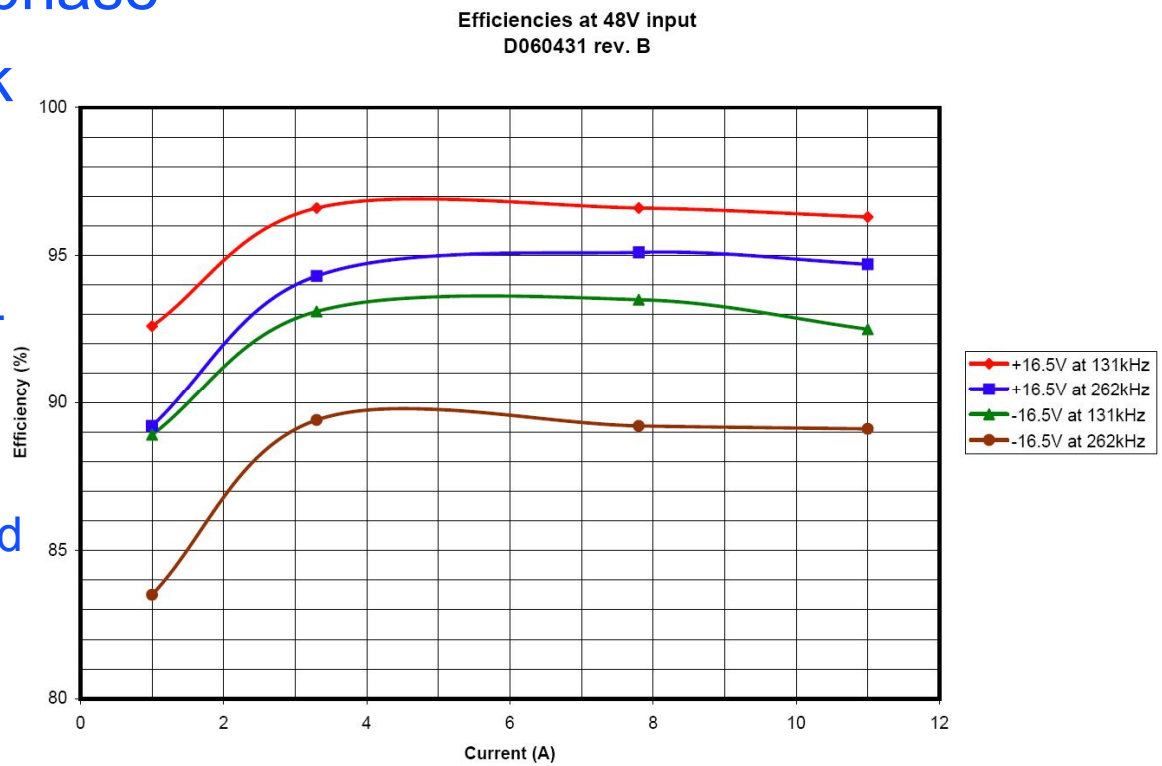
Point-of-Load Regulation

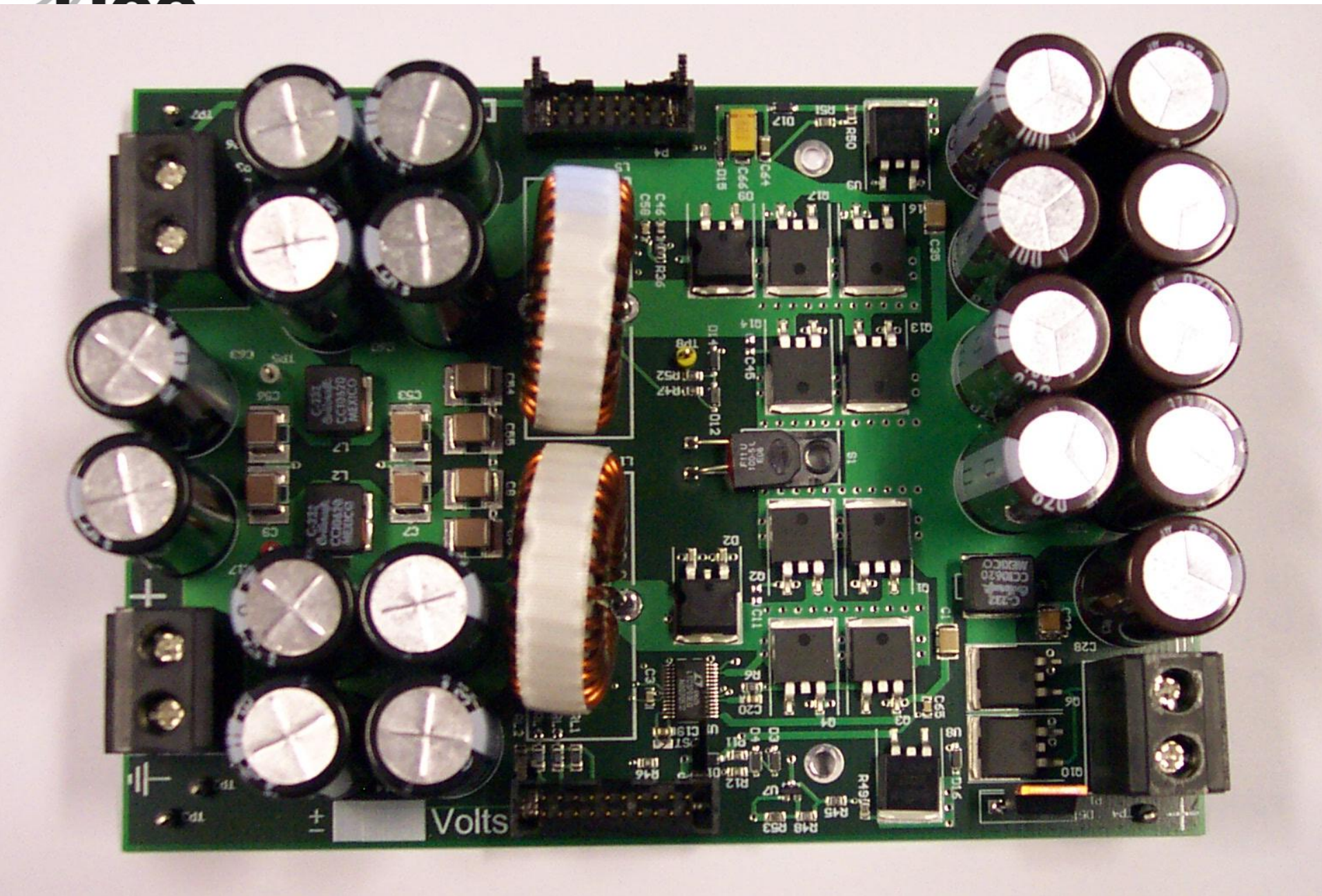
- Texas Instrument PTH08T240W
  - 12VDC input
  - 1V-5V at 10A output
  - External sync. input at 262144 Hz



Synchronous Buck Regulator / Vicor V·I Modules

- Still in evaluation phase
- Synchronous buck regulator
  - Runs at 131072 Hz
  - Dual output, 10A ea.
  - Almost works
- Vicor V·I Modules
  - Prototypes fabricated
  - Testing in progress




Volts

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Power Supply Chassis

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Summary

- New timing design well underway
  - Hope to have final design by end of year
- First prototype for new converter design is ready
  - Hope to have noise performance evaluated by end of year
  - Hope to have a full prototype with uplink mid next year
- New ideas for power supplies under investigation
  - Hope to have a design by mid next year