Digital Controls, ADC and DAC Research and Development for LIGO II

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J. Heefner

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ADC and DAC Research

- The ADC and DAC modules used in LIGO for real-time control are Pentek model 6102
  - ››VME based
  - ››8 channels of ADC (+/- 10 volt input)
  - ››8 channels of DAC (+/- 5 volt output)
  - ››The input referred noise of the ADCs is ~7uV/rtHz
  - ››The output referred noise of the DAC is ~2-3uV/rtHz

ADC and DAC Research

- For LIGO II it would be beneficial to have better performance and additional/different features.

  ››Input and output referred noise closer to the theoretical limits. This would simplify whitening and dewhitening of signals.

  ››More channels per module and ADC and DAC in separate modules

  —Each 6102 has 8 ADC and 8 DAC channels. In most LIGO (LIGO II) applications it would be better to have these functions separated and the channel density increased.

  ››Features more tuned to LIGO applications

  —The 6102 has many features that are not used by LIGO. These include on board FIFOs, auxiliary DSP comm ports, many triggering options. Elimination of these would presumably allow the number of channels to be increased and the cost of each module to be reduced.

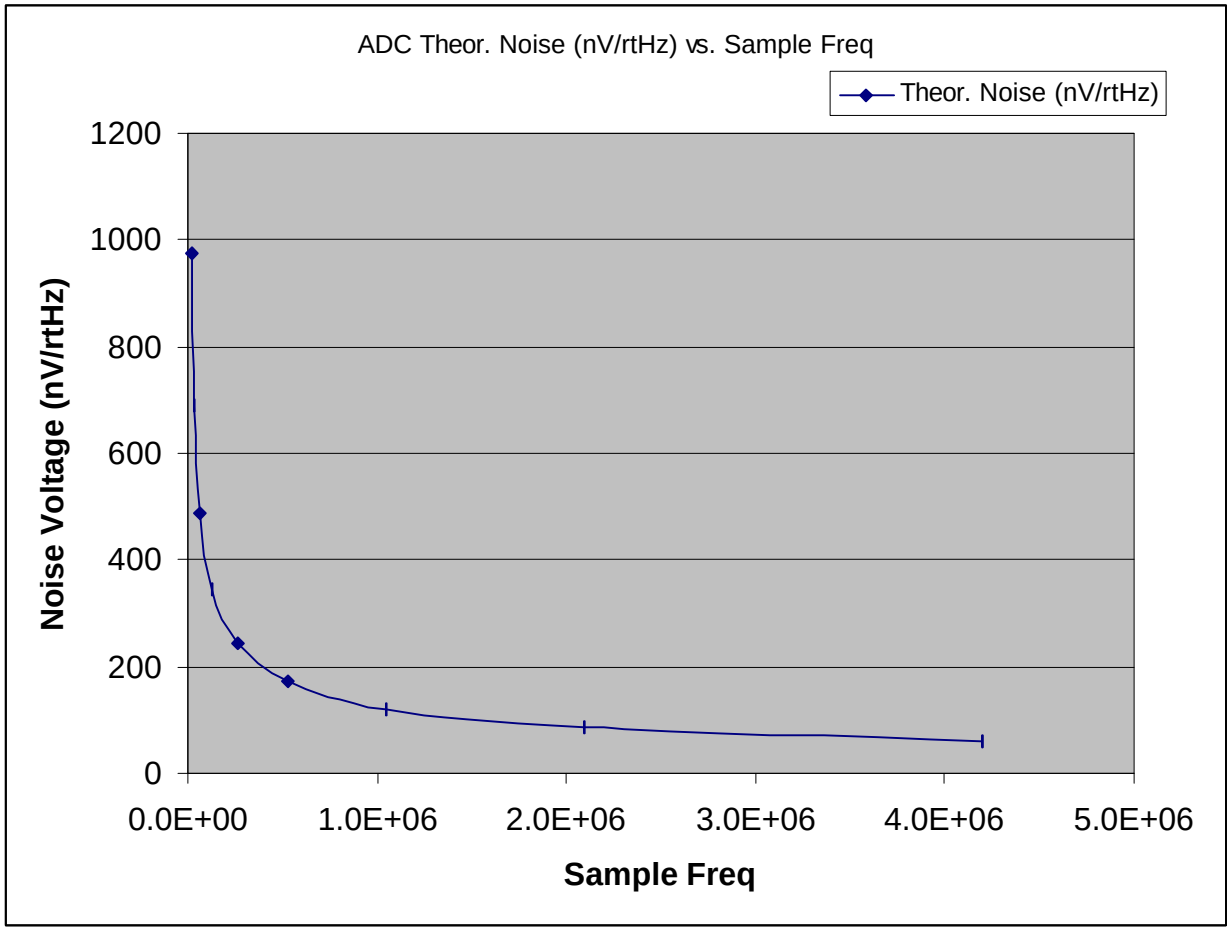
  —Clocking of DAC independent of ADC

  —Interrupt on single sample

  —On board anti-Alias and anti-Image filtering

  —Clock input separated from signal input (separate connectors and cable)

ADC and DAC Research



ADC and DAC Research

- The requirements that we have are not beyond the current state of the art, but it will require a development program
- In order to get the modules that we need there are two paths that we can take:
  - ››Contract with an vendor to produce modules to our specifications
    - —We have already begun discussions with several manufacturers. So far it appears as though many of our requirements and desires can be met.
  - ››Design the modules in house or in collaboration with another group
    - — Many of our requirements are the same as other groups (VIRGO, GEO). VIRGO has already designed ADCs and DACs to be used in their interferometers. We have begun looking at the performance of these modules and will begin discussions of a collaboration to build next generation ADCs and DACs.

Digital System/Servo Research

- LIGO operations and commissioning have shown that a great deal of flexibility is needed in system design and implementation.
- Servos and systems implemented digitally provide this added flexibility.
- The suspension systems in LIGO are a good example of this:

  ››The original suspension controllers were analog and developed using requirements early in the project.

  ››Over time it was found that additional features and performance were necessary. The “old” analog controllers proved hard to reconfigure and are now being replaced with digitally based controls.

  ››These digital controls allow the operator to change servo filters, transformation matrices and add such things as frequency dependence to the matrices. These changes can be made on the fly.

Digital System/Servo Research

- Processors (faster, better, cheaper)

  ››It is not currently envisioned that LIGO II will require more complex algorithms, but there will be many more servos implemented digitally. Many of these servos will cross subsystems boundaries and will produce “bottlenecks” at points such as the outputs to suspension actuators.

  ››Processor speed can help reduce these bottlenecks.

  ››The processor industry is changing rapidly and we need to keep up. Processors available today will not be available 1 year from now.

- Platform (backplane)

  ››The platform of choice is currently VME, but moving to another platform may have some advantages.

Digital System/Servo Research

- Communications

  ››Reflective memory is currently used to move data and communicate between real-time systems. There may be alternatives that would provide higher bandwidth and greater flexibility.

  ››One of the other “bottlenecks” in the system is the VMEbus connection from the processor to the ADC/DACs. It may be advantageous to pursue processor to ADC/DAC links that are separate from the VMEbus. These could include PCI/PMC, DSP comm port, etc. This research will obviously have to proceed in parallel with the ADC/DAC development.

Digital System/Servo Research

- Full up Test Stands and Development Areas

  ››Due to schedule and manpower constraints in LIGO we did not have time to build up and fully test many of the digital systems prior to installation on the interferometer.

  ››In LIGO II we would like to minimize this by building up test stands and development areas early. In addition, we would like to use the 40 Meter and LASTI as testing and development areas. We should then be able to incorporate features and eliminate as many problems as possible prior to installation. This will allow the commissioning team to concentrate more fully on commissioning.