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High-Power High-Speed Photodiode for LIGO II

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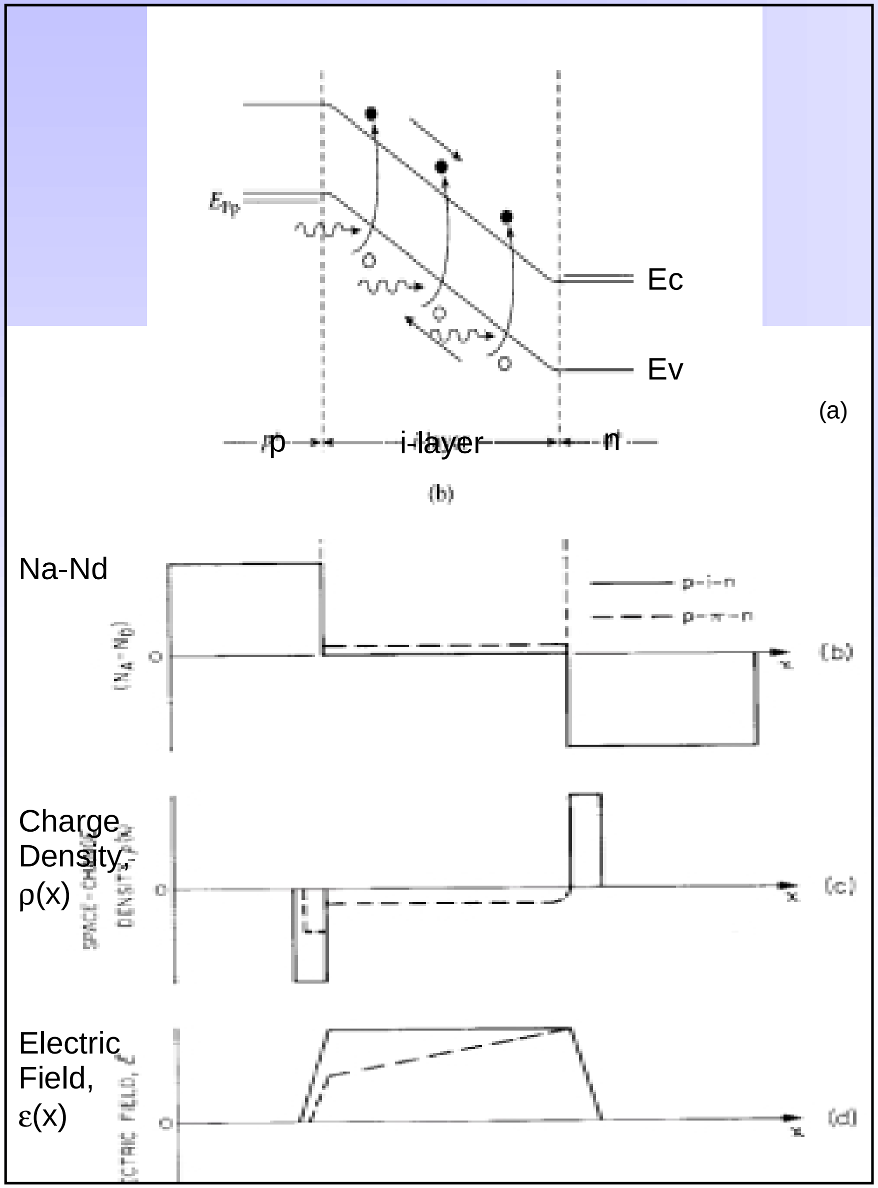
LIGO-G000241-00-D

Outline

- Motivation
- Diode structure & Materials choices
  - Graded buffer layer
  - Processing procedure
- Simulations
  - Absorption QE
  - Frequency response
  - Electronic noise
- Experimental results & Future work

P-I-N Device Characteristics



- Large E-field in I-region
- Depletion Width ≈ Width of I- region
  - Frequency response

    $$f_{max} \approx (v_{sat} / W_I)$$

  - RC time constant

    $$\approx R_s C_J$$

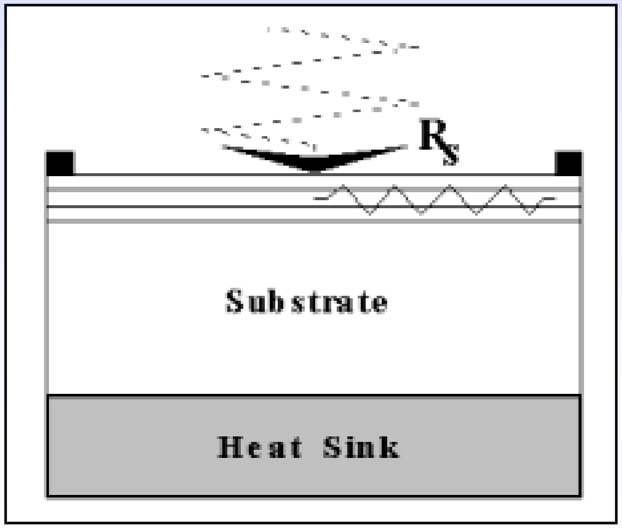
    $$C_J = K_s \varepsilon_0 A / W_I$$

  - Tuned to a specific λ

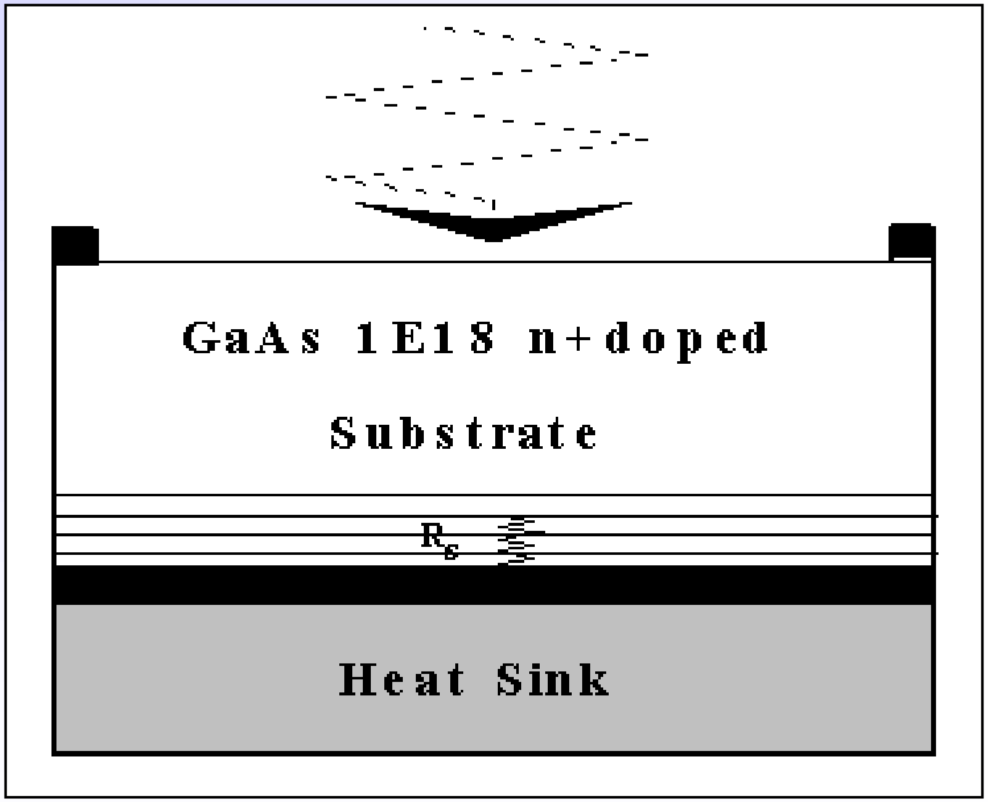
    $$W_I >> \frac{1}{\alpha}$$

Photodiode Advantages

- High Power
- Linear Response
- Optimum E_g
- High Speed

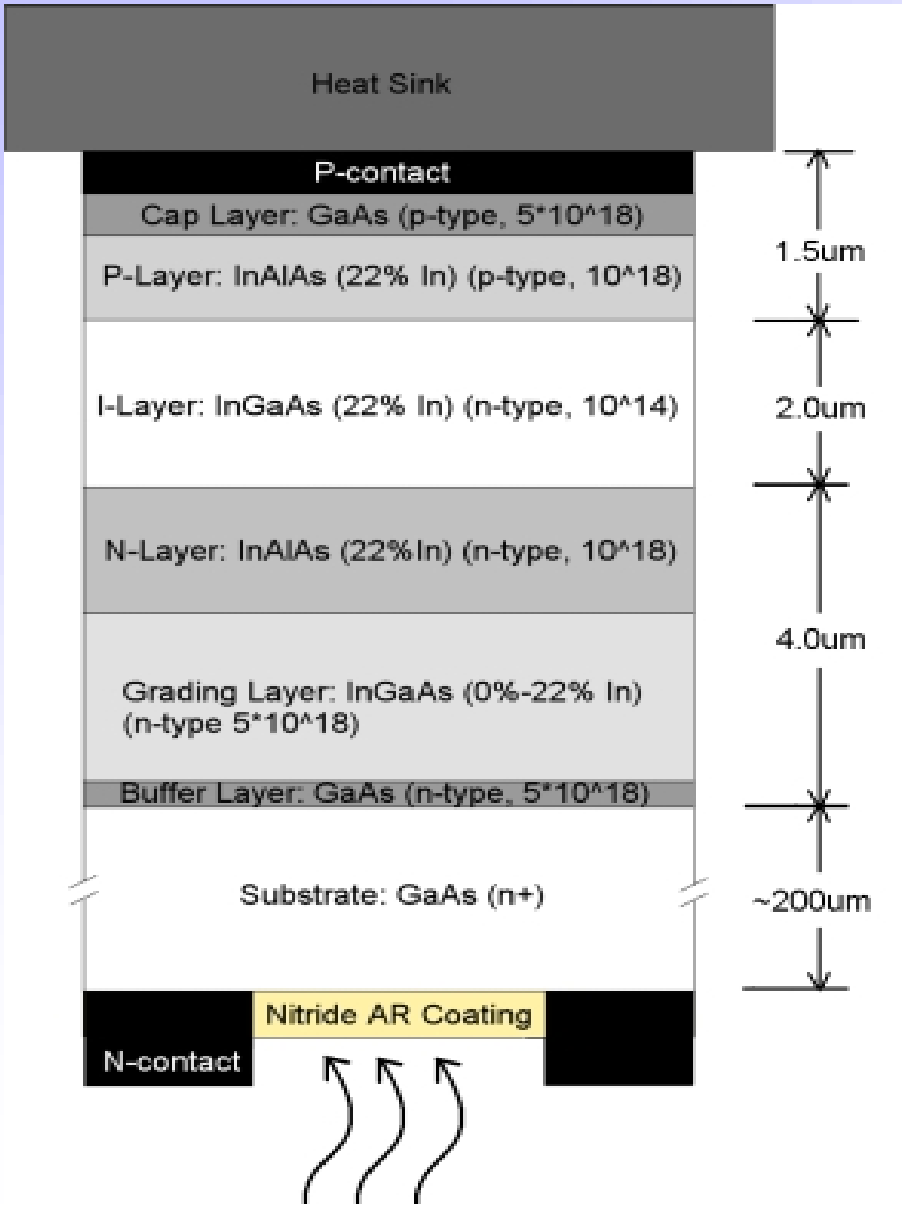


Conventional PD



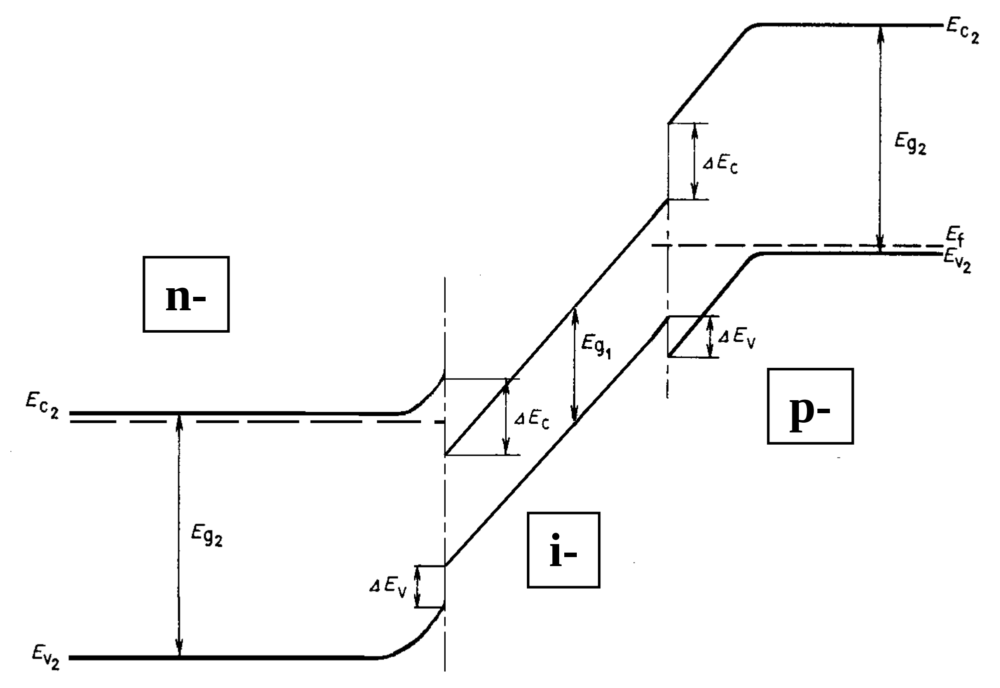
Proposed PD (Rear-Illuminated)

InGaAs/GaAs PD Structure



- InGaAs for i-layer
- InAlAs for the n- and p- layers
- P-I-N structure
- MBE
- Grading layer
- AR coating & Au/Pt contacts

Band Gap Diagram w/ Heterojunctions



N-layer:	I-layer:	P-layer:
$In_{.22}Al_{.78}As$	$In_{.22}Ga_{.78}As$	$In_{.22}Al_{.78}As$
$E_{g2} = 2.0$eV	$E_{g1} = 1.1$eV	$E_{g2} = 2.0$eV

- **InAlAs Optically transparent to 1.06µm radiation**
- **Absorption occurs in i-region**

III-V Lattice Constants and Band Gaps

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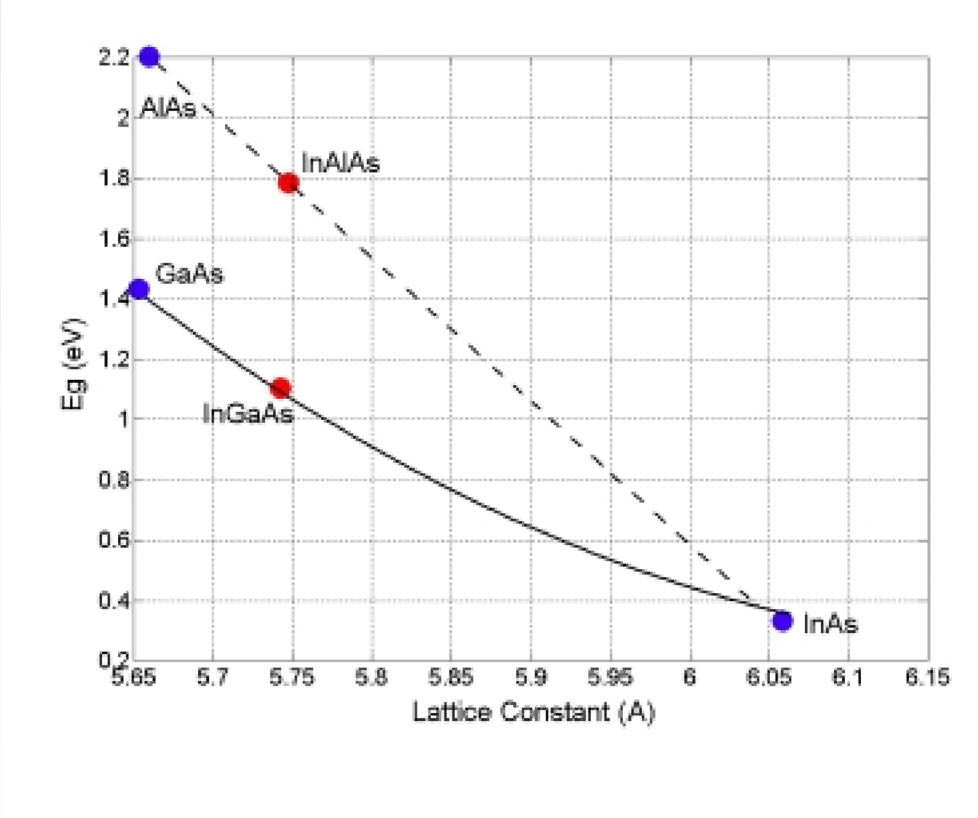

- **InAlAs and InGaAs well lattice matched**
- **InAlAs much wider band gap**

Lattice Mismatched Growth

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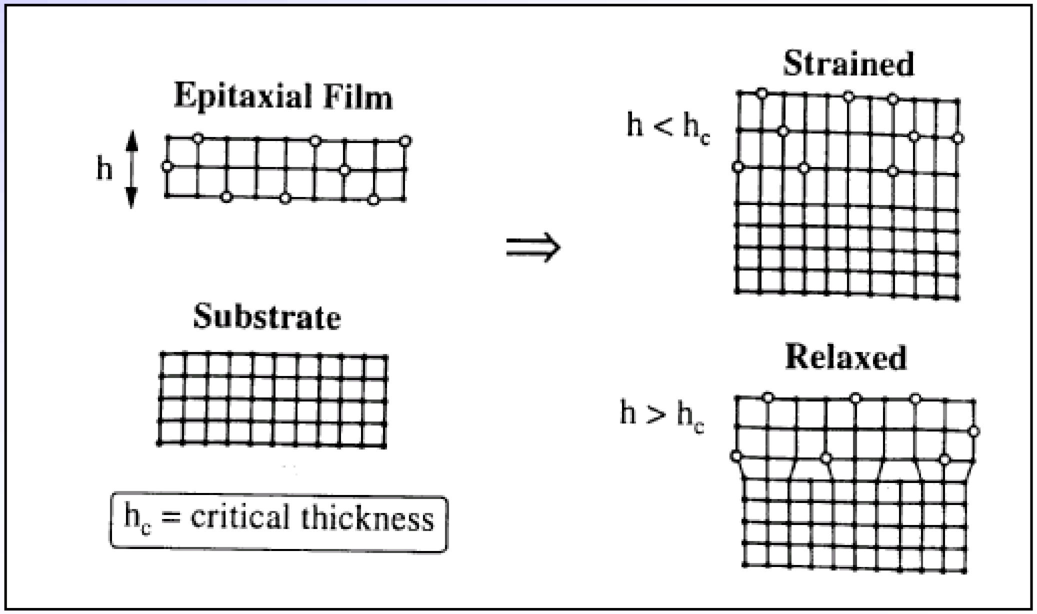
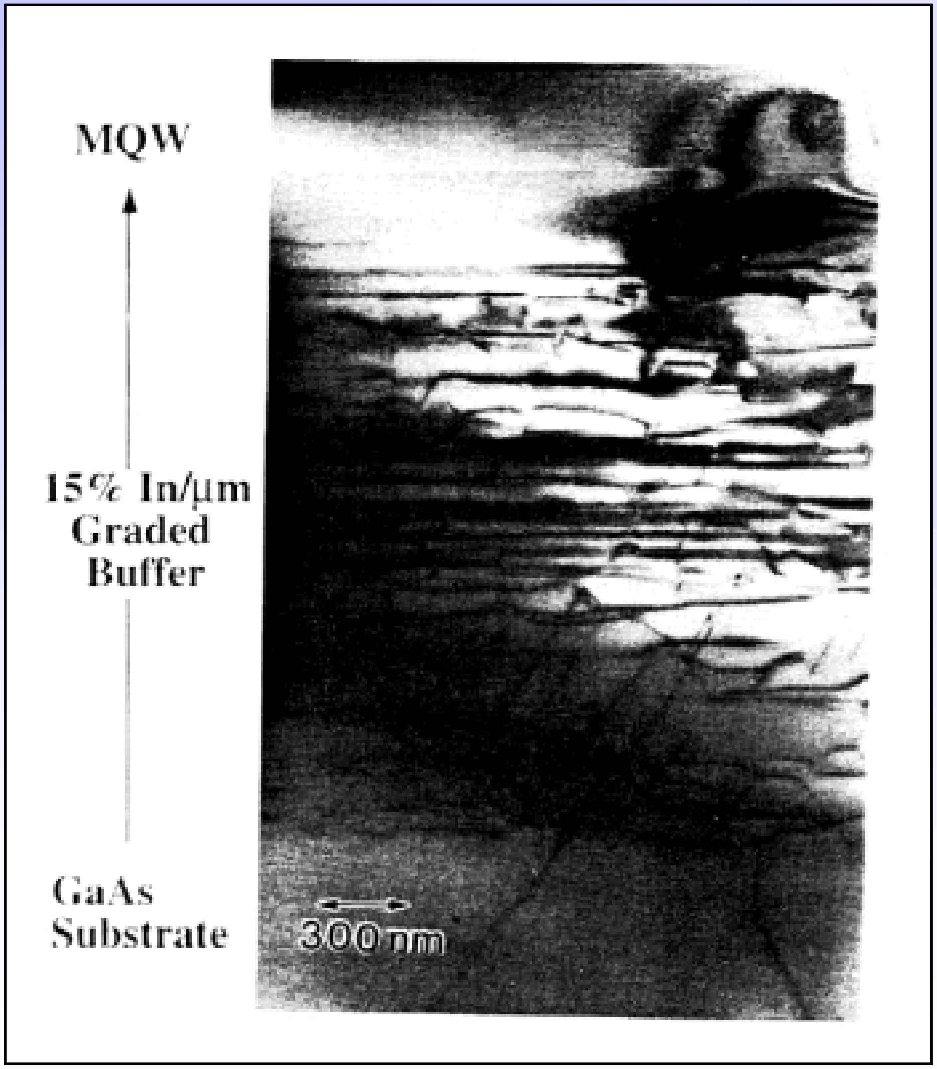
- **Lattice Constant for $In_xGa_{(1-x)}As$:**

  a=5.6536+0.4054x

- **$In_{.4}Ga_{.6}As$: $h_c \approx 100$Å**



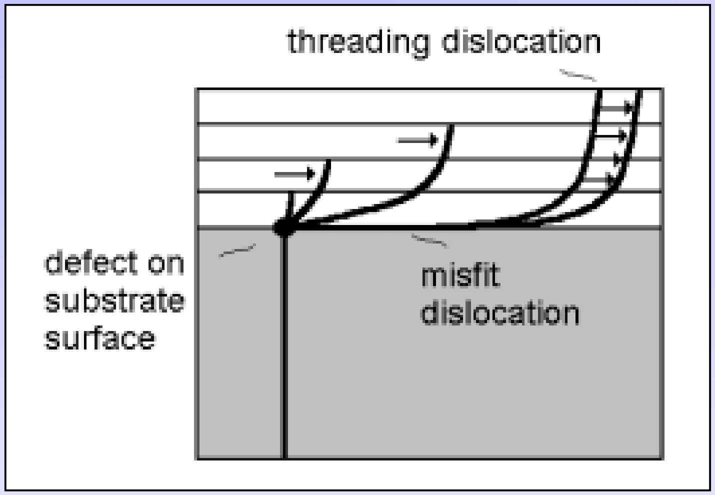
Solution: Graded Buffer Layer



- **Dislocations propagate downwards**
- **Active region free from dislocations**

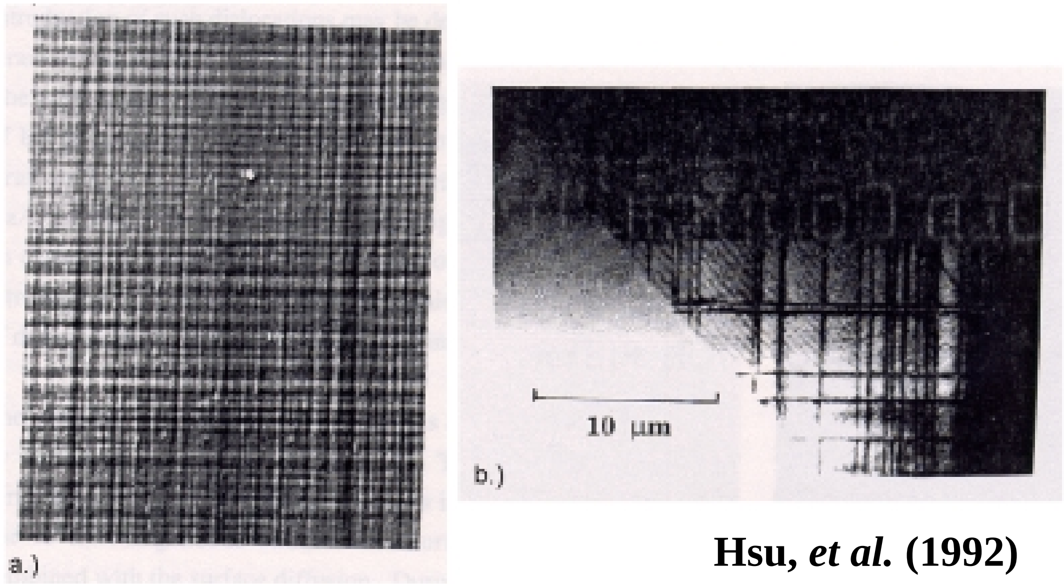
Susan Marie Lord, Ph.D Thesis,
Stanford Univ., 1993

Graded Buffer Dislocations



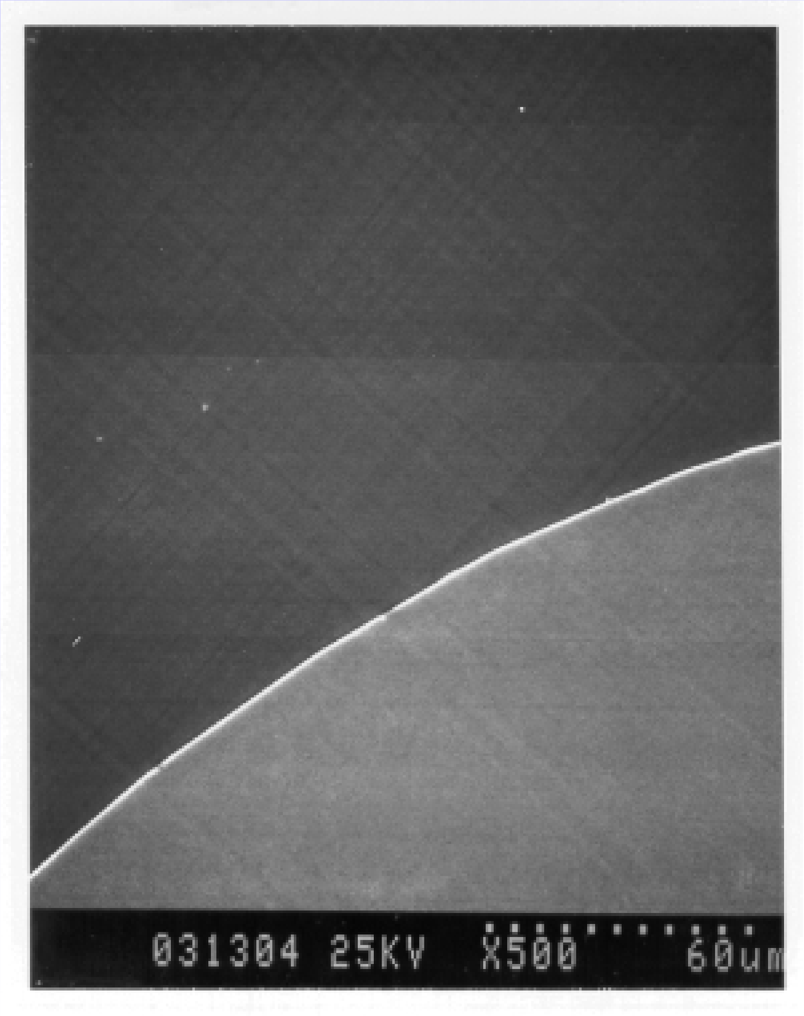
Biaxial stress in film causes dislocations to glide

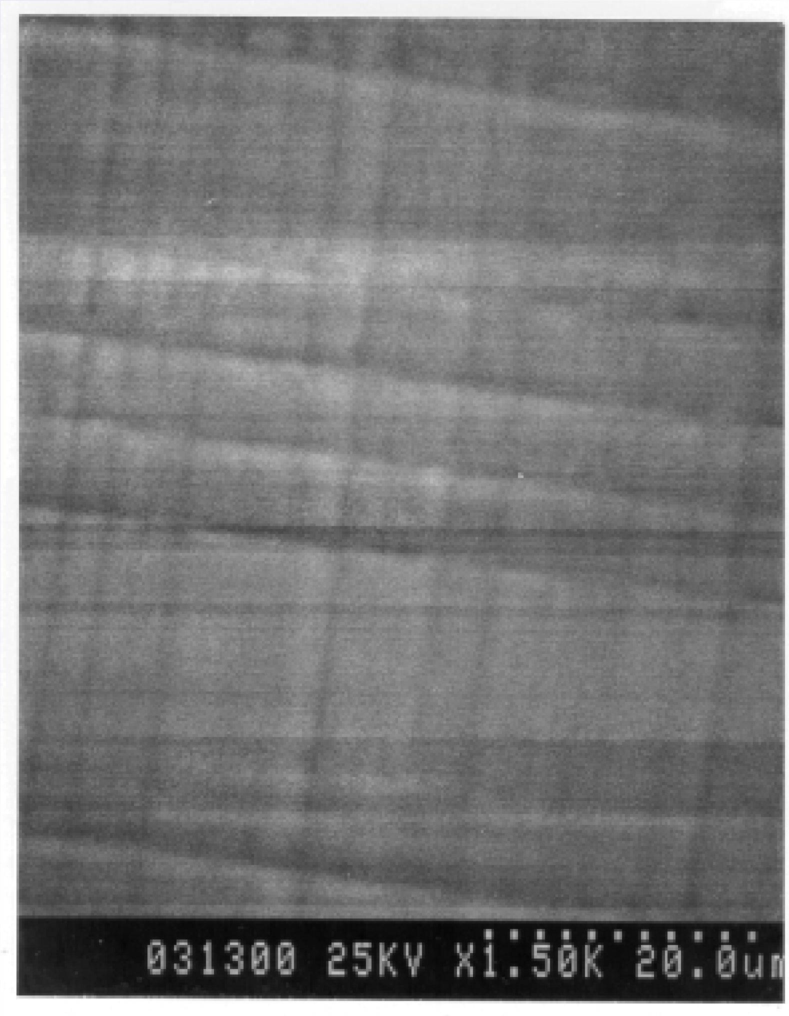
Misfit growth often results in surface striations



Hsu, *et al.* (1992)

Rear Contact (#637)





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Processing: Slide #1

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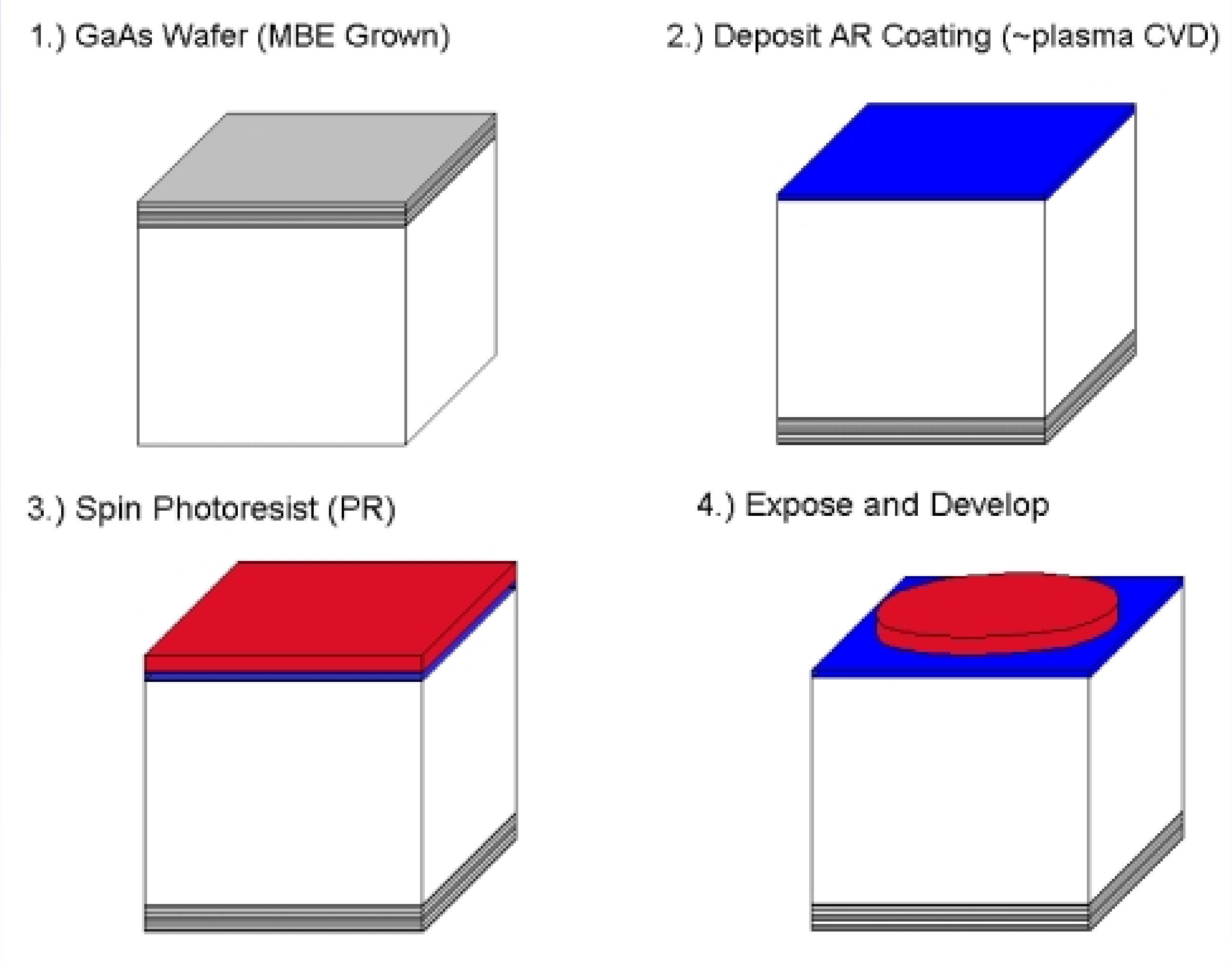

Processing: Slide #2

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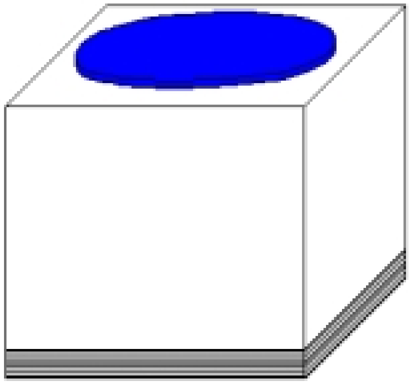
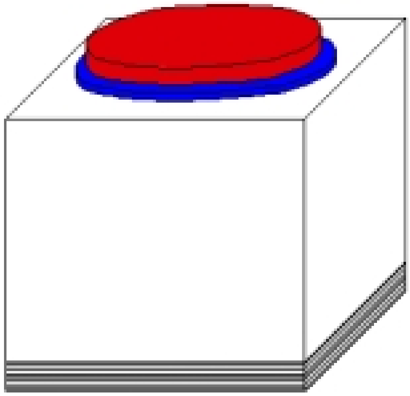
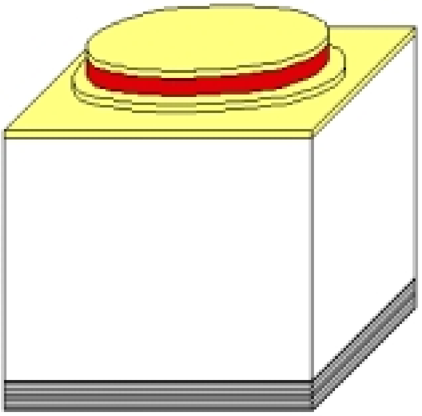
5.) Etch Nitride and remove excess PR



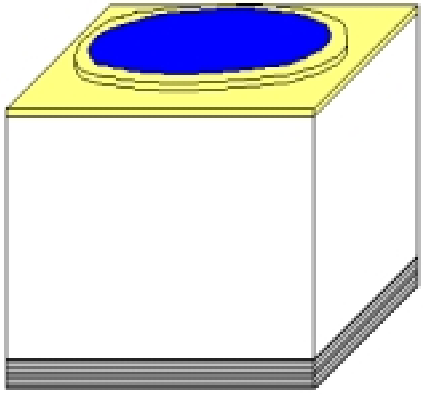
6.) Spin/Expose/Develop PR for N-Contact



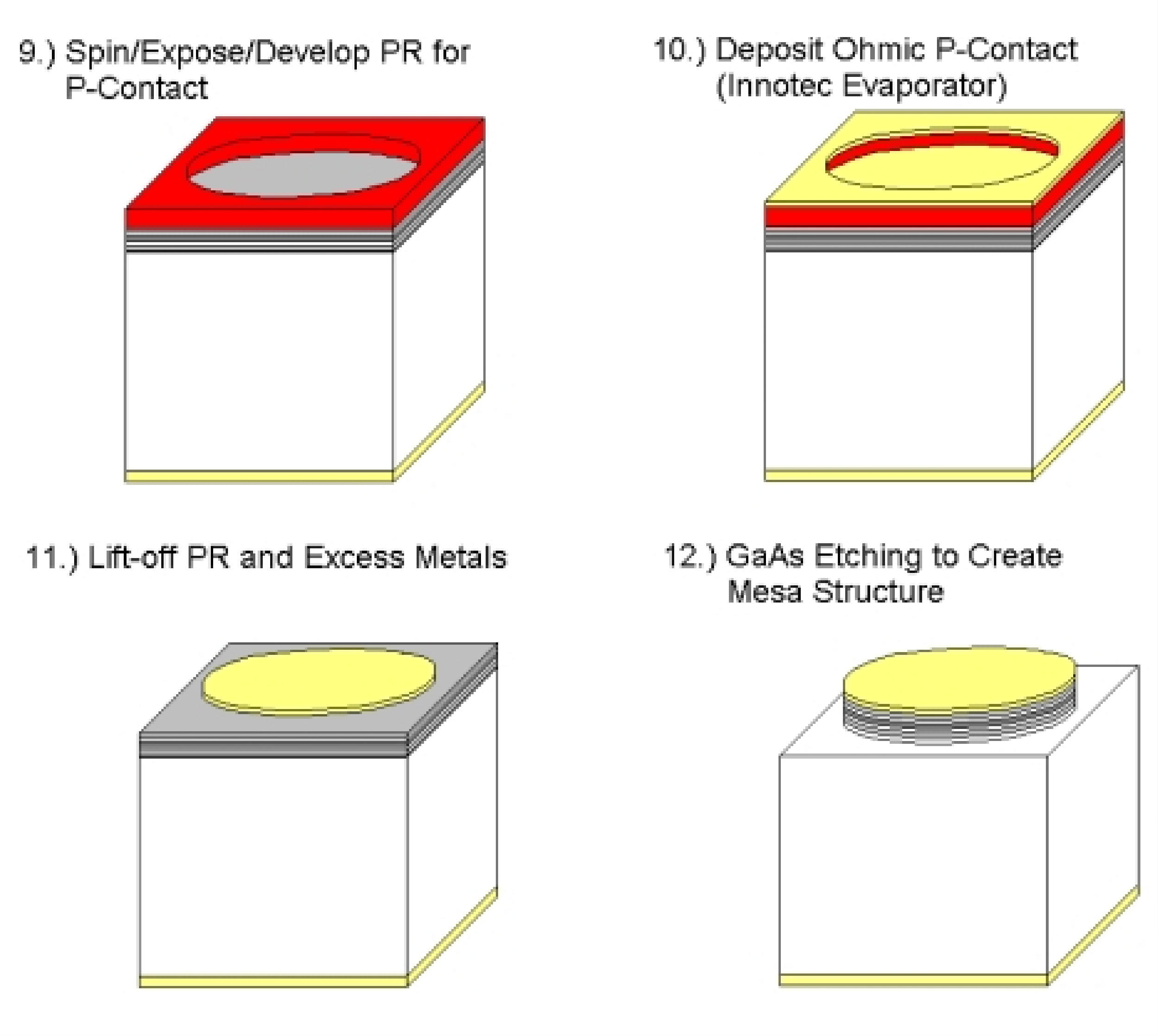
7.) Deposit Ohmic N-Contact (Innotec Evaporator)



8.) Lift-off PR and Excess Metals



Processing: Slide #3



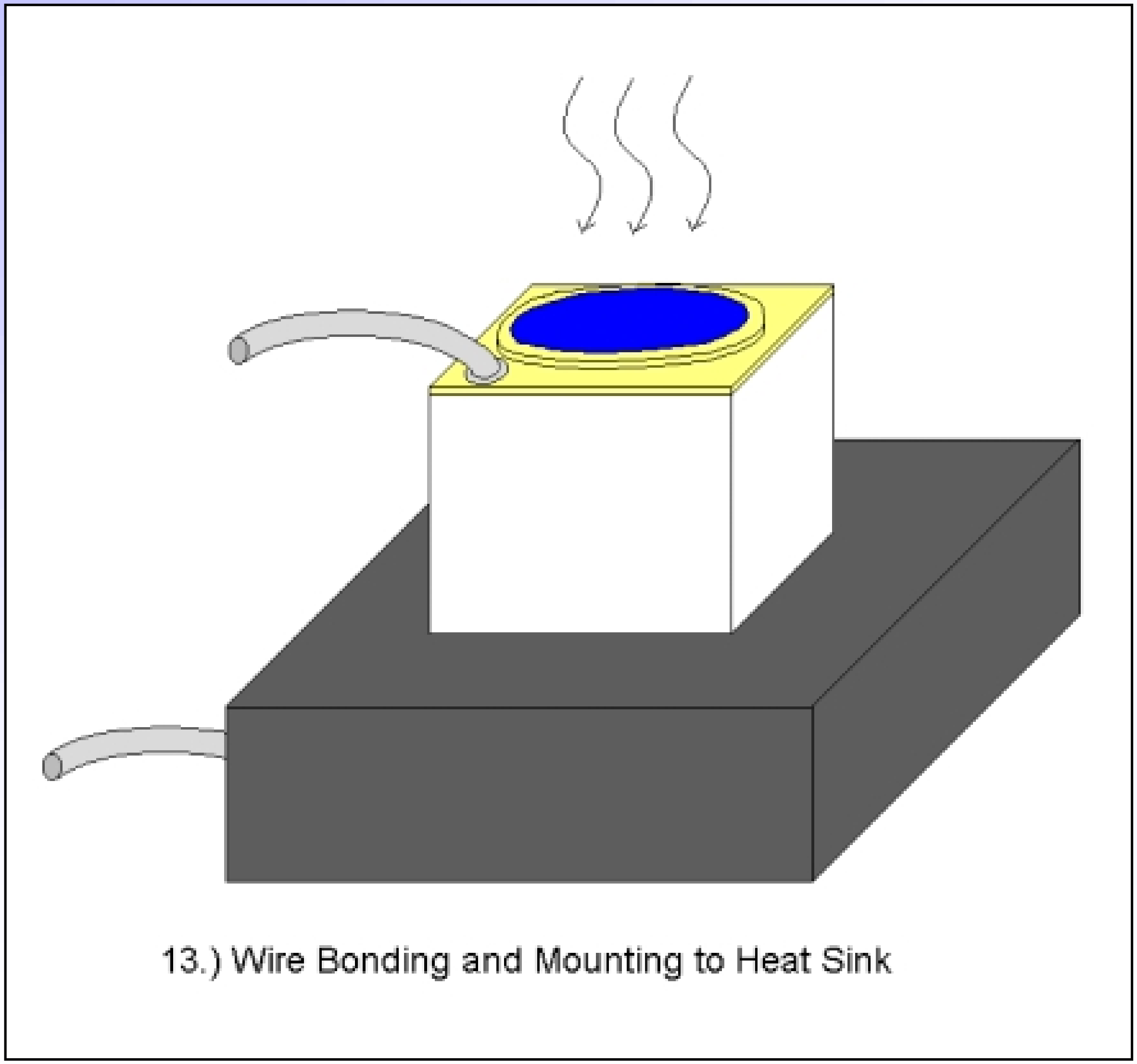
9.) Spin/Expose/Develop PR for P-Contact

10.) Deposit Ohmic P-Contact (Innotec Evaporator)

11.) Lift-off PR and Excess Metals

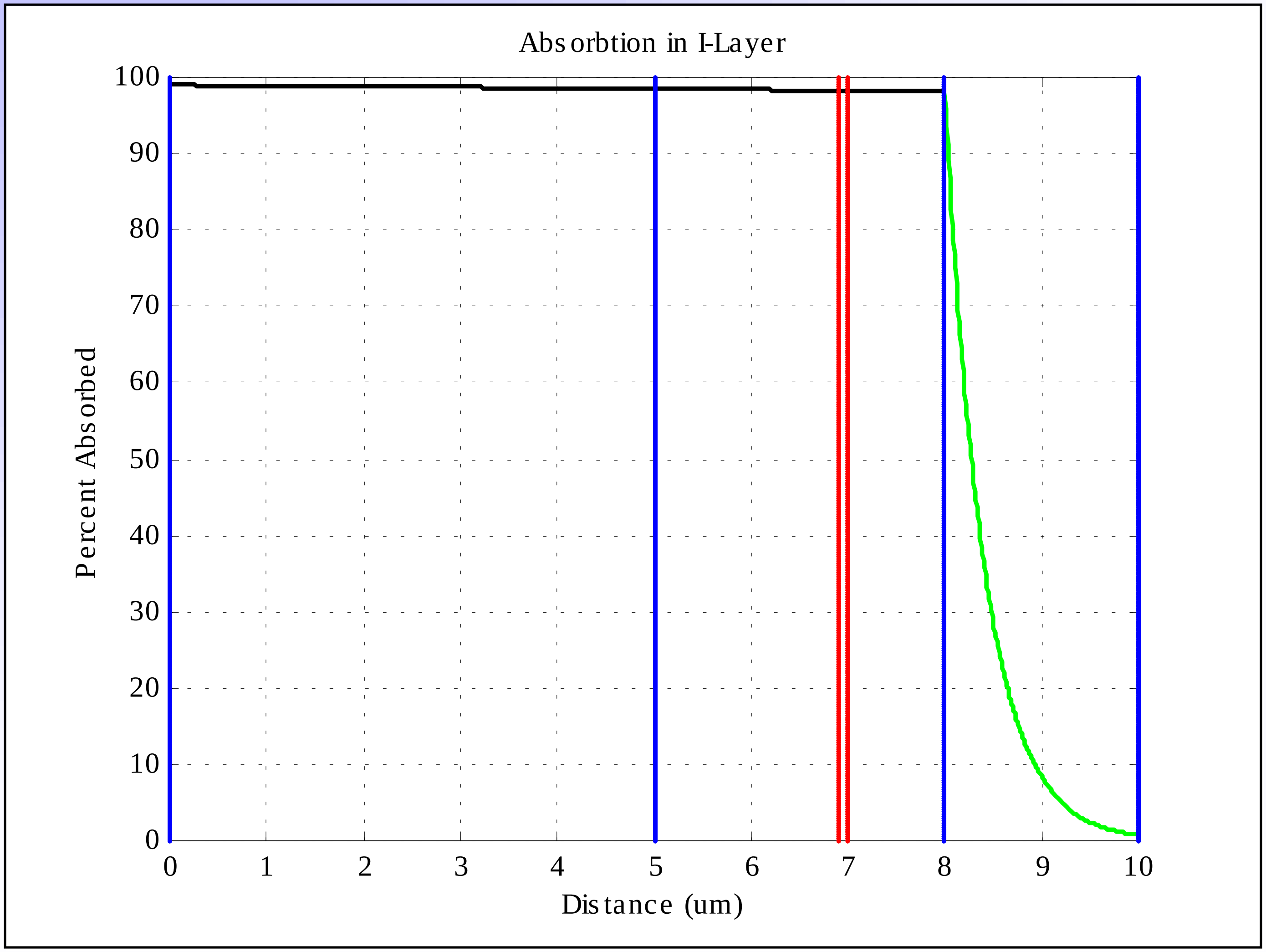
12.) GaAs Etching to Create Mesa Structure

Processing: Slide #4



13.) Wire Bonding and Mounting to Heat Sink

Absorption Simulation (1)



$$I(z) = I_0 \exp(-\alpha \cdot z)$$

Absorption Simulation (2)

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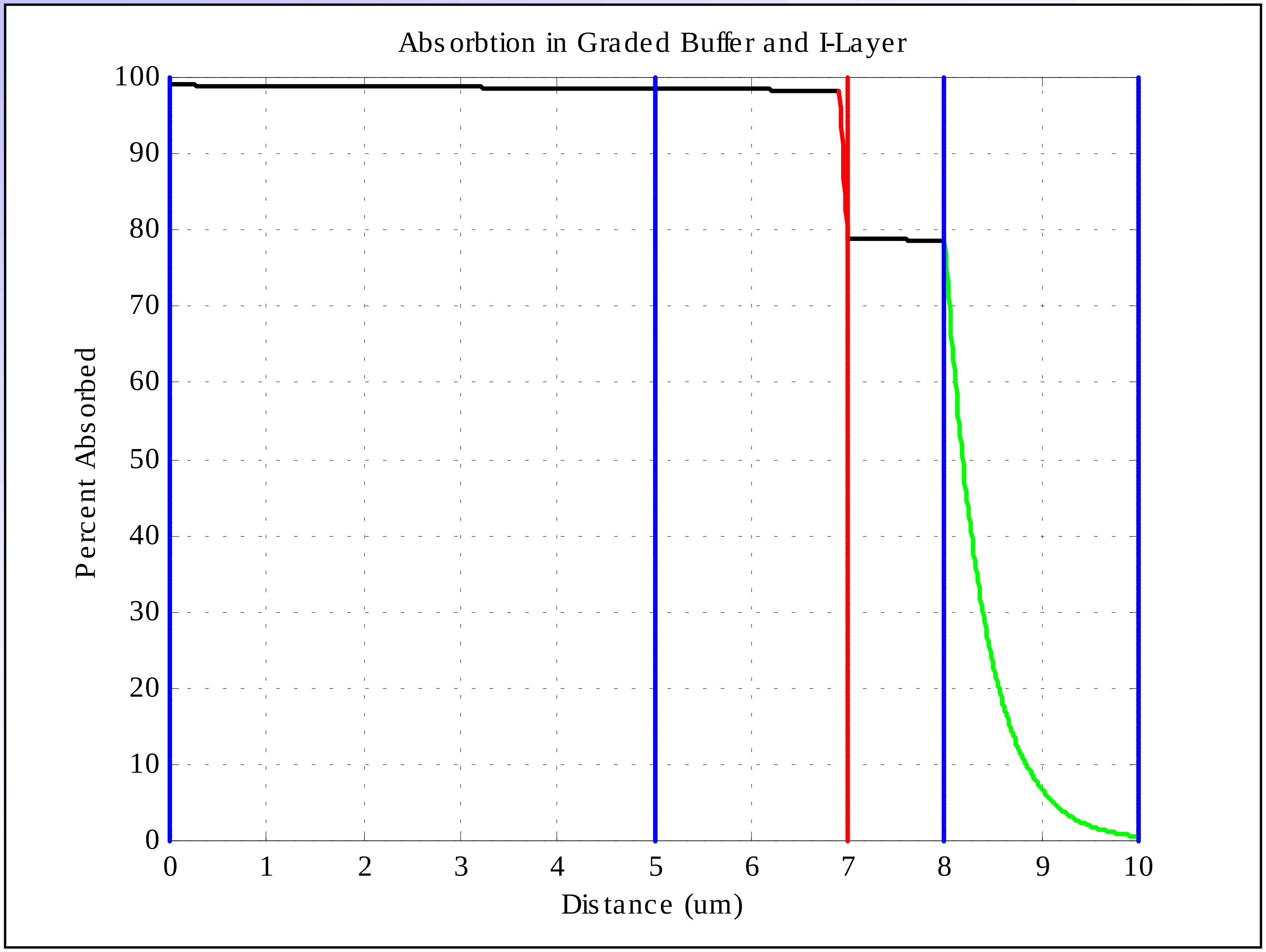
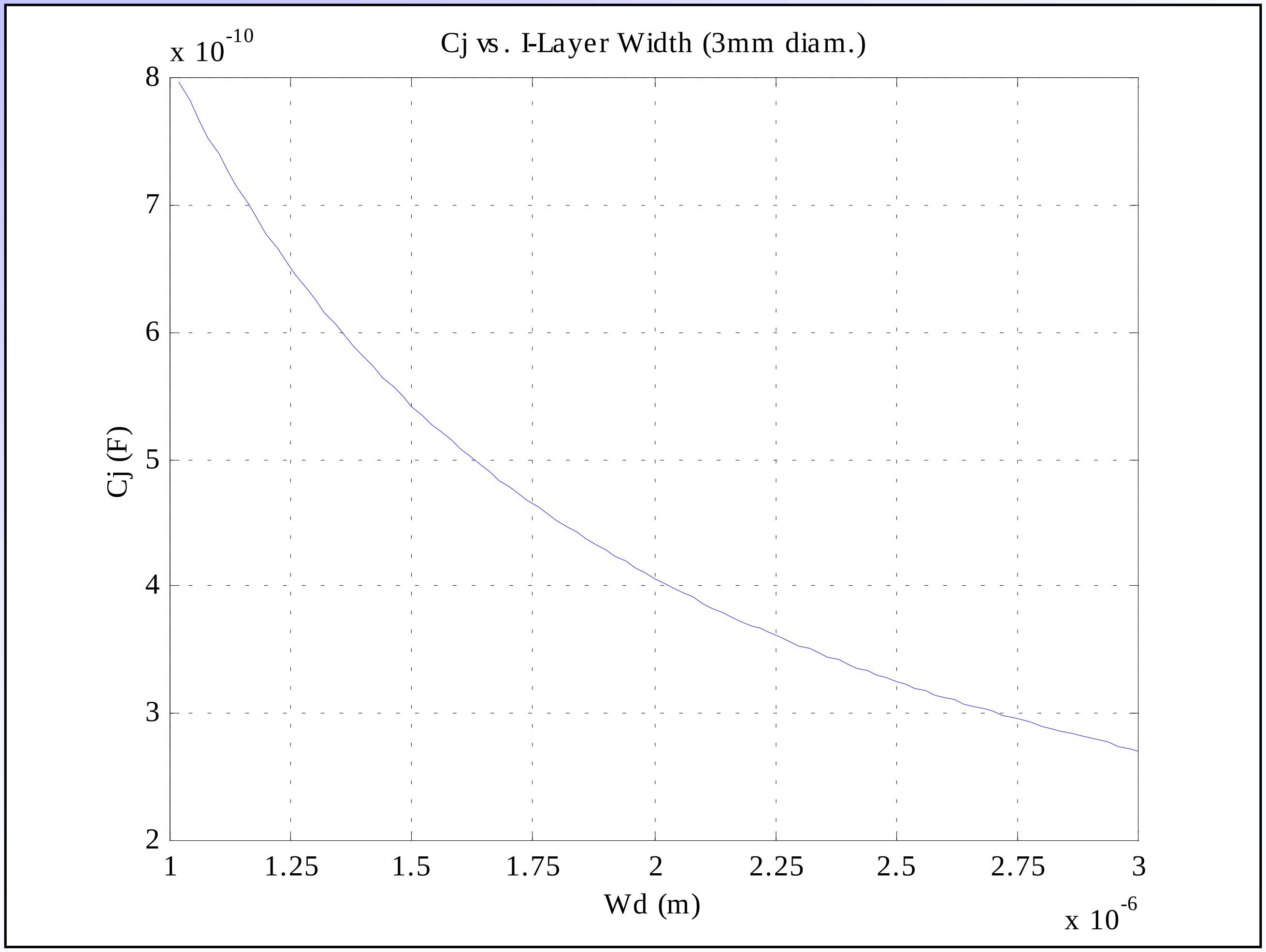


$\alpha_{InGaAs} \approx 2.41 \mu m^{-1}$

$\alpha_{GaAs} \approx 1 mm^{-1}$

Frequency Response Simulation (1)



$$C_j = \frac{\varepsilon_0 \varepsilon_r A}{w_d}$$

Frequency Response Simulation (2)

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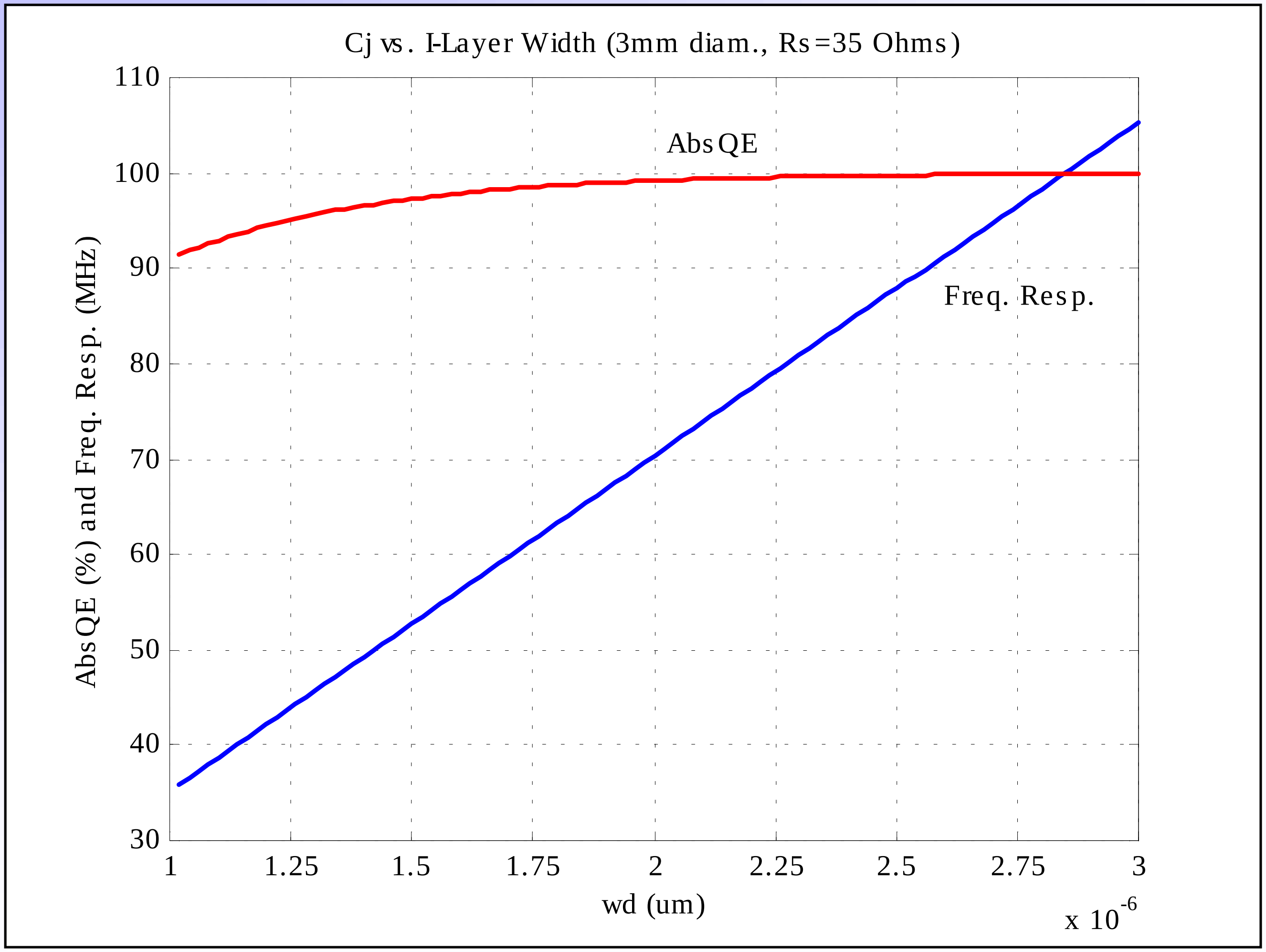
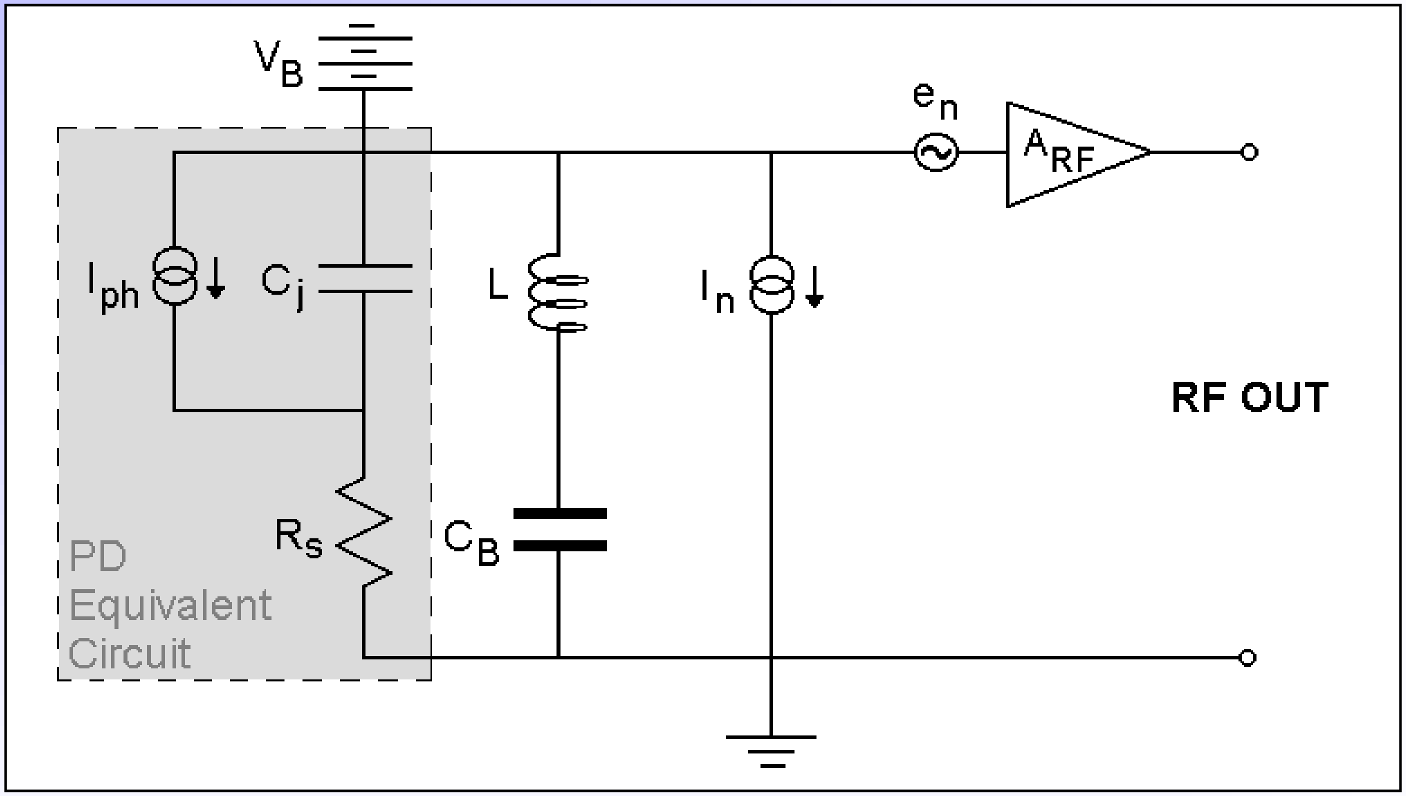


$$Freq.\,\mathrm{Re}\,sp. = {}^{1}\!/_{R_s C_j}$$

Electronic Noise



$$e_{elec}^2 = 4k_B T Z_D + i_n^2 Z_D^2 + e_n^2$$

$$e_{shot}^2 = Z_D^2 \cdot 2eI_{DC} \cdot K_{mod}$$

$$Z_D(\omega_0) = \frac{1}{R_S C_j^2 \omega_0^2}$$

Electronic Noise Simulation (1)

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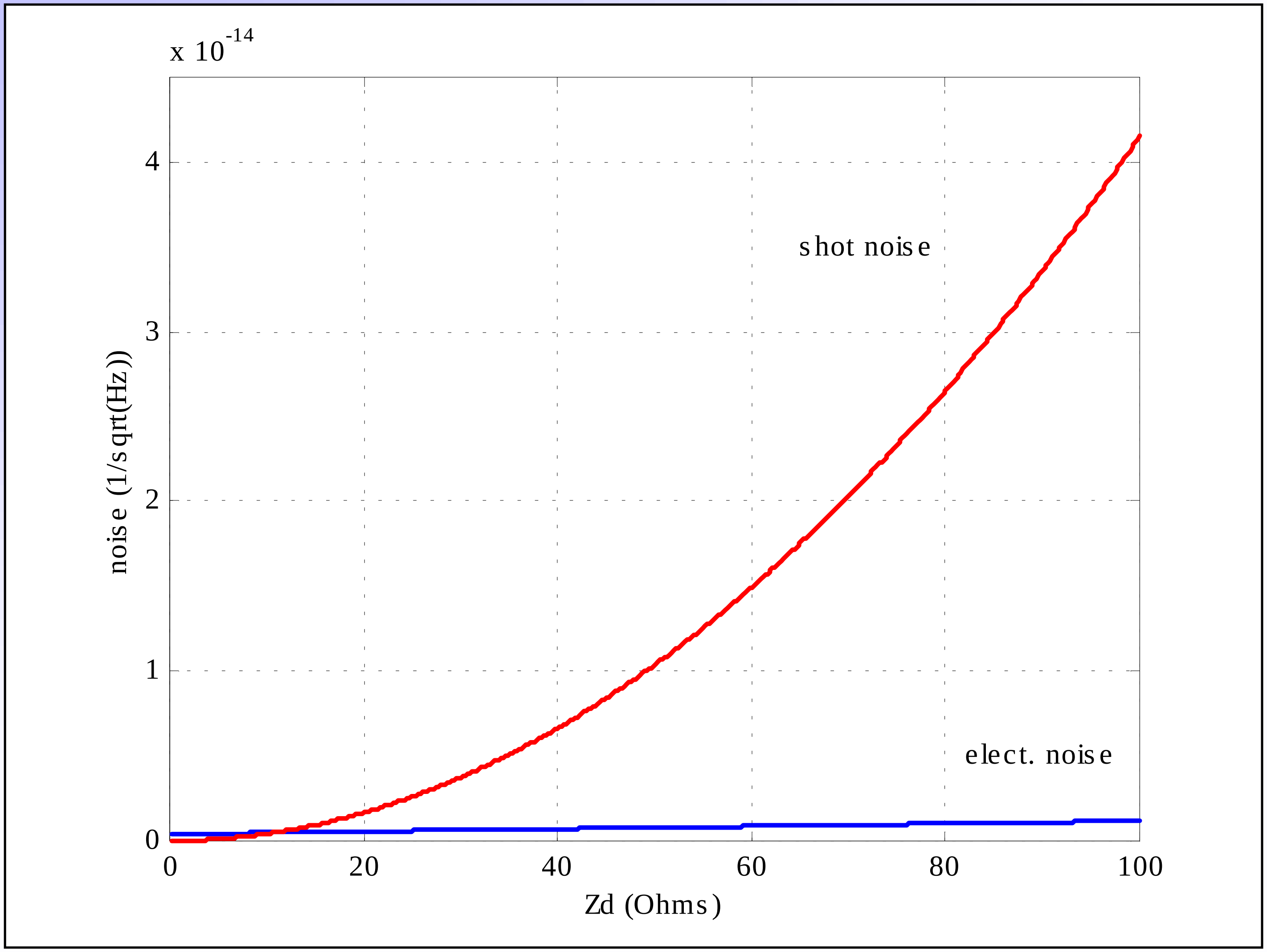
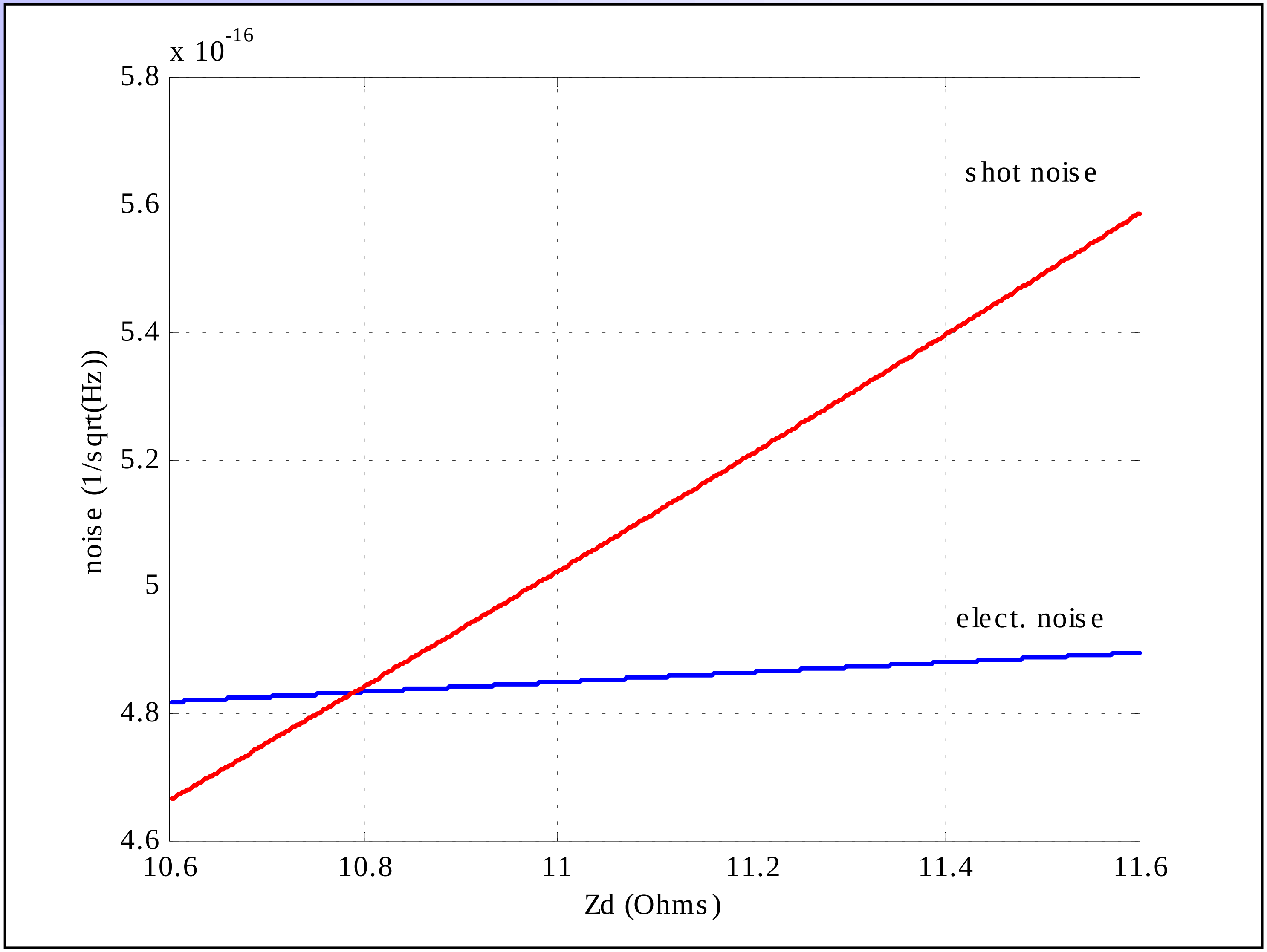


Electronic Noise Simulation (2)



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Electronic Noise Simulation (3)

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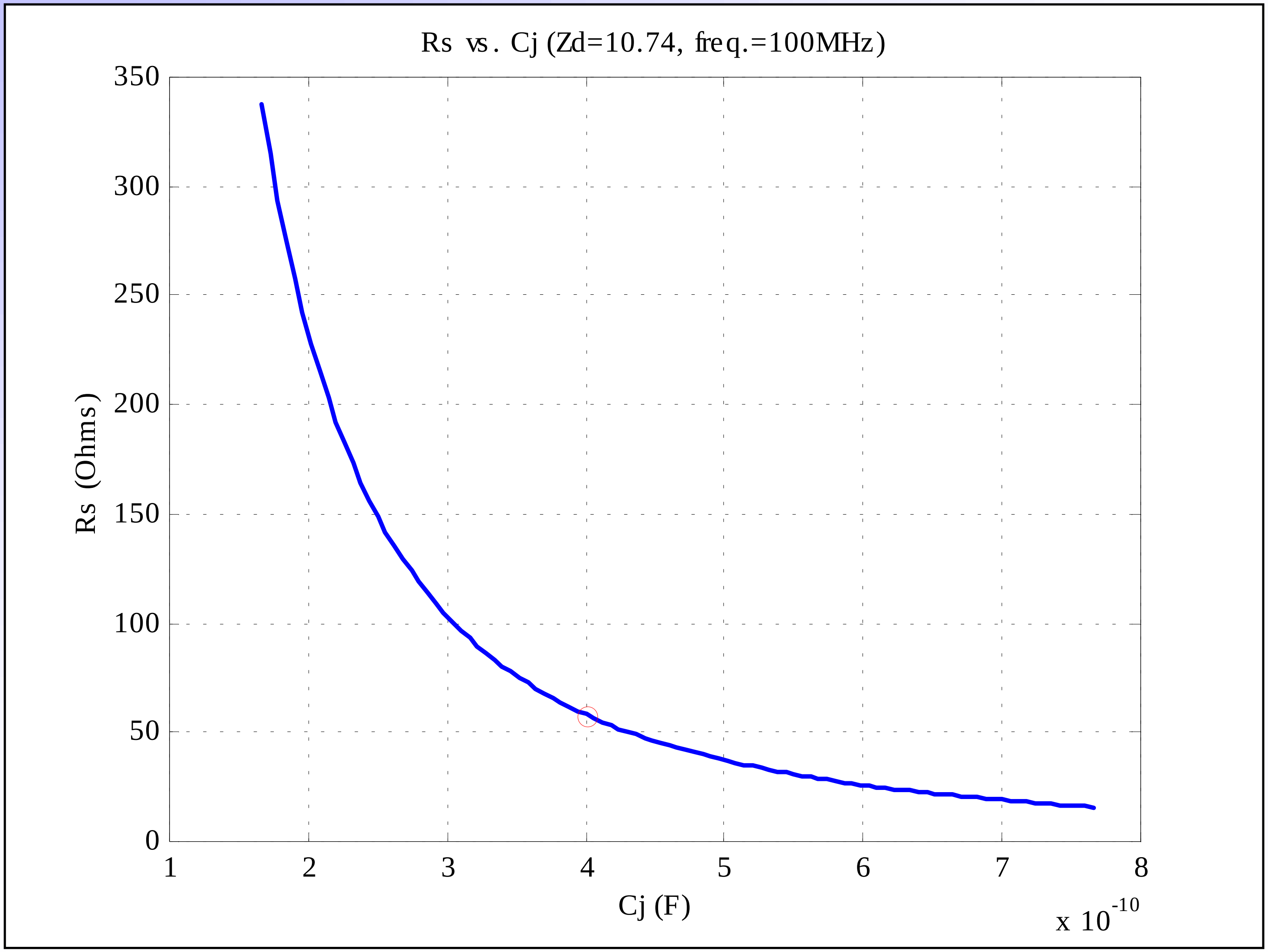

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I-V Curves: Mounted Diodes

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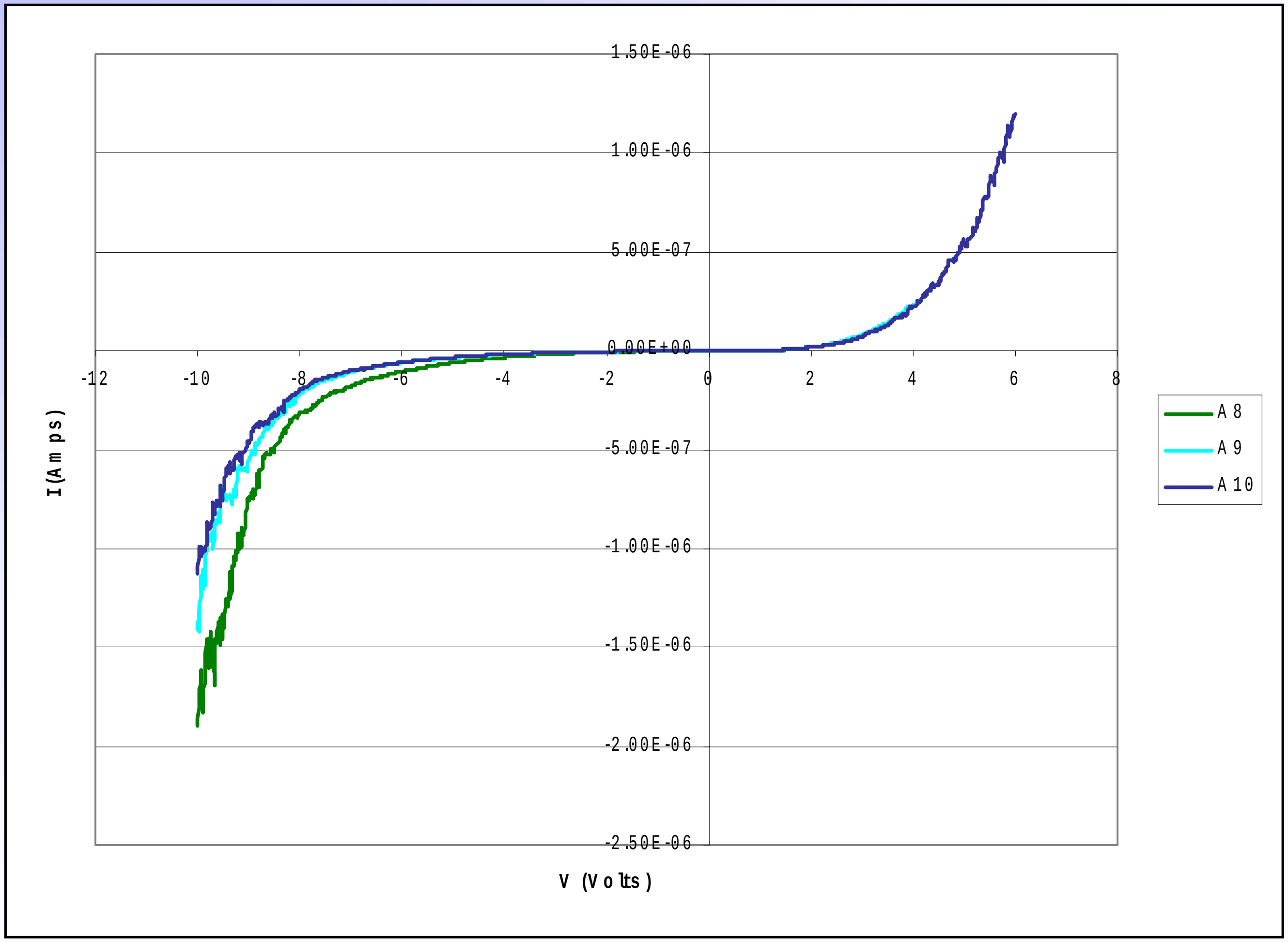
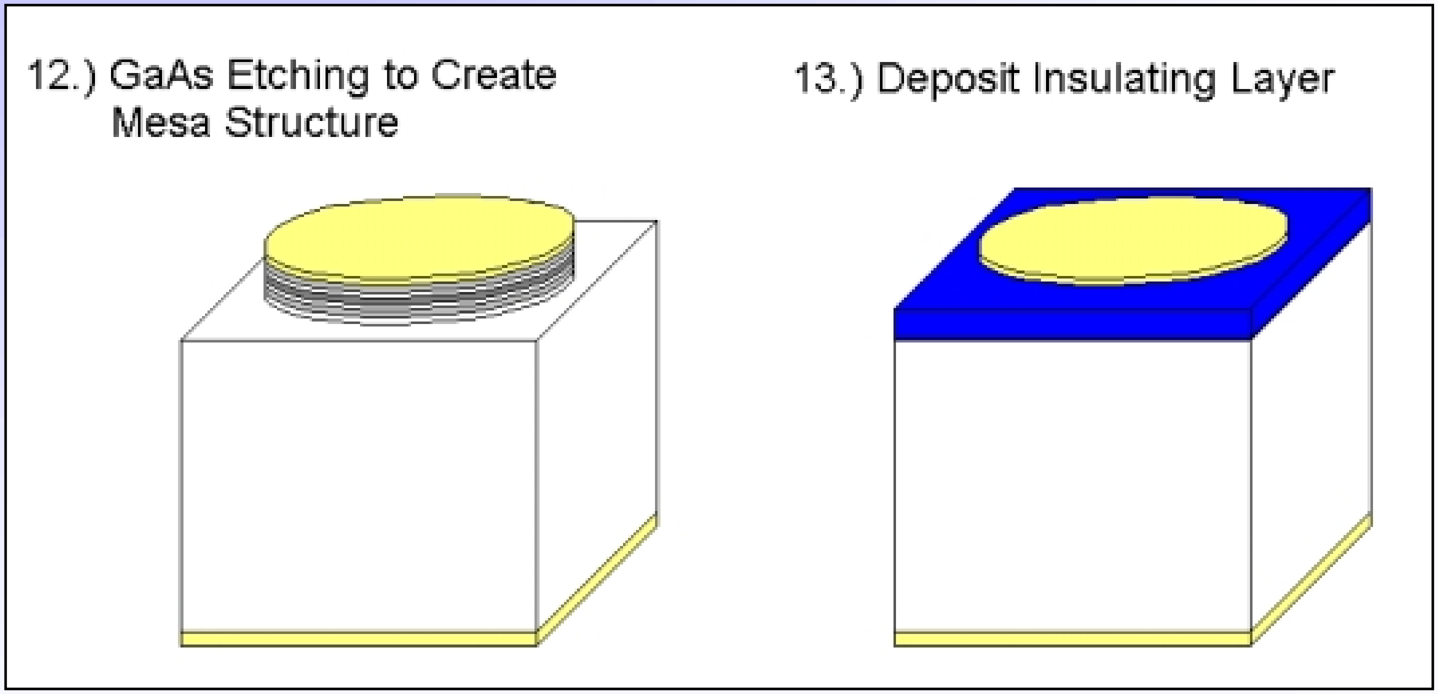


Possible Solution- Insulating Layer



Diagnostics by Processing Step

I.) MBE Growth

- Transmission
- XRD
- TEM

II.) AR Coating

- Transmission

III.) N- and P- Contacts

- TLM
- I-V Measurements
- C-V Measurements

IV.) Etch Mesa

- I-V Measurements
- C-V Measurements
- Low Power LASER testing

V.) Insulating Layer

- I-V Measurements

VI.) Mounting to Heat sink & Wire Bonding

- I-V Measurements
- High Power LASER Testing (10W)
  i. QE
  ii. Response Linearity
  iii. Bandwidth
  iv. Power Dissipation

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Transmission Spectra

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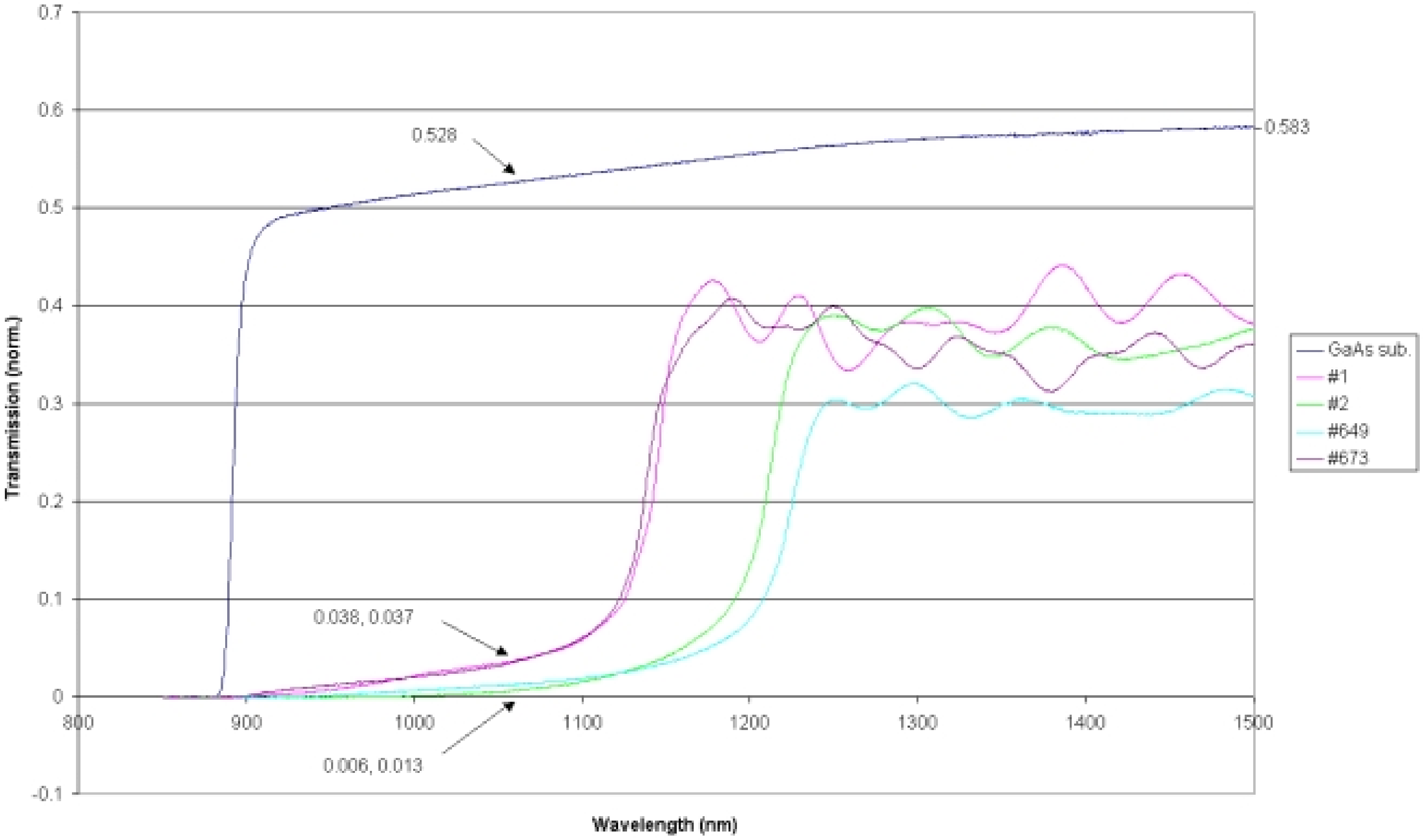

XRD Measurements

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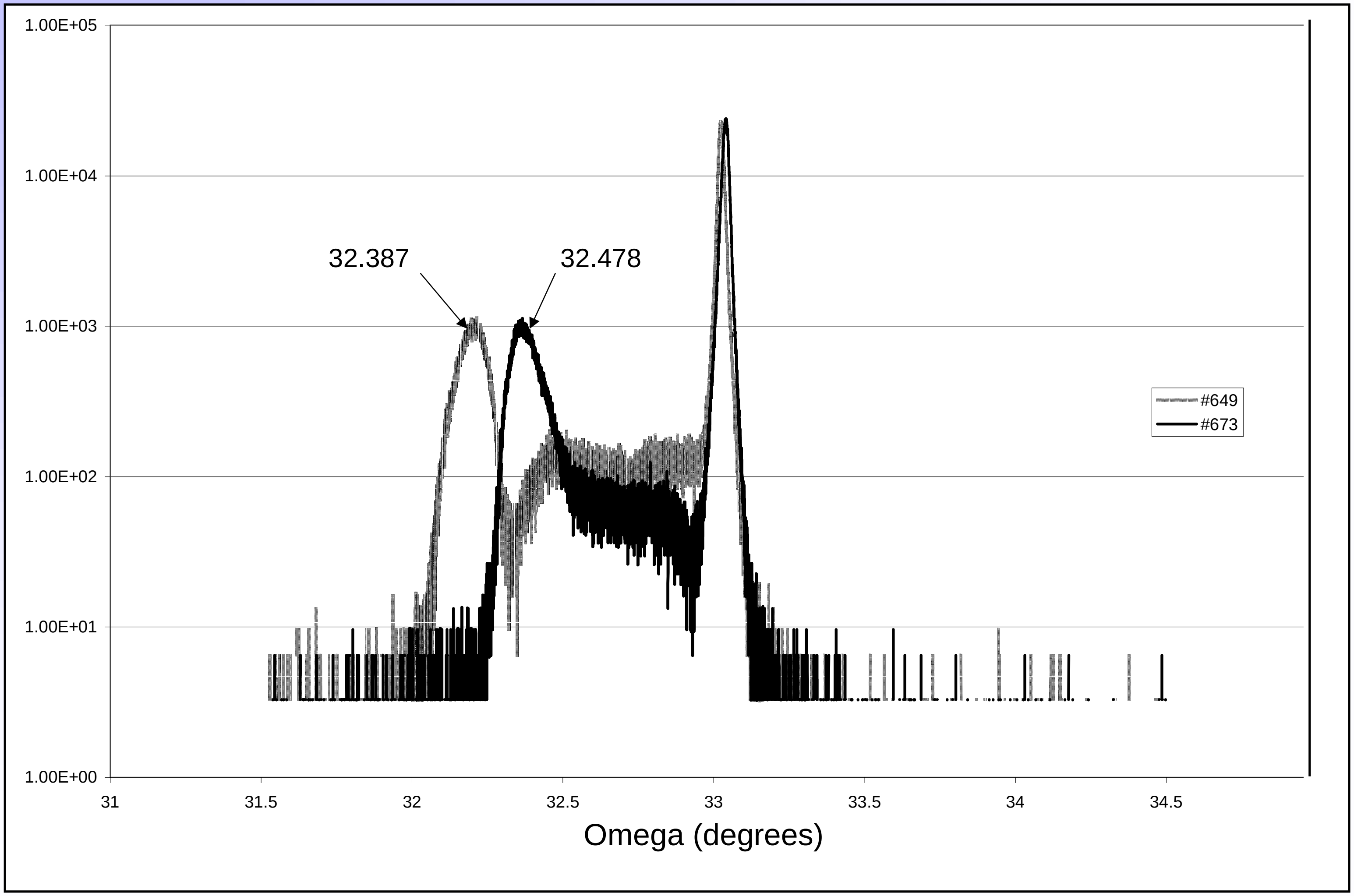

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Compositions- XRD & Transmission

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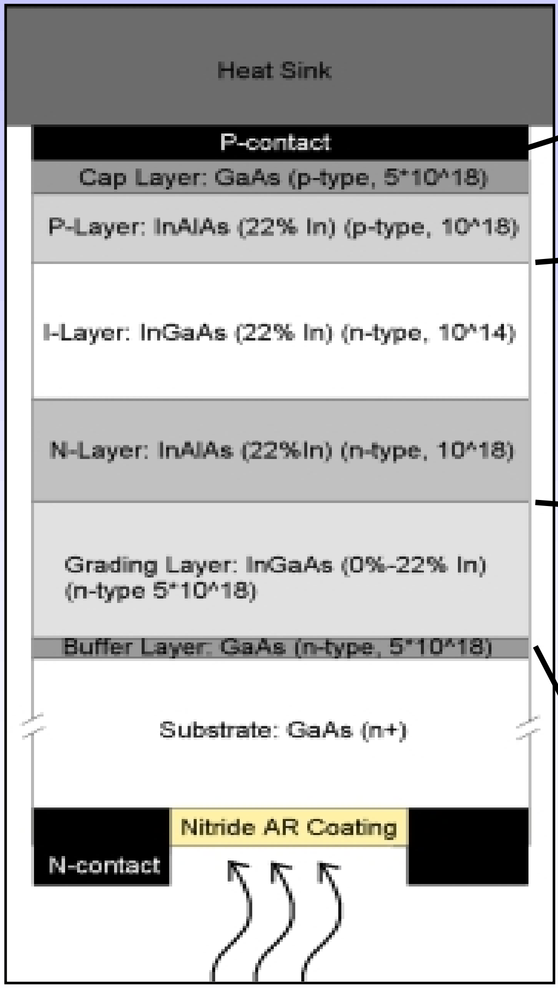
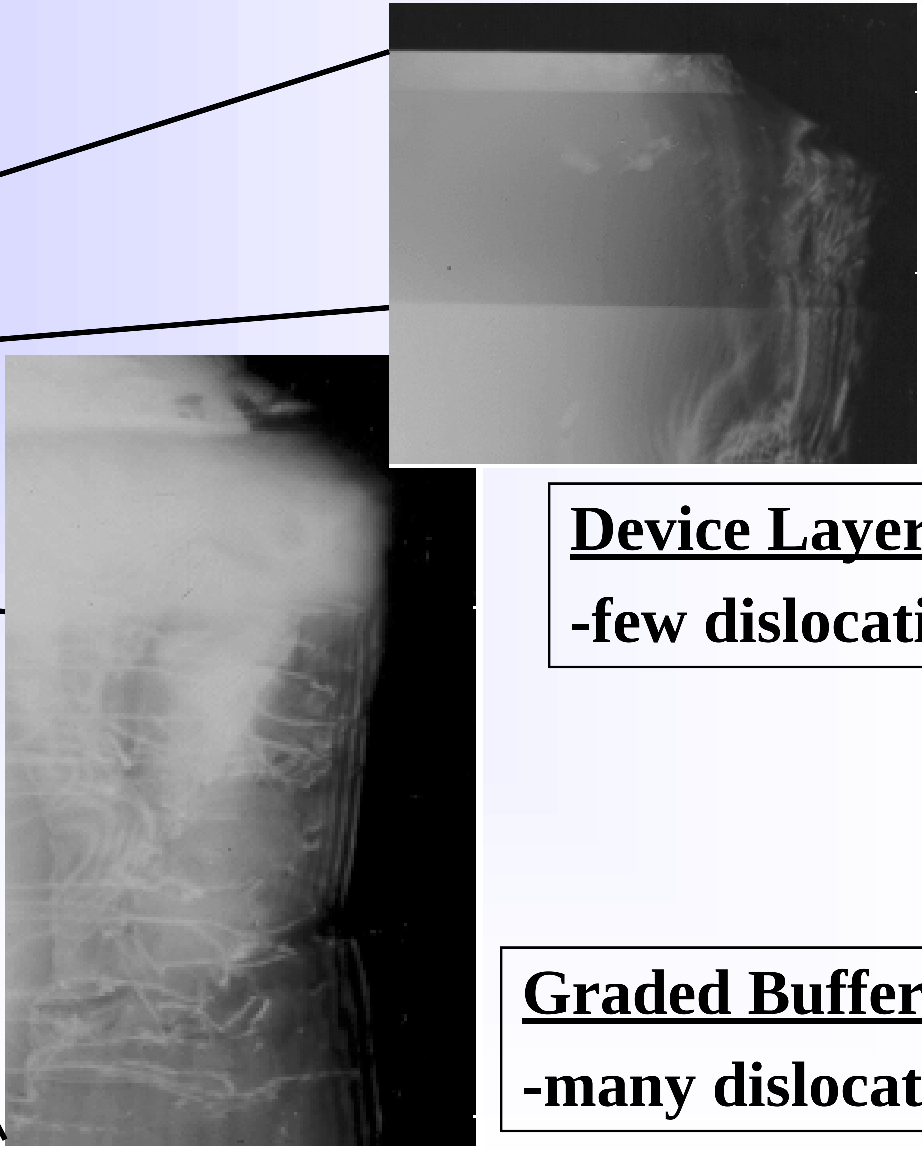
	XRD			Transmission		
	Omega (degrees)	Lattice Const. (Ang.)	In %	Abs. Edge (nm)	Band Gap (eV)	In %
#649	32.378	5.754	24.78%	1.20	1.03	36%
#673	32.478	5.748	20.90%	1.12	1.11	29%

TEM Images of Confined Dislocations


Heat Sink
P-contact
Cap Layer: GaAs (p-type, 5*10^18)
P-Layer: InAlAs (22% In) (p-type, 10^18)
I-Layer: InGaAs (22% In) (n-type, 10^14)
N-Layer: InAlAs (22%In) (n-type, 10^18)
Grading Layer: InGaAs (0%-22% In) (n-type 5*10^18)
Buffer Layer: GaAs (n-type, 5*10^18)
Substrate: GaAs (n+)
N-contact
Nitride AR Coating



Device Layers:

-few dislocations

Graded Buffer:

-many dislocations

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Absorption Data: #649 (w/ ARC)

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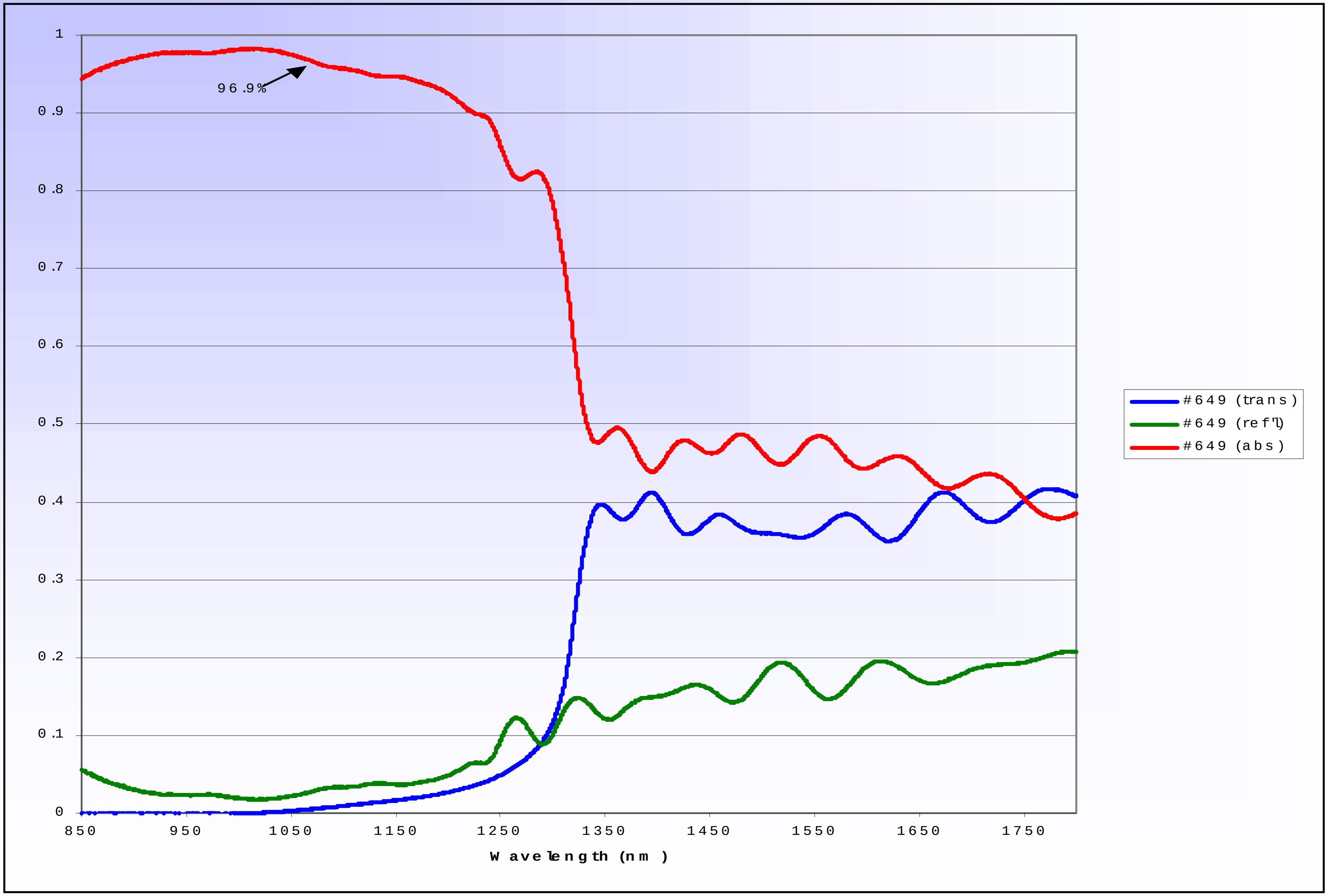

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GaAs Substrate Absorption

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