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GDS REFLECTIVE MEMORY ORGANIZATION

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Distribution of this draft:

DAQ and diagnostics system

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1 Introduction and Overview

This is a companion document to the “Data Acquisition System: Reflected Memory Network Design” (T980017-00) and details the organization of the part of the reflective memory which controlled by the GDS. One DAQ/GDS reflective memory ring is provided per interferometer (see Fig. 1 of T980017-00). The reflective memory is divided into a DAQ and a GDS section with a size of 2MB each (see Fig. 2 of T980017-00).

The reflective memory is subdivided into memory regions dedicated to specific data collection units (DCUs). Each DCU has a memory map which looks like:
following regions:

- interprocess communication area:
  Used to send messages and status information between DCUs and the DAQ system controller.
- data definition area:
  Used to describe the channels which are provided by the DCU.
- Data area:
  Used to store the data of individual channels. The data area is divided into equal length memory block, each holding 1/16 sec worth of data.

The diagnostics system together with the ISC system define 6 separate digital data collection units (DDCUs):

- DDCU for LSC
- DDCU for ASC
- DDCU for the LSC excitation channels
- DDCU for the ASC excitation channels
- DDCU for the LSC test output channels
- DDCU for the ASC test output channels

The DDCU for ASC and LSC follow the exact same layout as the analog data collection units (ADCUs) and, hence, need no further explanation. DDCUs for excitation and test output channels introduce the concept of test points which allow the selection of a subset of all available test inputs and outputs of the digital servo systems.

1.1 Data Definition Area Extensions

The basic concept of managing test points is that the data area is divided into a fixed number of channel slots which can be assigned to real channels on-the-fly. Exactly speaking, a test point configuration can only change at the GPS 1 sec boundary. To simplify the test point selection each test point has a unique number identifier. The data definition area is the divided into two regions: *(i)* a channel information area which is identical to the ones found in other DCUs with the exception that the channel names can change, and *(ii)* a lookup table which is located at the very end of the data definition area (last 256 bytes). At start-up the DAQ configuration manager loads the data definition area with a dummy set of channels and zeros out the lookup table; this automatically disables all test points.

Test points are the selected through a test point manager. The test point manager exports a test point API by implementing an rpc (remote procedure call) server. The test point manager will

update the data definition area in the 8th epoch[1] of every second. There is no notification when this happens, so each subsystem containing digital test points must update its internal data structures once every second. This information becomes valid for the next one second at the beginning of the 10 epoch and can be read from reflective memory until (and including) the 4 epoch of the second in which the test point information is valid. The test point manager updates both the channel information area and the lookup table. Additionally, it will update the channel count in the IPC area to reflect the actual number of used test points. The test point manager guarantees that test points are stored in a continuous data block (no holes). An empty channel name and a zero in the test point index indicates in inactive channel.

The lookup table is organized as a simple array of short integers (16 bit). Each entry holds the test point identification number of the corresponding data slot, i.e. table index 0 corresponds to the first slot, index 1 to the second slot, and so on. A test point identifier of zero indicates an inactive slot. The table length is determined by the number of data slots which are available in the DCU: 7 for LSC excitation channels, 15 for LSC test outputs, 28 for ASC excitation channels, and 60 for ASC test outputs.

A list of valid test point names and identifiers can be found in Section 2. A channel information structure (dataInfo) contains a ‘chNum’ field which is used by ADCUs to identify the ADC channel number. DDCUs with test points use this field to store the test point identifier.

1.2 Data Area Organization

The data area is divided into 8 equally sized data blocks each containing one epoch worth of data. The first block contains data corresponding the 0th or the 8th epochs, the second one contains data of the 1st or 9th epoch, and so on. This is also valid for test point DDCUs where the first data block contains either data obtained by the ISC digital servo during the first epoch, or data which has to be added to one of the excitation points during the first epoch. This requires that the excitation engine writes the excitation channel data of the 0th epoch no later than the 14th epoch of the previous second. This allows the ISC servo control to read the data in the 15th epoch and make it ready for adding in the 0th epoch. On the other hand test output data of the 0th epoch will be written to the corresponding data block in the 1st epoch. Ideally, the data acquisition system reads both the excitation and the test output channels in the 2nd epoch. The excitation channel data of the 0th epoch is then valid until the end of the 4th epoch, after it will be overwritten by data for the 8th epoch. Test output data of the 0th epoch will be valid until the end of the 8th epoch.

Within each data block the test point channel data is stored continuously, staring at slot 0. Channel data consists of a integer (32 bits) describing the validity of the channel, and an array of data points in single precision floating point format. For LSC test points the array length is 1024 points, whereas for ASC test points it is 128 points. This leads to a total length of 4100 bytes and 516 bytes, respectively.

1. A second is divided into 16 epochs, numbered from 0 to 15.

2 DIGITAL SERVO TEST POINTS

Test points (TP) are internal servo signals of digital subsystems and can be outputs or inputs. Outputs are used for reading out internal servo signals; they are written by the digital subsystem and read out by the DAQS. Inputs are used to inject excitations signals; they are written by the GDS excitation system and are read by both the digital subsystem and the DAQS.

Digital servo test points are used to perform the following functions:

1. Measure closed loop gains. These measurements are used for:
   - determination of phase and gain margins
   - adjustment of gains to achieve intended unity gain frequencies
   - diagnostic tests that make estimates of noise couplings (frequency noise, e.g.)
   - calibrations
2. Strain calibration, performed with various types of excitation:
   - swept sine
   - fixed sine(s)
   - pseudo-random noise
3. Measure cross-couplings:
   - length-length
   - length-angle
4. Measure sensing matrices:
   - alignment sensing
   - length sensing

2.1 TEST POINT INTERFACE

All digital test points are given an ID number and a corresponding dataInfo structure. The dataInfo structure definition follows that given in T980017-00, with the extensions mentioned in Section 1.2. Zero is an invalid TP ID. The ID numbers are grouped by subsystem and are separated into inputs and outputs; blocks of ID numbers are assigned as follows:

- 1 – 99: LSC; test inputs
- 100 – 499: LSC; test outputs
- 500 – 699: ASC; test inputs
- 700 – 1499: ASC; test outputs
- 2000 – 2099: excitation system DAC channels
- 3000 – 3099: excitation signals of stand-alone signal generators

The channel names and the ID numbers for all test points are given in Table 1 in Appendix A.

There are many more (potential) test points in digital subsystems than will ever be used simultaneously, so we define a (re)configurable subset which is deemed large enough to accommodate maximum usage of simultaneous test points:

- Rates: TPs can either be 16384 S/sec (16k) or 2048 S/sec (2k).
- Number: the TP subset allows a maximum of 16 16k and 64 2k TP channels.

Test point subsets are configured through a lookup table, which will list the TP ID#s for each data channel in the index. The size of the index is DCU dependent; unused channels are marked with 0.

2.2 Digital Subsystem Test Points

Loop gain measurements during servo operation can generally be made by forming the ratio between the signal after a summing junction and the injected test signal, giving $1/(1 + G)$, where G is the total open loop gain. In some cases, such as when correcting an error signal spectrum for loop gain, the value of $(1 + G)$ is desired. In other cases the value of G itself is desired; while this can be calculated from the above measurement, it can be directly measured by forming the ratio between the signals before and after the summing junction. For each sensed degree-of-freedom in a MIMO (multiple-input multiple-output) digital servo, we thus include a TP input with readouts before and after the summing point (typically the normal DAQ channel for that degree-of-freedom provides the readout before the summing point, and a TP output gives it after). Excitations to perform the other types of measurements listed in the Introduction can also be applied at these TP inputs. It is also useful to be able to excite degrees-of-freedom after the servo functions are applied, and TP inputs are supplied here in both the sensing and the individual mirror bases. Note that because the sensing basis is different from the mirror basis for each of the subsystems, there is generally no single test input that allows excitation of a single mirror within the servo band. However by applying an excitation simultaneously to several test inputs in the proper ratio, a given single optic can be stimulated.

For the two digital subsystems, the individual raw sensor signals are available as test points; these are the outputs from each photodetector channel, demodulated in two, (nearly)-orthogonal phases. Each signal corresponding to a given degree-of-freedom is provided to the DAQS for writing to frames. In between the signal types may be software for summing and/or mixing the two phases of the individual raw sensor signals; this is indicated by the box labeled Σ–ϕ in Figures 2–4.

2.2.1 LSC TPs

A block diagram of the digital portion of the LSC servo is shown in Figure 1. It shows the test points as well as the normal sensor and control outputs that the DAQS always stores to disk. In the LSC there are some instances of more than one control path for a given degree-of-freedom (in addition to the straightforward sensor-to-mirror basis rotation performed on all channels). Where there is a split in the control path, test inputs are inserted in each path at the split, and a test output is included just before the split. These allow for convenient measurement of the (open) loop gain of the individual paths (in combination with the total closed loop gain measurement).

2.2.2 ASC Test Points

A block diagram of the digital portion of the ASC servo is shown in Figure 2. The block diagram shows the current conception of how the wavefront sensor signals will be processed, and the test points have been chosen in this context. If some of the servo filters and rotation matrices are done differently, the test points may change.

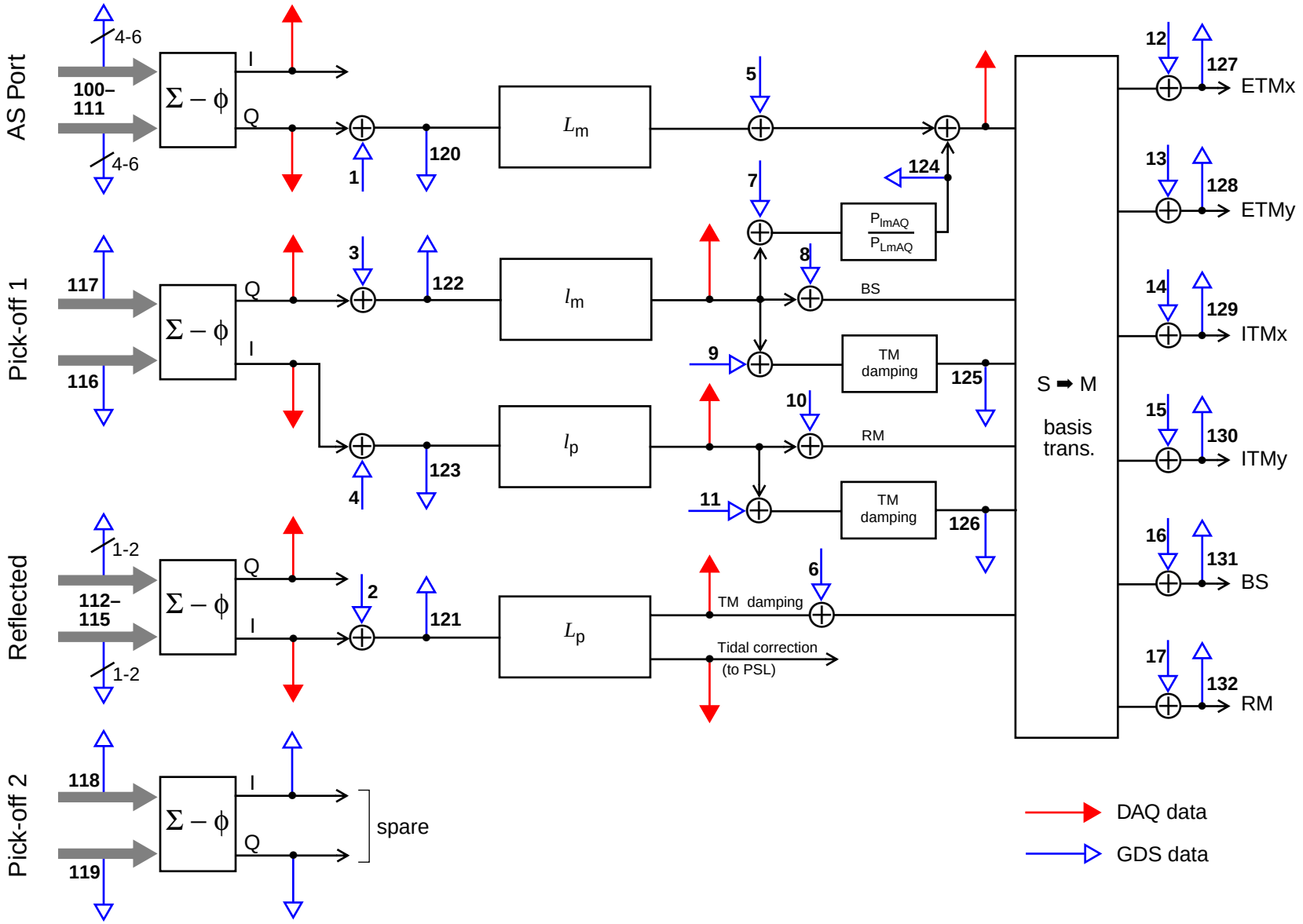

Figure 1: Digital portion of LSC servo, showing ID#s for test points.

Note: all TPs are pairs (for pitch & yaw), unless otherwise noted.

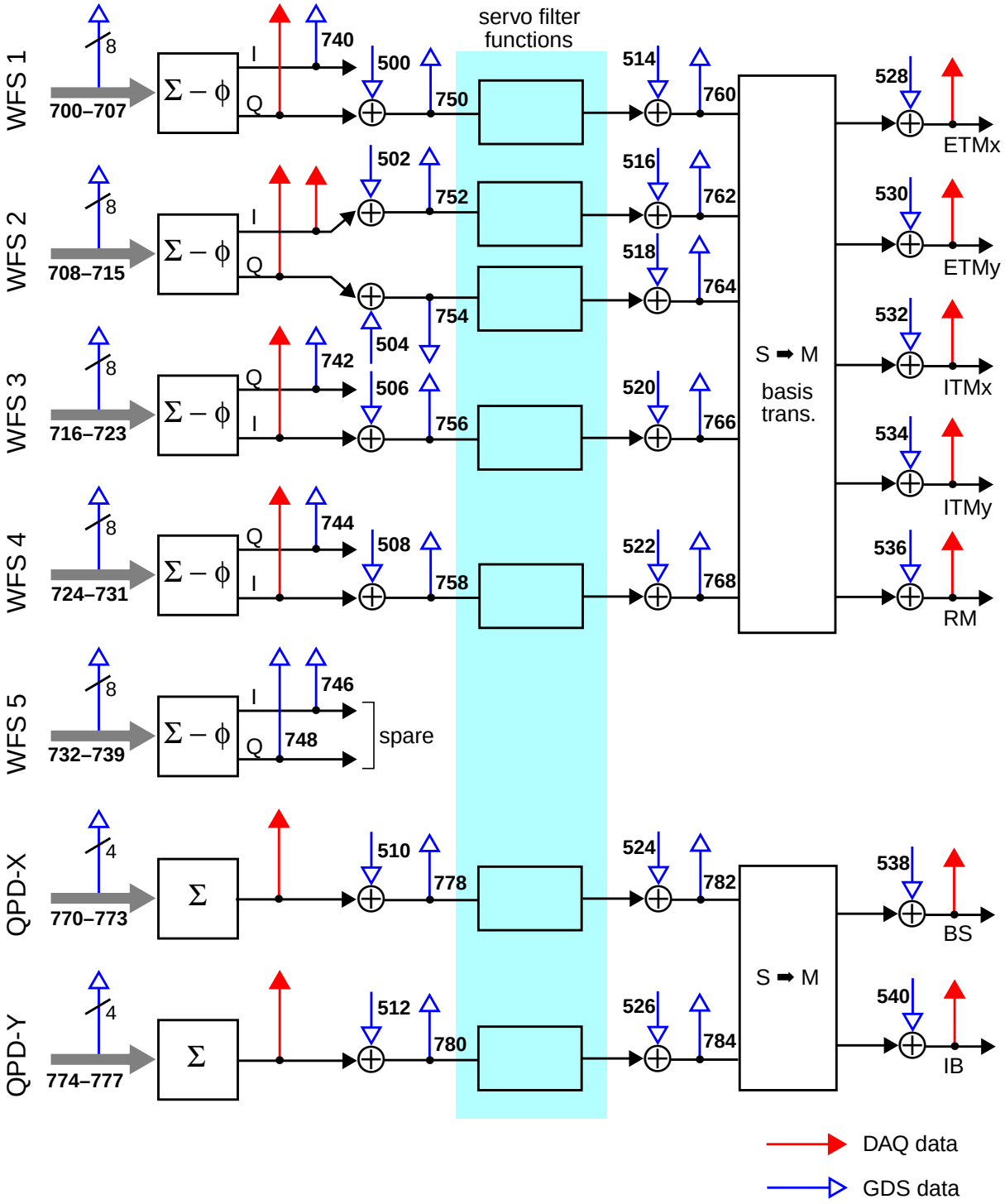

Figure 2: Digital portion of ASC servo, showing ID#s for test points (except for the raw sensor signals, only the even TP IDs, corresponding to the yaw signals, are shown).

APPENDIX A TEST POINT LIST

Test points which are currently supported are shown in bold.

Table 1: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
		0			invalid
H1	LSC	**1**	GW_EXC	16k	Test In, GW (L-) error signal
H1	LSC	**2**	REF_I_EXC	16k	Test In, Common arm (L+) error signal
H1	LSC	**3**	POX_Q_EXC	16k	Test In, Michelson (l-) error signal
H1	LSC	**4**	POX_I_EXC	16k	Test In, Recycling cav (l+) error signal
H1	LSC	**5**	DARM_EXC	16k	Test In, GW (L-) control signal
H1	LSC	**6**	CARM_EXC	16k	Test In, Comm arm (TM damping) control signal
H1	LSC	**7**	MICH3_EXC	16k	Test In, Michelson correction control signal
H1	LSC	**8**	MICH1_EXC	16k	Test In, Michelson beamsplitter control signal
H1	LSC	**9**	MICH2_EXC	16k	Test In, Mich. TM damping control signal
H1	LSC	**10**	REC1_EXC	16k	Test In, Rec cav, rec mirror control signal
H1	LSC	**11**	REC2_EXC	16k	Test In, Rec cav, TM damping control signal
H1	LSC	**12**	ETMX_EXC	16k	Test In, End Test Mass, X arm
H1	LSC	**13**	ETMY_EXC	16k	Test In, End Test Mass, Y arm
H1	LSC	**14**	ITMX_EXC	16k	Test In, Input Test Mass, X arm
H1	LSC	**15**	ITMY_EXC	16k	Test In, Input Test Mass, Y arm
H1	LSC	**16**	BS_EXC	16k	Test In, Beamsplitter
H1	LSC	**17**	RM_EXC	16k	Test In, Recycling mirror
H1	LSC	100	AS1_I	16k	anti-symmetric port, diode 1, I-phase
H1	LSC	101	AS1_Q	16k	anti-symmetric port, diode 1, Q-phase
H1	LSC	102	AS2_I	16k	anti-symmetric port, diode 2, I-phase
H1	LSC	103	AS2_Q	16k	anti-symmetric port, diode 2, Q-phase
H1	LSC	104	AS3_I	16k	anti-symmetric port, diode 3, I-phase
H1	LSC	105	AS3_Q	16k	anti-symmetric port, diode 3, Q-phase
H1	LSC	106	AS4_I	16k	anti-symmetric port, diode 4, I-phase
H1	LSC	107	AS4_Q	16k	anti-symmetric port, diode 4, Q-phase
H1	LSC	108	AS5_I	16k	anti-symmetric port, diode 5, I-phase
H1	LSC	109	AS5_Q	16k	anti-symmetric port, diode 5, Q-phase
H1	LSC	110	AS6_I	16k	anti-symmetric port, diode 6, I-phase
H1	LSC	111	AS6_Q	16k	anti-symmetric port, diode 6, Q-phase
H1	LSC	112	RFL1_I	16k	reflection port, diode 1, I-phase
H1	LSC	113	REF1_Q	16k	reflection port, diode 1, Q-phase
H1	LSC	114	REF2_I	16k	reflection port, diode 2, I-phase
H1	LSC	115	REF2_Q	16k	reflection port, diode 2, Q-phase

Table 1: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
H1	LSC	116	POX1_I	16k	RC pick-off from ITM X, I-phase
H1	LSC	117	POX1_Q	16k	RC pick-off from ITM X, Q-phase
H1	LSC	**118**	POY1_I	16k	RC pick-off from ITM Y, I-phase
H1	LSC	**119**	POY1_Q	16k	RC pick-off from ITM Y, Q-phase
H1	LSC	**120**	GW_TO	16k	Test Out, GW (L-) error signal (after sum junction)
H1	LSC	**121**	REF_TO	16k	Test Out, Com arm (L+) error sig (after sum junc.)
H1	LSC	**122**	POX_Q_TO	16k	Test Out, Mich (l-) error signal (after sum junction)
H1	LSC	**123**	POX_I_TO	16k	Test Out, Rec cav (l+) error sig (after sum junc.)
H1	LSC	**124**	MICH3_TO	16k	Test Out, Michelson correction control signal
H1	LSC	**125**	MICH2_TO	16k	Test Out, Mich. TM damping control signal
H1	LSC	**126**	REF2_TO	16k	Test Out, Rec cav TM damping control signal
H1	LSC	**127**	ETMX_TO	16k	Test Out, End Test Mass, X arm (after sum junc.)
H1	LSC	**128**	ETMY_TO	16k	Test Out, End Test Mass, Y arm (after sum junc.)
H1	LSC	**129**	ITMX_TO	16k	Test Out, Input Test Mass, X arm (after sum junc.)
H1	LSC	**130**	ITMY_TO	16k	Test Out, Input Test Mass, Y arm (after sum junc.)
H1	LSC	**131**	BS_TO	16k	Test Out, Beamsplitter (after sum junc.)
H1	LSC	**132**	RM_TO	16k	Test Out, Recycling mirror (after sum junc.)
H1	ASC	**500**	WFS1_QY1_EXC	2k	Test In, wavefront sensor 1 yaw error signal
H1	ASC	**501**	WFS1_QP1_EXC	2k	Test In, wavefront sensor 1 pitch error signal
H1	ASC	**502**	WFS2_IY1_EXC	2k	Test In, wavefront sensor 2a yaw error signal
H1	ASC	**503**	WFS2_IP1_EXC	2k	Test In, wavefront sensor 2a pitch error signal
H1	ASC	**504**	WFS2_QY1_EXC	2k	Test In, wavefront sensor 2a yaw error signal
H1	ASC	**505**	WFS2_QP1_EXC	2k	Test In, wavefront sensor 2b pitch error signal
H1	ASC	**506**	WFS3_IY1_EXC	2k	Test In, wavefront sensor 3 yaw error signal
H1	ASC	**507**	WFS3_IP1_EXC	2k	Test In, wavefront sensor 3 pitch error signal
H1	ASC	**508**	WFS4_IY1_EXC	2k	Test In, wavefront sensor 4 yaw error signal
H1	ASC	**509**	WFS4_IP1_EXC	2k	Test In, wavefront sensor 4 pitch error signal
H1	ASC	**510**	QPDX_Y1_EXC	2k	Test In, X-arm quad. pos. sensor yaw error signal
H1	ASC	**511**	QPDX_P1_EXC	2k	Test In,X-arm quad. pos. sensor pitch error signal
H1	ASC	**512**	QPDY_Y1_EXC	2k	Test In, Y-arm quad. pos. sensor yaw error signal
H1	ASC	**513**	QPDY_P1_EXC	2k	Test In,Y-arm quad. pos. sensor pitch error signal
H1	ASC	**514**	WFS1_QY2_EXC	2k	Test In, wavefront sensor 1 yaw control signal
H1	ASC	**515**	WFS1_QP2_EXC	2k	Test In, wavefront sensor 1 pitch controlr signal
H1	ASC	**516**	WFS2_IY2_EXC	2k	Test In, wavefront sensor 2a yaw control signal
H1	ASC	**517**	WFS2_IP2_EXC	2k	Test In, wavefront sensor 2a pitch control signal
H1	ASC	**518**	WFS2_QY2_EXC	2k	Test In, wavefront sensor 2a yaw control signal
H1	ASC	**519**	WFS2_QP2_EXC	2k	Test In, wavefront sensor 2b pitch control signal
H1	ASC	**520**	WFS3_IY2_EXC	2k	Test In, wavefront sensor 3 yaw control signal
H1	ASC	**521**	WFS3_IP2_EXC	2k	Test In, wavefront sensor 3 pitch control signal
H1	ASC	**522**	WFS4_IY2_EXC	2k	Test In, wavefront sensor 4 yaw control signal

Table 1: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
H1	ASC	**523**	WFS4_IP2_EXC	2k	Test In, wavefront sensor 4 pitch control signal
H1	ASC	**524**	QPDX_Y2_EXC	2k	Test In, X-arm quad. pos. sensor yaw control sig.
H1	ASC	**525**	QPDX_P2_EXC	2k	Test In,X-arm quad. pos. sensor pitch control sig.
H1	ASC	**526**	QPDY_Y2_EXC	2k	Test In, Y-arm quad. pos. sensor yaw control sig.
H1	ASC	**527**	QPDY_P2_EXC	2k	Test In,Y-arm quad. pos. sensor pitch control sig.
H1	ASC	**528**	ETMX_Y_EXC	2k	Test In, End test mass, X arm, yaw angle
H1	ASC	**529**	ETMX_P_EXC	2k	Test In, End test mass, X arm, pitch angle
H1	ASC	**530**	ETMY_Y_EXC	2k	Test In, End test mass, Y arm, yaw angle
H1	ASC	**531**	ETMY_P_EXC	2k	Test In, End test mass, Y arm, pitch angle
H1	ASC	**532**	ITMX_Y_EXC	2k	Test In, Input test mass, X arm, yaw angle
H1	ASC	**533**	ITMX_P_EXC	2k	Test In, Input test mass, X arm, pitch angle
H1	ASC	**534**	ITMY_Y_EXC	2k	Test In, Input test mass, Y arm, yaw angle
H1	ASC	**535**	ITMY_P_EXC	2k	Test In, Input test mass, Y arm, pitch angle
H1	ASC	**536**	RM_Y_EXC	2k	Test In, Recycling mirror, yaw angle
H1	ASC	**537**	RM_P_EXC	2k	Test In, Recycling mirror, pitch angle
H1	ASC	**538**	BS_Y_EXC	2k	Test In, Beamsplitter, yaw angle
H1	ASC	**539**	BS_P_EXC	2k	Test In, Beamsplitter, pitch angle
H1	ASC	**540**	IB_Y_EXC	2k	Test In, Input beam, yaw angle
H1	ASC	**541**	IB_P_EXC	2k	Test In, Input beam, pitch angle
H1	ASC	**700**	WFS1_I1	2k	wavefront sensor 1, channel 1, I-phase
H1	ASC	**701**	WFS1_I2	2k	wavefront sensor 1, channel 2, I-phase
H1	ASC	**702**	WFS1_I3	2k	wavefront sensor 1, channel 3, I-phase
H1	ASC	**703**	WFS1_I3	2k	wavefront sensor 1, channel 4, I-phase
H1	ASC	**704**	WFS1_Q1	2k	wavefront sensor 1, channel 1, Q-phase
H1	ASC	**705**	WFS1_Q2	2k	wavefront sensor 1, channel 2, Q-phase
H1	ASC	**706**	WFS1_Q3	2k	wavefront sensor 1, channel 3, QI-phase
H1	ASC	**707**	WFS1_Q4	2k	wavefront sensor 1, channel 4, Q-phase
H1	ASC	**708**	WFS2_I1	2k	wavefront sensor 2, channel 1, I-phase
H1	ASC	**709**	WFS2_I2	2k	wavefront sensor 2, channel 2, I-phase
H1	ASC	**710**	WFS2_I3	2k	wavefront sensor 2, channel 3, I-phase
H1	ASC	**711**	WFS2_I4	2k	wavefront sensor 2, channel 4, I-phase
H1	ASC	**712**	WFS2_Q1	2k	wavefront sensor 2, channel 1, Q-phase
H1	ASC	**713**	WFS2_Q2	2k	wavefront sensor 2, channel 2, Q-phase
H1	ASC	**714**	WFS2_Q3	2k	wavefront sensor 2, channel 3, Q-phase
H1	ASC	**715**	WFS2_Q4	2k	wavefront sensor 2, channel 4, Q-phase
H1	ASC	**716**	WFS3_I1	2k	wavefront sensor 3, channel 1, I-phase
H1	ASC	**717**	WFS3_I2	2k	wavefront sensor 3, channel 2, I-phase
H1	ASC	**718**	WFS3_I3	2k	wavefront sensor 3, channel 3, I-phase
H1	ASC	**719**	WFS3_I4	2k	wavefront sensor 3, channel 4, I-phase
H1	ASC	**720**	WFS3_Q1	2k	wavefront sensor 3, channel 1, Q-phase
H1	ASC	**721**	WFS3_Q2	2k	wavefront sensor 3, channel 2, Q-phase

Table 1: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
H1	ASC	**722**	WFS3_Q3	2k	wavefront sensor 3, channel 3, Q-phase
H1	ASC	**723**	WFS3_Q4	2k	wavefront sensor 3, channel 4, Q-phase
H1	ASC	**724**	WFS4_I1	2k	wavefront sensor 4, channel 1, I-phase
H1	ASC	**725**	WFS4_I2	2k	wavefront sensor 4, channel 2, I-phase
H1	ASC	**726**	WFS4_I3	2k	wavefront sensor 4, channel 3, I-phase
H1	ASC	**727**	WFS4_I4	2k	wavefront sensor 4, channel 4, I-phase
H1	ASC	**728**	WFS4_Q1	2k	wavefront sensor 4, channel 1, Q-phase
H1	ASC	**729**	WFS4_Q2	2k	wavefront sensor 4, channel 2, Q-phase
H1	ASC	**730**	WFS4_Q3	2k	wavefront sensor 4, channel 3, Q-phase
H1	ASC	**731**	WFS4_Q4	2k	wavefront sensor 4, channel 4, Q-phase
H1	ASC	**732**	WFS5_I1	2k	wavefront sensor 5, channel 1, I-phase
H1	ASC	**733**	WFS5_I2	2k	wavefront sensor 5, channel 2, I-phase
H1	ASC	**734**	WFS5_I3	2k	wavefront sensor 5, channel 3, I-phase
H1	ASC	**735**	WFS5_I4	2k	wavefront sensor 5, channel 4, I-phase
H1	ASC	**736**	WFS5_Q1	2k	wavefront sensor 5, channel 1, Q-phase
H1	ASC	**737**	WFS5_Q2	2k	wavefront sensor 5, channel 2, Q-phase
H1	ASC	**738**	WFS5_Q3	2k	wavefront sensor 5, channel 3, Q-phase
H1	ASC	**739**	WFS5_Q4	2k	wavefront sensor 5, channel 4, Q-phase
H1	ASC	**740**	WFS1_IY	2k	wavefront sensor 1, yaw signal, I-phase
H1	ASC	**741**	WFS1_IP	2k	wavefront sensor 1, pitch signal, I-phase
H1	ASC	**742**	WFS3_QY	2k	wavefront sensor 3, yaw signal, Q-phase
H1	ASC	**743**	WFS3_QP	2k	wavefront sensor 3, pitch signal, Q-phase
H1	ASC	**744**	WFS4_QY	2k	wavefront sensor 4, yaw signal, Q-phase
H1	ASC	**745**	WFS4_QP	2k	wavefront sensor 4, pitch signal, Q-phase
H1	ASC	**746**	WFS5_IY	2k	wavefront sensor 5, yaw signal, I-phase
H1	ASC	**747**	WFS5_IP	2k	wavefront sensor 5, pitch signal, I-phase
H1	ASC	**748**	WFS5_QY	2k	wavefront sensor 5, yaw signal, Q-phase
H1	ASC	**749**	WFS5_QP	2k	wavefront sensor 5, pitch signal, Q-phase
H1	ASC	**750**	WFS1_QY1_TO	2k	Test Out, wavefront sensor 1 yaw error signal
H1	ASC	**751**	WFS1_QP1_TO	2k	Test Out, wavefront sensor 1 pitch error signal
H1	ASC	**752**	WFS2_IY1_TO	2k	Test Out, wavefront sensor 2a yaw error signal
H1	ASC	**753**	WFS2_IP1_TO	2k	Test Out, wavefront sensor 2a pitch error signal
H1	ASC	**754**	WFS2_QY1_TO	2k	Test Out, wavefront sensor 2a yaw error signal
H1	ASC	**755**	WFS2_QP1_TO	2k	Test Out, wavefront sensor 2b pitch error signal
H1	ASC	**756**	WFS3_IY1_TO	2k	Test Out, wavefront sensor 3 yaw error signal
H1	ASC	**757**	WFS3_IP1_TO	2k	Test Out, wavefront sensor 3 pitch error signal
H1	ASC	**758**	WFS4_IY1_TO	2k	Test Out, wavefront sensor 4 yaw error signal
H1	ASC	**759**	WFS4_IP1_TO	2k	Test Out, wavefront sensor 4 pitch error signal
H1	ASC	**760**	WFS1_QY2_TO	2k	Test Out, wavefront sensor 1 yaw control signal
H1	ASC	**761**	WFS1_QP2_TO	2k	Test Out, wavefront sensor 1 pitch control signal
H1	ASC	**762**	WFS2_IY2_TO	2k	Test Out, wavefront sensor 2a yaw control signal
H1	ASC	**763**	WFS2_IP2_TO	2k	Test Out, wavefront sensor 2a pitch control signal
H1	ASC	**764**	WFS2_QY2_TO	2k	Test Out, wavefront sensor 2a yaw control signal

Table 1: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
H1	ASC	**765**	WFS2_QP2_TO	2k	Test Out, wavefront sensor 2b pitch control signal
H1	ASC	**766**	WFS3_IY2_TO	2k	Test Out, wavefront sensor 3 yaw control signal
H1	ASC	**767**	WFS3_IP2_TO	2k	Test Out, wavefront sensor 3 pitch control signal
H1	ASC	**768**	WFS4_IY2_TO	2k	Test Out, wavefront sensor 4 yaw control signal
H1	ASC	**769**	WFS4_IP2_TO	2k	Test Out, wavefront sensor 4 pitch control signal
H1	ASC	**770**	QPDX_1	2k	quadrant position sensor, channel 1, X arm
H1	ASC	**771**	QPDX_2	2k	quadrant position sensor, channel 2, X arm
H1	ASC	**772**	QPDX_3	2k	quadrant position sensor, channel 3, X arm
H1	ASC	**773**	QPDX_4	2k	quadrant position sensor, channel 4, X arm
H1	ASC	**774**	QPDY_1	2k	quadrant position sensor, channel 1, Y arm
H1	ASC	**775**	QPDY_2	2k	quadrant position sensor, channel 2, Y arm
H1	ASC	**776**	QPDY_3	2k	quadrant position sensor, channel 3, Y arm
H1	ASC	**777**	QPDY_4	2k	quadrant position sensor, channel 4, Y arm
H1	ASC	**778**	QPDX_Y1_TO	2k	Test Out, X-arm QPD yaw error signal
H1	ASC	**779**	QPDX_P1_TO	2k	Test Out, X-arm QPD pitch error signal
H1	ASC	**780**	QPDY_Y1_TO	2k	Test Out, Y-arm QPD yaw error signal
H1	ASC	**781**	QPDY_P1_TO	2k	Test Out, Y-arm QPD pitch error signal
H1	ASC	**782**	QPDX_Y2_TO	2k	Test Out, X-arm QPD yaw control signal
H1	ASC	**783**	QPDX_P2_TO	2k	Test Out, X-arm QPD pitch control signal
H1	ASC	**784**	QPDY_Y2_TO	2k	Test Out, Y-arm QPD yaw control signal
H1	ASC	**785**	QPDY_P2_TO	2k	Test Out, Y-arm QPD pitch control signal
H1	LSC	**2000**	MOD_1_EXC	16k	modulation input of rf generator, sidebands
H1	LSC	**2001**	MOD_2_EXC	16k	modulation input of rf generator, non-res. SBs
H1	LSC	**2002**	MOD_3_EXC	16k	modulation input of rf generator, MC sidebands
H1	IOO	**2003**	MC_I_EXC	16k	modecleaner error signal offset
H1	IOO	**2004**	MC_L_EXC	16k	modecleaner length offset
H1	IOO	**2005**	MC_1_EXC	16k	after servo split, MC path
H1	IOO	**2006**	MC_2_EXC	16k	after servo split, laser path
H1	IOO	**2007**	WFS1_Y_EXC	16k	MC WFS 1, yaw offset
H1	IOO	**2008**	WFS1_P_EXC	16k	MC WFS 1, pitch offset
H1	IOO	**2009**	WFS2_Y_EXC	16k	MC WFS 2, yaw offset
H1	IOO	**2010**	WFS2_P_EXC	16k	MC WFS 2, pitch offset
H1	IOO	**2011**	IB1_Y_EXC	16k	input beam PZT 1, yaw offset
H1	IOO	**2012**	IB1_P_EXC	16k	input beam PZT 1, pitch offset
H1	IOO	**2013**	IB2_Y_EXC	16k	input beam PZT 2, yaw offset
H1	IOO	**2014**	IB2_P_EXC	16k	input beam PZT 2, pitch offset
H1	IOO	**2015**	MMT1_EXC	16k	mode matching mirror 1 offset
H1	IOO	**2016**	MMT2_EXC	16k	mode matching mirror 2 offset
H1	IOO	**2017**	MMT3_EXC	16k	mode matching mirror 3 offset
H1	PSL	**2018**	AOM_F_EXC	16k	laser frequency offset, AOM

Table 1: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
H1	PSL	**2019**	PWR_1_EXC	16k	laser power modulation
H1	PSL	**2020**	PMC_I_EXC	16k	pre-mode cleaner offset
H0	GDS	**2021**	LVEA1_TI1_EXC	16k	temporary test input, LVEA 4K
H0	GDS	**2022**	LVEA1_TI2_EXC	16k	temporary test input, LVEA 4K
H0	GDS	**2023**	LVEA1_TI3_EXC	16k	temporary test input, LVEA 4K
H0	GDS	**2024**	LVEA1_TI4_EXC	16k	temporary test input, LVEA 4K
H1	LSC	**2100**	ETMX_CAL_EXC	16k	calibration signal ETMX
H0	GDS	**2101**	EX_TI1_EXC	16k	temporary test input, X end station
H0	GDS	**2102**	EX_TI2_EXC	16k	temporary test input, X end station
H0	GDS	**2103**	EX_TI3_EXC	16k	temporary test input, X end station
H1	LSC	**2200**	ETMY_CAL_EXC	16k	calibration signal ETMY
H0	GDS	**2101**	EY_TI1_EXC	16k	temporary test input, Y end station
H0	GDS	**2102**	EY_TI2_EXC	16k	temporary test input, Y end station
H0	GDS	**2103**	EY_TI3_EXC	16k	temporary test input, Y end station

APPENDIX B TEST POINT MANAGER

B.1 CONSTANTS

Useful constants and macros for dealing with the reflective memory layout of test point DDCUs are defined in ‘rmorg.h’. More detailed information can be found in the corresponding web page.

B.2 API

The test point API is defined in the ‘testpoint.h’ header file. This API provides functions to reserve and activate test points, functions to remove test points, and functions to query the configuration of the test point manager. On a CPU which has direct access to reflective memory the test point information of active test points is read in directly, on all other machines the information is obtained from the test point manager through remote procedure calls. Requesting and removing test points is always done through the test point manager. More detailed information can be found in the corresponding web page.