LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
- LIGO -
CALIFORNIA INSTITUTE OF TECHNOLOGY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Document Type	**LIGO-T970139-00 - C**	7/20/97

LSC CDS Conceptual Design

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Distribution of this draft:

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1 INTRODUCTION

The LSC subsystem provides for all aspects of interferometer length control involved in maintaining the signal sensitivity required for LIGO. This includes:

- Support for the Lock Acquisition, Detection, Calibration and Diagnostics Modes of operation.
- The photodetectors and related protective hardware.
- RF source, phase shifters, mixers, cabling.
- LSC control electronics, and signal processing software used in the feedback control portion of the servo loops.
- Any hardware and/or algorithms for calibrating the gravity wave readout.

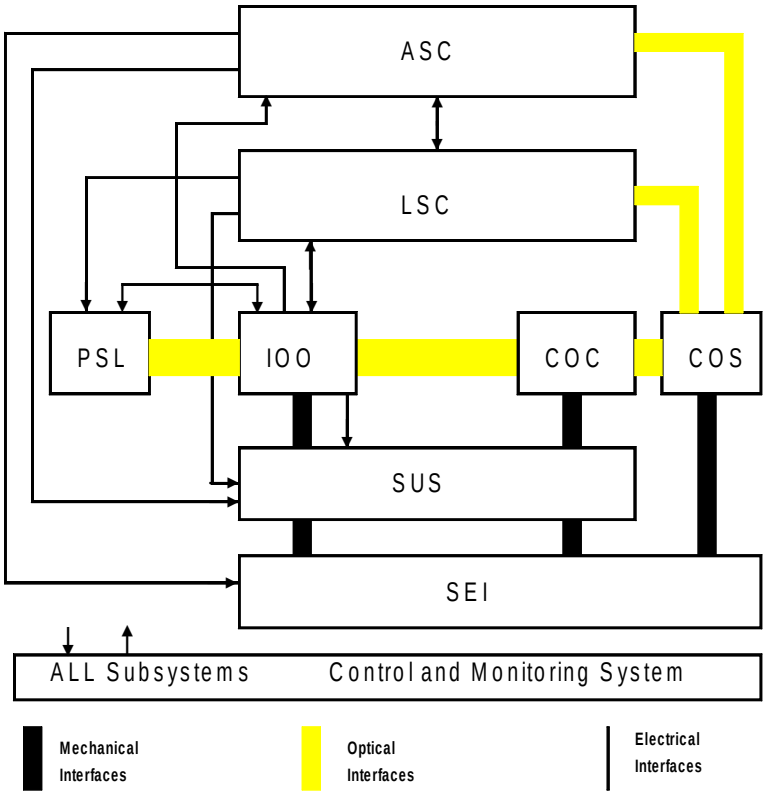
Not included in the LSC scope is any aspect of the performance of the LIGO optics, interferometer alignment, production of light or actuation of input light stabilization. It does not include the suspension or seismic isolation actuators, beam shaping optics, vacuum system viewports or hardware, or phase modulators. It also does not include the suspension control actuators in the feedback path which drive the suspended optics.

We present here a conceptual design for the CDS portion of the Length Sensing and Control system. Many aspects of this derive from the LSC PDR (LIGO-T970122-00).

2 LSC SUBSYSTEM DESCRIPTION

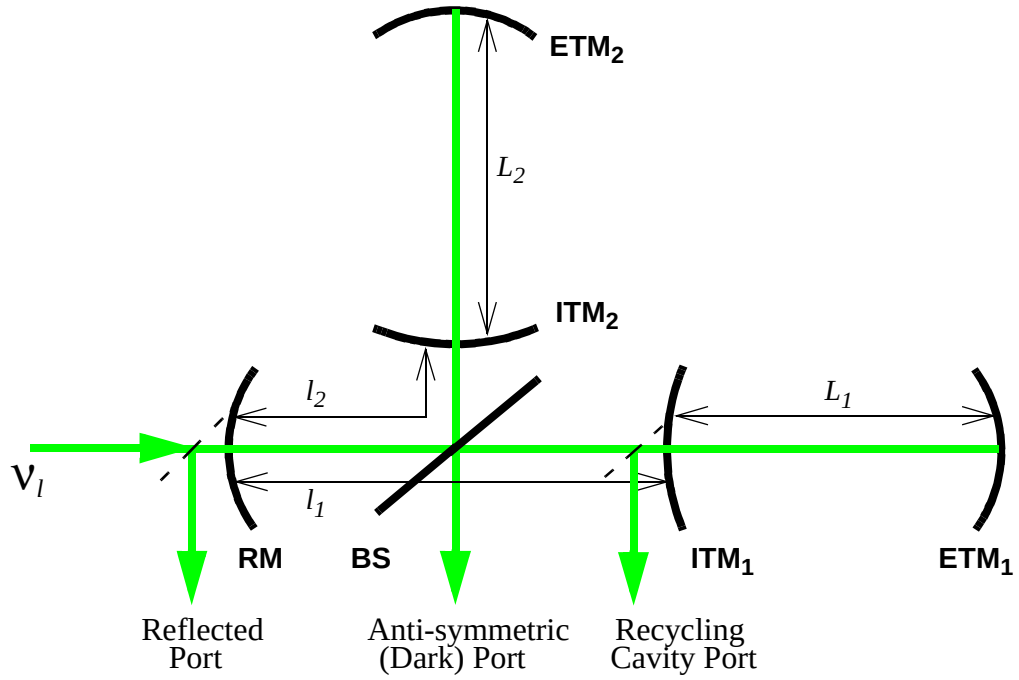
The initial LIGO detector system consists of three power-recycled Michelson interferometers with Fabry-Perot cavity arms, a 2 Km and 4 Km interferometer at Hanford and a 4 Km interferometer at Livingston. The LSC subsystem provides the control to bring the interferometer lengths to resonance with the light source, sense deviations from resonance and apply the necessary corrections to the Suspension Subsystem (SUS) to cancel them. The LSC also provides a control loop correction to tune the laser frequency of the prestabilized laser (PSL) and provide the calibrated gravity wave readout to the Data Acquisition subsystem (DAQ). This document is part of an overall LIGO detector requirement specification tree. Refer to the SYS DRD for a diagram of the tree.

2.1. Subsystem Block Diagram



2.2. Control System Definitions

The following two figures are taken from the LSC PDR and are included here for reference only.



Name	*Symbol*	*Definition*	*Deviation Symbol*
Differential Arm Length	L_-	$L_1 - L_2$	δL_-
Common Arm Length	L_+	$L_1 + L_2$	δL_+
Michelson Length	l_-	$l_1 - l_2$	δl_-
Recycling Cavity Length	l_+	$l_1 + l_2$	δl_+
Michelson Asymmetry	Δl	$(l_1 - l_2)/2$	N.A.

Figure 1 Definitions of length degrees-of-freedom and output ports. 'ITM' stands for input test mass, 'ETM' for end test mass, 'BS' for beamsplitter, and 'RM' for recycling mirror. The frequency, wavelength and propagation constant of the laser light is denoted by ν_l, λ_l, and k_l respectively.

2.3. Control System Configuration

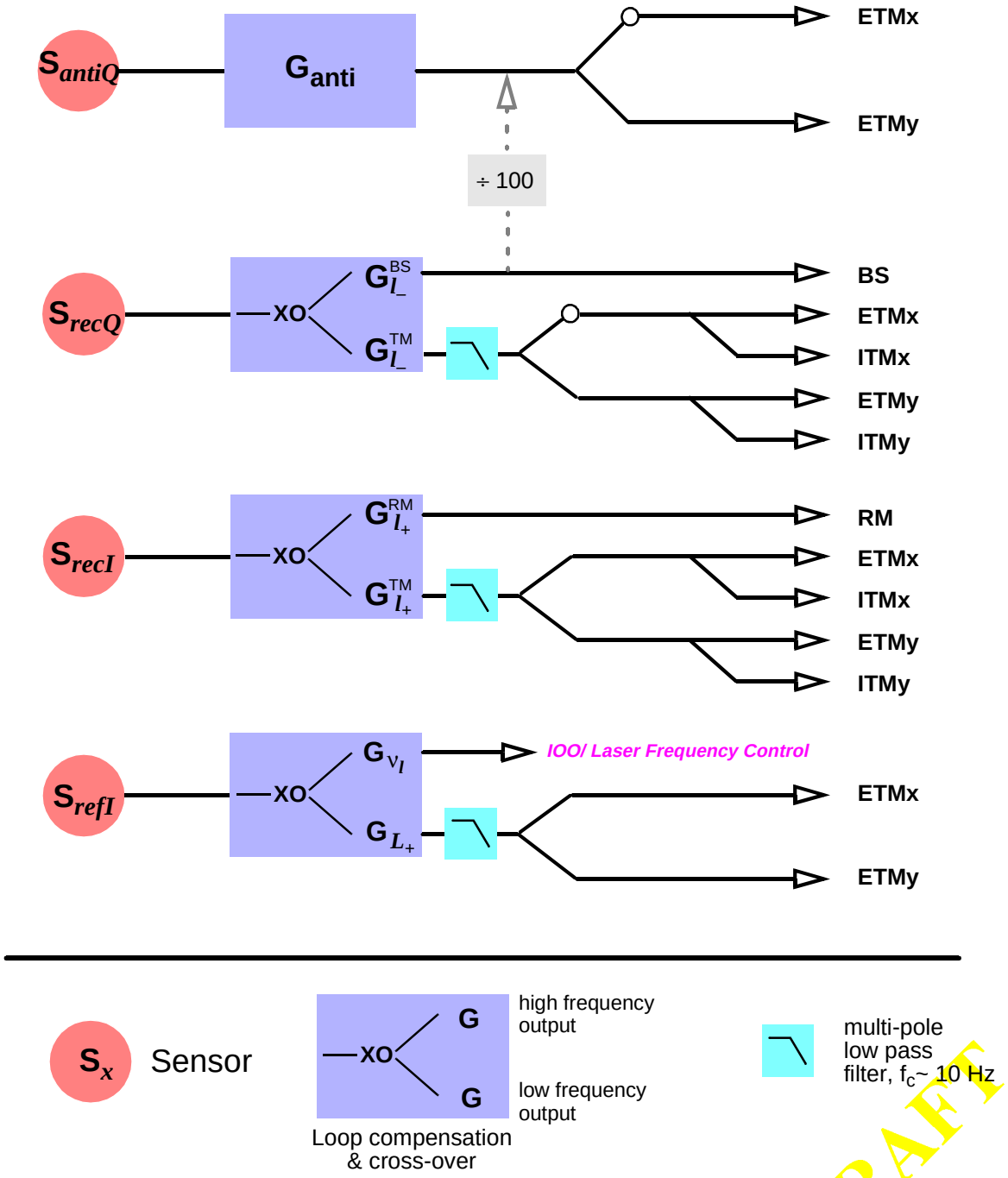


Figure 2: Sensing & control configuration diagram. For all loops other than the gravity wave channel (top), the sensor signals are fed to the test masses at low frequencies (to damp the pendula), and are crossed over to the beamsplitter, recycling mirror and laser frequency actuator at higher frequencies; the cross-over frequency will be 1-2 Hz. The test mass path is low-pass filtered at ~10× the cross-over frequency in order to eliminate the sensor noise from the gravity wave channel. Also shown is an optional control path that adds approximately 1/100 of the Michelson control signal to the L_- control signal in order to further reduce the contribution of the Michelson sensing noise in the gravity wave channel.

2.4. Modes of Operation

The LSC CDS shall be capable of supporting the operational modes described below.

2.4.1. Acquisition Mode

Acquisition Mode refers to the state in which the interferometer lengths are brought into resonance from their initial uncontrolled values. The PSL and IOO subsystems are assumed to be fully operational in this mode. The primary function of the LSC in this mode is to lock the interferometer. After lock a settling time is required. Wire and mirror resonances are permitted to settle down (or are actively damped), filters are allowed to equilibrate, control ranges are adjusted, and self tests are completed to verify that residual excitations do not exceed Detection Mode limits.

2.4.2. Detection Mode

In this mode the interferometer lengths are maintained at a level of stability which allows detection of strain signals within the LIGO sensitivity specifications. The functions in this mode are:

- sense and control the four interferometer lengths and the input laser frequency
- provide a measure of the residual deviations of the four lengths and the laser frequency
- provide a calibrated readout of the interferometer strain

2.4.3. Diagnostics & Calibration Mode

This is a mode (in fact a set of modes) that may be accessed from the preceding modes. The functions of this mode are:

- provide diagnostic capability to determine the performance of the LSC
- enable implementation of calibration procedures within the LSC
- support diagnosis and calibration of other subsystems

2.5. General Constraints

The most severe constraint that the LSC CDS must accommodate is the fact that the control servos span a physical distance of four kilometers between the LSC sensors and the end test masses (ETMs). It is not practical and may not even be possible to send control signals via copper wire over such a distance while maintaining the low noise, wide dynamic range and frequency response required for the LSC servos. This necessitates the use of optic fibers for these signals and this in turn makes the use of digital controllers highly desirable if not absolutely necessary.

3 RF MODULATION AND DEMODULATION

For current status of the RF modulation and demodulation design see the LSC PDR (T970122-00).

4 RF PHOTODIODES

It is currently envisioned that design of the RF photodiode circuit recently developed for the 40 meter prototype will be modified and used for the LIGO LSC subsystem. During the preliminary design phase it will be modified to meet the LSC requirements and tested on the LSC prototype setup TBD. These requirements are outlined in the LSC DRD.

5 SERVO ELECTRONICS

The decision to control the end test masses constrains us to the use of digital controllers as was mentioned in section 2.3. This has the benefit that changes can be made to the controllers via software providing some versatility. It also provides a natural input and output diagnostic port for each of the servos. The drawback to this is that there are additional noise sources arising from the digitization process. These must be well understood and handled carefully in order to meet the LIGO requirements with a robust system design. In this section we will discuss the nature of the most troublesome noise sources and how they impact the requirements of the LSC. We will show an example of the modeling efforts that are being used to study and characterize this noise. We will show the various LSC servo configurations and then describe the major components of an LSC digital servo and the current state of design and testing.

5.1. Configuration and Layout

Figures 3 through 6 show the system layouts for the four length degrees of freedom and are derived from the sensing and control diagram in figure 2. All whitening filters, ADCs and signal processing to implement the servo transfer functions are performed at the corner station where the sensor signals originate. Signals that terminate in the corner station are converted back to analog, then filtered and sent to their destination as shown in the figures. Signals that terminate at the mid-stations (for the 2 Km) or end stations (for the 4 Km) are sent via optical fibers to those destinations and then converted, filtered and interfaced to the suspension system drivers.

5.1.1. Differential Mode Servos (*L*- and *l*-)

Figure 3 shows the differential mode servos in detection mode operation. The *L*- servo uses the Q output of the dark port demodulator and sends opposite polarity signals down each arm to the end test masses to control the arm cavity differential error. The *l*- servo which controls the Michelson differential error uses the Q output of the recycling port demodulator to send opposite polarity

signals down each arm to control both input and end test masses at frequencies below about two Hertz. At higher frequencies a signal is sent to the beam splitter.

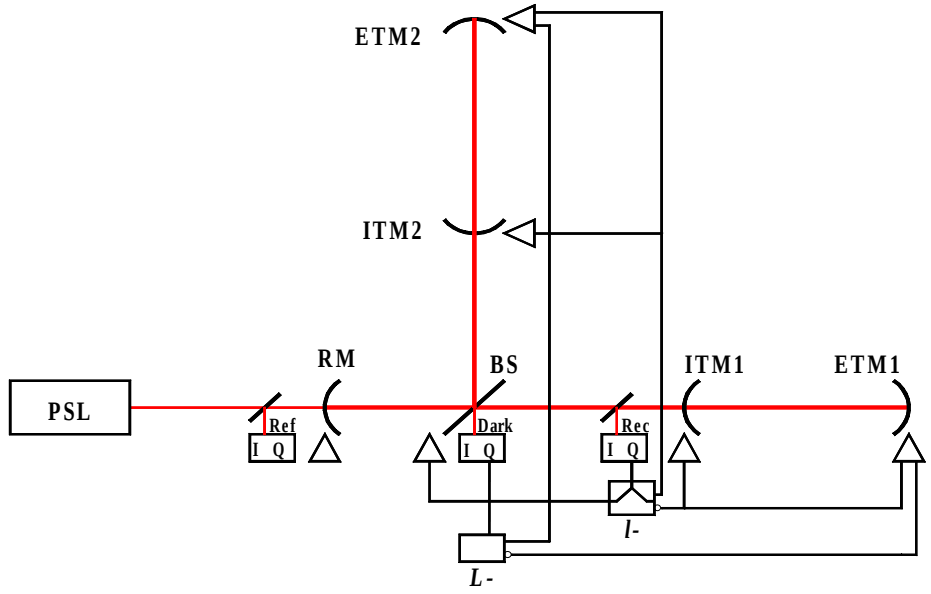


Figure 3: *L1-L2* and *l1-l2* servos in Detection Mode

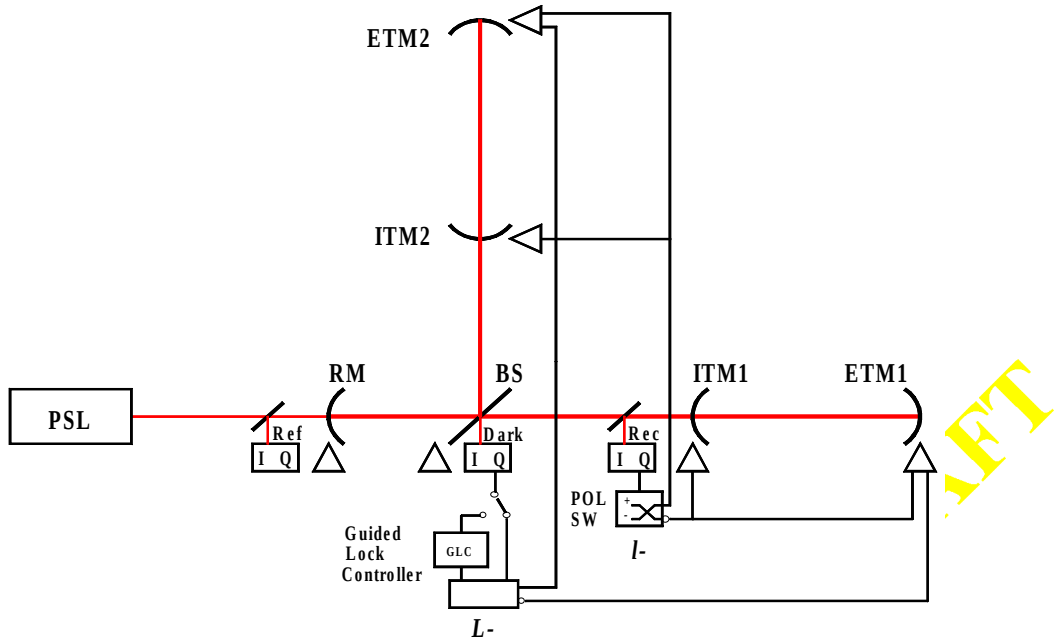


Figure 4: *L1-L2* and *l1-l2* servos in Acquisition Mode

Figure 4 shows the differential mode servos in acquisition mode operation. In this mode a guided lock controller has been added to the *L*- servo to increase the speed of acquisition as described in the LSC PDR. During the acquisition process the stable feedback sign of the *l*- loop changes sign as the interferometer transitions from the unlocked state to the state where all the cavity lengths are controlled. This necessitates a polarity switch of the signal sent to the test masses. Since the differential signals to each arm are opposite in polarity this amounts to switching the signals to the arms during the acquisition process. This does not occur in detection mode.

5.1.2. Common Mode Loops (*L*+ and *l*+)

Figure 5 shows the two common mode servos in detection mode operation. The *L*+ servo uses the in-phase output of the reference cavity demodulator to send a low frequency control signal (<2Hz) to each of the four test masses. It also sends both a high frequency and a low frequency control signal back to the IOO for frequency stabilization. Separate inputs (not shown) are retained so that the LSC has controller over the cross-over between them. The *l*+ servo uses the in-phase output of the recycling mirror cavity to send a low frequency control signal to the four test masses and a higher frequency signal back to the recycling mirror. The crossover frequency is about 2 Hz.

Figure 6 shows the same two servos in detection mode. The *L*+ servo has a polarity switch of the signals going to the test masses for the same reason as the *l*- servo in figure 4. The *l*+ servo is the same as detection mode except that the high frequency signal is fed back to the laser for frequency stabilization.

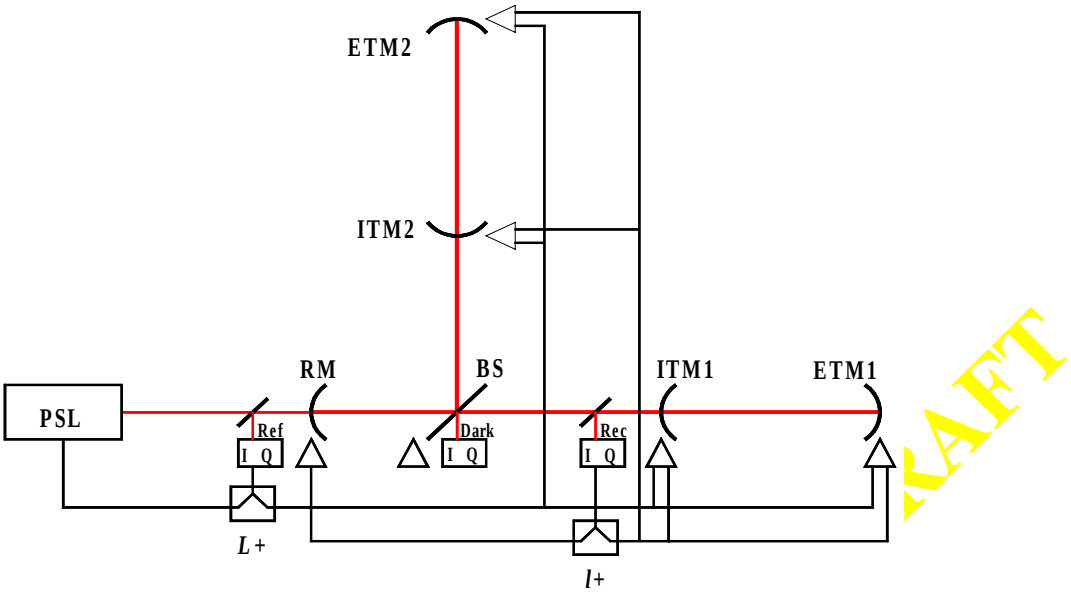


Figure 5: *L1+L2* and *l1+l2* servos in Detection Mode

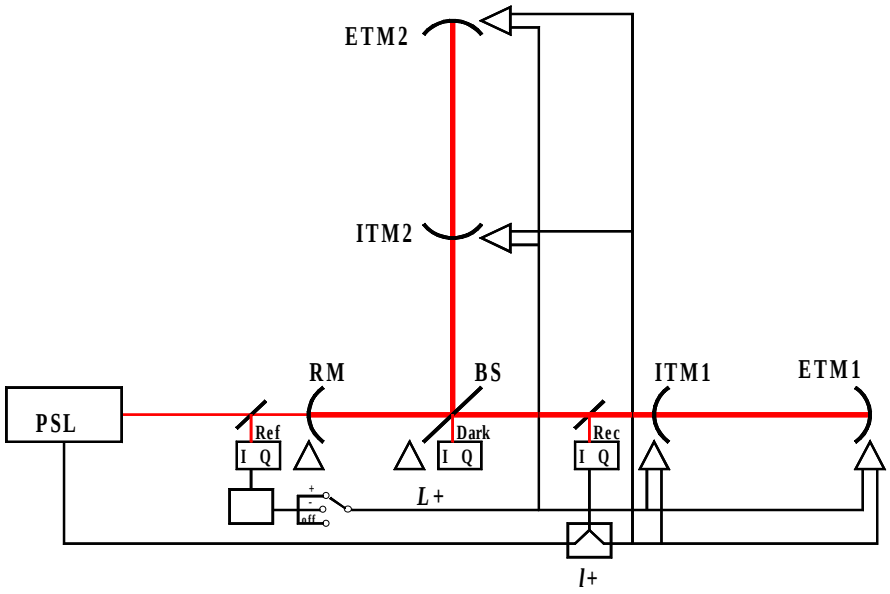


Figure 6: *L1+L2* and *l1+l2* servos in Acquisition Mode

5.2. Digital Controllers

Here we present a detailed discussion of each of the components of a digital controller with respect to the LSC servo loops.

5.2.1. Block Diagram

This simplified diagram of the *L*- servo loop is typical of the four digital servo loops that include the end test masses. Not shown here are the sensor switching circuits and frequency crossover circuits of the other loops. The digital controller is that portion of the servo that has a dimensionless gain of volts per volt and includes the analog conditioning filters at the input and output of the controller. As was mentioned earlier, all signals that terminate in the corner station will have the entire controller contained within the same electronics rack with copper wire connections to the suspension controller. Signals that terminate at the mid or end stations will have the DAC and unwhitening filter near the suspension controller with an optic fiber link between the CPU and DAC. This link may be in the form of a reflective memory (TBD) not shown in this diagram.

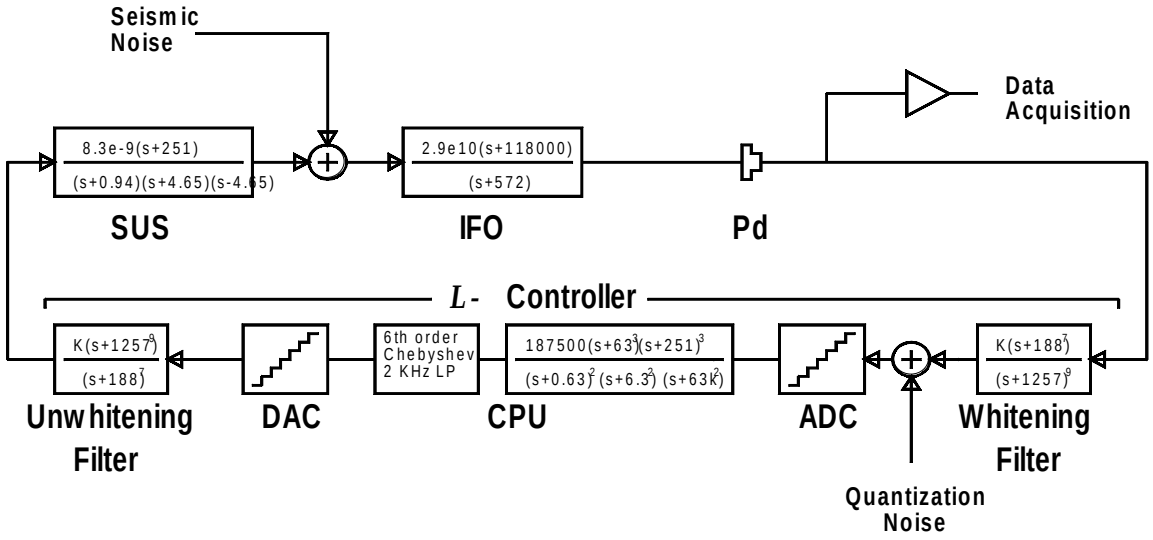


Figure 7: Block diagram of the *L1-L2* servo loop.

5.2.2. Whitening / Anti-aliasing Filter

This filter performs all of the input signal conditioning to the ADC. The whitening filter is necessary to match the dynamic range of the input signal to the input range of the ADC. This must include some safety factor to ensure sufficient headroom to minimize the occasional large noise signal saturating the ADC input. This filter must necessarily include some anti-alias filtering to prevent noise above the Nyquist frequency from reaching the input to the ADC where it will be aliased to a lower frequency. Once a signal is aliased into the signal band of interest it can not be discerned from true in band signals and therefore can not be filtered out. The filter circuit itself requires some bandwidth limiting to take out any noise pick up on the input lines that could saturate some stages of the electronics. It is interesting to note that if these servos were physically small the bandwidth of the servo itself would act like a low pass anti-alias filter. Because the distances between components in the LSC are quite large an anti-alias filter is required to filter out wide band noise induced in the system that has not been suppressed before it gets to the ADC. The whitening and anti-alias filters will be combined into one analog signal conditioning filter. The specifications for this filter are TDB. A first cut design of the filter will be discussed in the modeling section.

5.2.3. Analog-to-Digital Converter

The number of binary bits required for the ADC is determined by the dynamic range (plus headroom) of the signal spectrum at the input to the ADC. As was mentioned above, this can be enhanced by judicious design of the whitening filter. There are a number of commercial vendors that produce 16 bit ADCs in VME format with sampling rates up to 200Ks/s. Our current investigations center around these devices. There are two popular schemes used in these ADCs, Sigma-Delta converters and Successive Approximation. We have restricted our studies to the latter because of the inherent delay through the sigma delta digital filter which can be quite long if high

precision is required. The Successive Approximation ADC uses an internal sample/hold and then performs a binary search to find a reference voltage to match the sampled signal. Therefore it takes 16 clock pulses to digitize one sample. These clock cycles should not be confused with the sample clock which performs the sample/hold operation. A 200 Ks/s ADC is actually sampling at 200Ks/s but the internal clock must run 16 times faster.

5.2.4. Digital Signal Processor

To meet the LSC requirements we do not need a Digital Signal Processor as such. These are specialized processors optimized to perform multiplies and adds in a single clock cycle. They are still somewhat expensive and come with a steep learning curve. We are currently looking at the Baja 4700 CPU from Heurikon which will run at about 80 Mflops and should be sufficient for our needs.

5.2.5. Digital-to-Analog Converter

The search for a Digital to Analog converter is the same as for the ADC. In all likelihood we will find a suitable pair from the same vendor. This makes implementation and programming easier.

5.2.6. Unwhitening / Anti-Imaging Filter

The unwhitening filter at the output of the DAC essentially undoes everything that the whitening filter did at the input. The dynamic range of the signal must be expanded back to the levels sufficient to drive the summing node to zero error. As will be discussed in the modeling section, this puts very tight constraints on these filters. They must be matched very closely in order to not compromise the phase margin of the loop. A low pass smoothing filter, sometimes called an anti-imaging filter is required to reduce the digital noise from the DAC. The spectrum of the unwhitening filter may already provide this function.

5.3. Digital Noise Sources

The number of binary bits, sampling frequency, clock stability and circuit components must be chosen carefully to ensure that signal to noise ratio of the gravity wave channel is not significantly reduced by the digitization process. Some noise sources are easy to deal with or are taken care of naturally with proper choice of floating point microprocessor with sufficient number of bits so that roundoff errors and accumulator widths do not cause significant errors. Below are listed the most bothersome of the noise sources in relation to our requirements for the LSC.

5.3.1. Quantization Noise

In an ideal n-bit ADC there are errors associated with the quantization process. The maximum error for a DC input signal is ± 1/2 LSB. For AC signals the ADC will produce quantization noise whose rms value (measured over the Nyquist bandwidth, 0Hz to $f_s/2$) is approximately equal to $q/\sqrt{12}$ where q is one Least Significant Bit (LSB) equal to $(VFS)/2^n$. This assume that the sig-

nal is at least a few LSBs in amplitude so that the ADC output always changes state. If this condition is not met then the rms noise is simply one LSB. In such a case the input signal can be dithered with out-of-band white noise which is then filtered with a low pass filter at the output of the DAC. This white noise must be less than the Nyquist frequency to prevent aliasing. This white noise dithering may be produced artificially or from the input noise spectrum by judicious design of the whitening filter at the input to the ADC. The use of a whitening filter serves two purposes. The first is to selectively amplify low amplitude frequencies in order to "Whiten" the input spectrum and thus allow a better match to the dynamic range of the ADC. Ideally this would raise all of the frequencies of interest above the level of the sensitivity of the ADC so that the feedback network can perform its function and suppress this noise at the summing junction of the servo. If there are midband frequencies that are still below one LSB the servo can still function provided there is sufficient energy in the high frequency part of the spectrum to dither the lower frequency signal. In other words the high frequency signals ensure that the ADC is always changing states. The second function of the whitening filter is to suppress the quantization noise of the ADC. This can easily be seen by examining the gain of the quantization noise at the photodiode referred to the ADC input.

$$n_{qpd} = \frac{n_q \cdot Cont \cdot SUS \cdot IFO}{1 + wf \cdot Cont \cdot SUS \cdot IFO} \cong \frac{n_q}{wf}$$

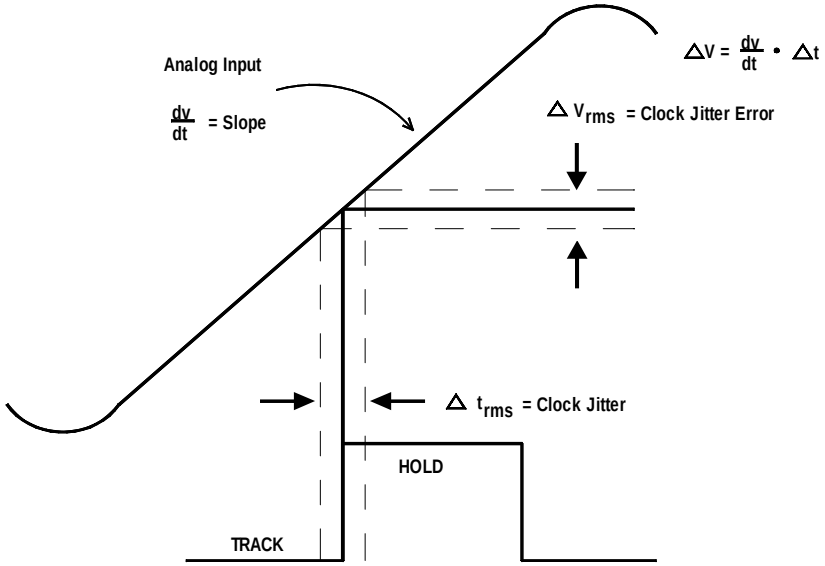
Where *Cont* is the LSC controller, *SUS* is the suspension controller, *IFO* is the interferometer and *wf* is the whitening filter. One way to characterize the quantization noise is by calculating the signal-to-noise ratio of an ideal n-bit ADC. This should be closely matched to the dynamic range requirements of the LSC servos. The signal to noise ratio of a full scale sinewave due to quantization error can be shown to be

$$SNR_q = 6.02n + 1.76 + 10\log\left(\frac{f_s}{2f_a}\right)[dB]$$

where n is the number of binary bits, f_s is the sampling frequency and f_a is the analog bandwidth. This equation shows that the dynamic range can be increased by oversampling of the input signal beyond the Nyquist criteria of twice the analog bandwidth. Currently there are commercially available 16 bit ADCs with sampling rates of 200 Ks/s. The *L*- loop has the highest bandwidth to the end test masses at about 140 Hz. This would give a theoretical signal to noise ratio of 126 dB, more than sufficient for the dynamic range requirements for the *L*- loop. The dynamic range for the entire servo loop is quite large but the range required for the ADC depends on how well one designs the whitening filter. The other three servo loop that include the end test masses have much lower bandwidths and lower dynamic range requirements are therefore of lesser concern. We assume that in reality we can not achieve anything near 126dB by oversampling. Fortunately, we probably don't need it. But one of the measurements that we are using to compare ADCs is to measure the signal to noise ratio as a function of sampling frequency and find the real limit.

5.3.2. Clock / Aperture Jitter

The previous discussion about quantization noise assumes that the input signal is sampled with zero time deviation of the sample clock (an ideal clock). Any time deviation (jitter) in sample clock translates directly into a voltage error (see figure below).



It should be noted that even with a perfect clock there are internal noise sources within the ADC chip sometimes specified as aperture jitter that produce the same effect. Both the clock jitter and the ADC aperture jitter will add to the overall error. The signal to noise ratio associated with this jitter can be expressed as

$$SNR_j = 20\log\left(\frac{1}{2\pi f_a t_j}\right)[dB]$$

where f_a is the analog bandwidth of the input signal and t_j is the time jitter of the sample clock in seconds. Figure 9 is a plot of signal to noise ratio for both clock jitter and quantization error verses sampling frequency for an analog input bandwidth of 140 Hz (unity gain bandwidth of the *L*-loop). Several clock jitters are plotted. From this plot we could infer that our signal to noise ratio could easily be limited by the clock jitter rather than by quantization noise but this is not the whole story. This is a useful measure to compare ADCs in a bench test and understand the various digital noise sources. But the clock jitter must be multiplied by the input spectrum to correctly show the impact on the LSC servos. This is discussed in more detail in the modeling section.

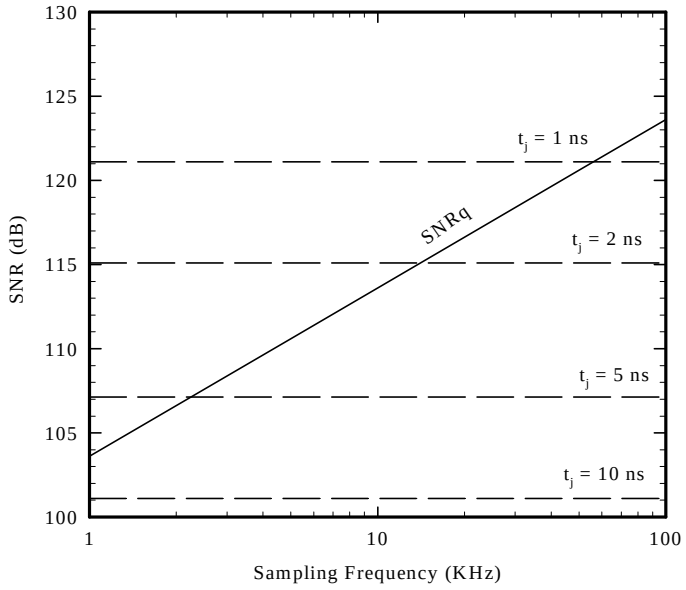


Figure 9: Signal-to-Noise ratio from quantization noise (SNR_q) and clock jitter (t_j) as a function of frequency at a bandwidth of 140 Hz.

One issue that must be resolved is what to use for the ADC/DAC sample clock. Currently the GPS clock that is to be used for the other LIGO systems has a clock jitter between 100 and 200 nsec (off the chart so to speak). We are exploring the possibility of getting a modified version of this clock with better specifications (chances seem to be slim). We are also in the process of measuring the "real" quantization error and aperture jitter error of commercially available ADCs to determine the useful limits of this technique to increase SNR. The GPS clock would be a convenient solution for the LSC because the ADCs and DACs are 4Km apart. An alternative would be to send a precision clock from the corner station to the mid and end stations via light fibers. We don't currently know what the expected clock jitter would be for that scheme.

5.3.3. Phase Delay / Jitter

The *L*- loop has a unity gain frequency of 140 Hz with about 36° of phase margin. At 140 Hz every 20 µsec of delay reduces the phase margin by 1°. The transit time down each arm of the interferometer is 13.4µsec. If we use reflective memory as the other subsystems do we can add another 7µsec for memory update time. We must also add processor time, read/write times, and any phase delays from filters in the loop. We will need to measure the maximum phase jitter in the signal path in order to set up the DAC clock with some safety margin. The total delay plus jitter

will probably be a few degrees of phase delay but care must be exercised to minimize this effect on the phase margin. This phase delay puts very stringent requirements on the whitening and unwhitening filters. The more poles and zeros we have in the filters, the more difficult it is to match them over time and temperature. We will probably need to make a trade-off between filter efficiency and phase margin. The other three LSC servo loops have very low bandwidth down the arms as well as larger phase margins to begin with. So their requirements will be met if the *L*-loop requirement is met.

5.3.4. DSP Noise Sources

We do not anticipate any problems here due to truncation or roundoff errors but we should watch for spurious effects during testing of the prototype system.

5.4. Controller Modeling

The following is a description of the modeling that has been done to define the parameters of the digital controllers. This effort was started some time ago with input from L. Seivers for the loop gains and others for the transfer functions of the suspension controller and interferometer. At the time this effort began there was no other input available to try to characterize the LSC digital controllers. Recently these modeling efforts have begun to merge with those by G. Gonzalez but are not included here due to there preliminary state. The current plan is that Gabriela will provide an input spectrum, an output spectrum and the transfer function for each of the servo loops. This input will be used to develop a model of the digital controllers, filters, etc. When a reasonable, "buildable" model (including saturation effects) has been made it will be inserted back into Gabriela's global model to verify that it meets requirements. Table 1 shows the current state of the LSC controller transfer functions supplied by G. Gonzalez. In order to explain the modeling process and goals we will use the previous version of the *L*- servo model as an example. Therefore the details of the transfer functions are slightly different but the following graphs demonstrate the methods being used to design the controllers and describe the main issues.

Figure 11 shows the loop gain for the *L*- servo that is used as input to the model. Figure 12 is a magnitude-phase plot which shows the conditional stability of the servo. The gain at 180 degrees of phase shift is constrained to about ± 12 dB and the phase margin at unity gain is about 36 degrees. This will make matching the whitening and unwhitening filters very critical. Figure 13 is the transfer function for the controller (solid line) which is derived by dividing the loop gain by the suspension transfer function and the interferometer transfer function. Also shown on this plot is an example of a whitening filter (dashed line) to match the dynamic range of the signal with the input to the ADC. The dotted line represents the unwhitening filter and is just the inverse of the whitening filter.

Table 1:

Controller	***Transfer Function***	***Filter 1***	***Filter 2***
L1 - L2 (V/V)	K=187500 poles @ 2x0.1Hz, 2x1Hz, 2x10KHz zeros @ 3x10Hz, 3x40Hz	6th order Cheb 3 dB ripple 2 KHz low pass	
l1 - l2 (V/V)	K=-260000 pole @ 100KHz zero @ 0.5Hz	2nd order Butter 15 Hz low pass	6th order Cheb 3 dB ripple 2 KHz low pass
L1 + L2 (V/V)	K=-8000 pole @ 20Hz zero @ 5Hz	3rd order Elliptic 3dB ripple 30 Hz low pass 30 dB stopband	
Laser Controller *(Hz /V)*	K=355.3058 poles @ 4Hz, 200Hz, 2x300Hz zeros @ 0Hz, 8KHz, 10KHz	3rd order Elliptic 3dB ripple 4 Hz high pass 20 dB stopband	
l1 + l2 (V/V)	K=600 poles @ 2x31.42Hz, 1885Hz zeros @ 2x4.65Hz, 251.3Hz	4th order Butter 500 Hz low pass	

Figure 14 is a plot of the ADC quantization noise at the photodiode (solid line) and the ***L-*** electronic noise requirement at the photodiode. The quantization noise is calculated as follows:

$$N_q = \frac{V_{fullscale}}{2^n \sqrt{3 f_s}}$$

Where $V_{fullscale}$ is the input range of the ADC (10V), *n* is the number of ADC bits (16) and f_s is the sampling frequency (100KHz).

$$\text{Lminus}(s) := \frac{K\cdot(s+40\cdot\tau)^2\cdot(s+50\cdot\tau)\cdot(s+10\cdot\tau)\cdot(s+18800\cdot\tau)}{(s+0.1\cdot\tau)^2\cdot(s+500\cdot\tau)\cdot(s+1000\cdot\tau)^2\cdot(s+91\cdot\tau)\cdot(s+j\cdot0.74\cdot\tau)\cdot(s-j\cdot0.74\cdot\tau)}$$

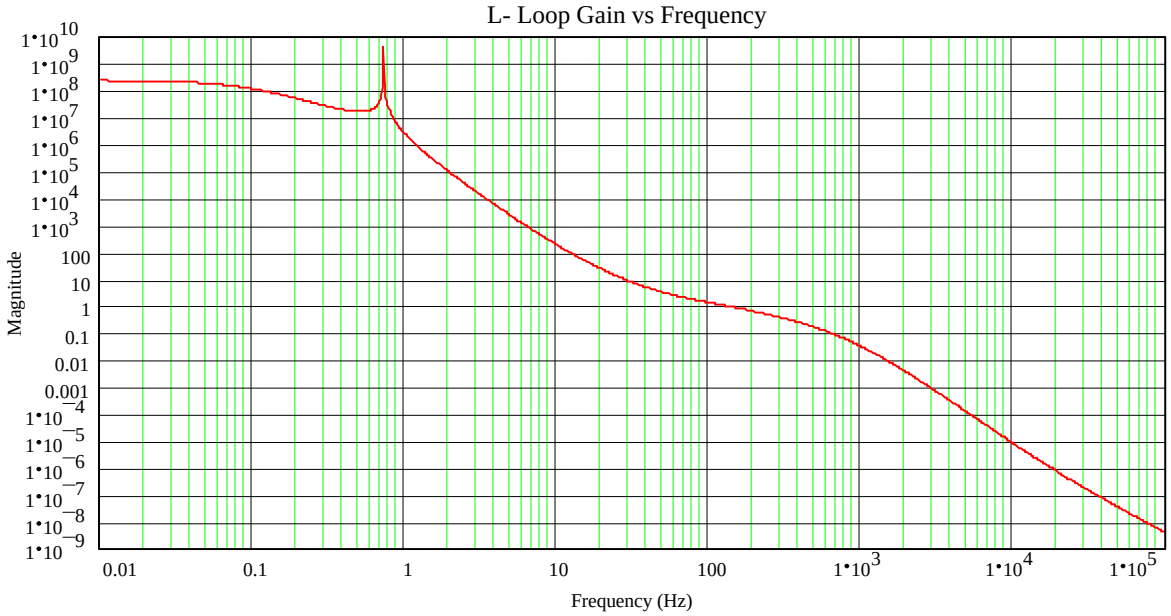


Figure 11: *L*- Loop Gain

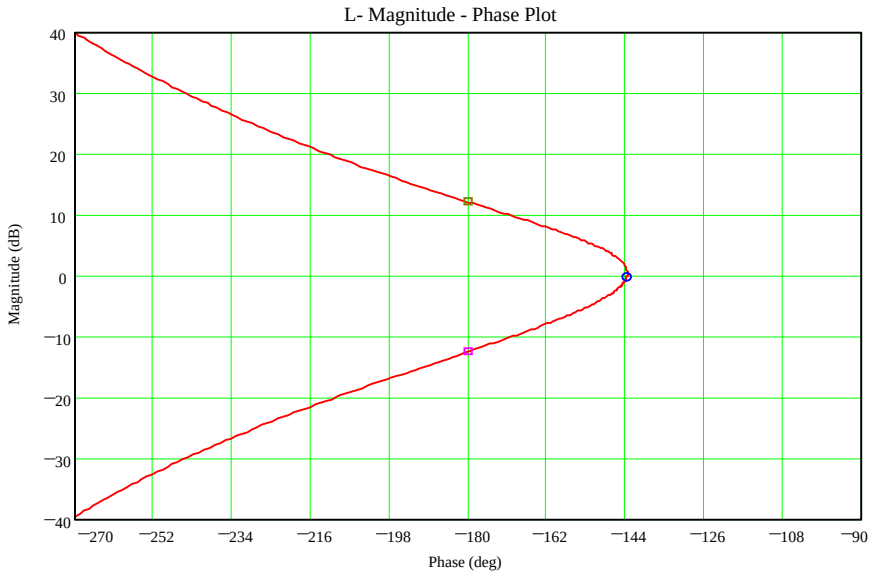


Figure 12: *L*- Magnitude - Phase plot. This shows a conditionally stable loop gain with a gain margin of ± 12 dB and a phase margin of 36°.

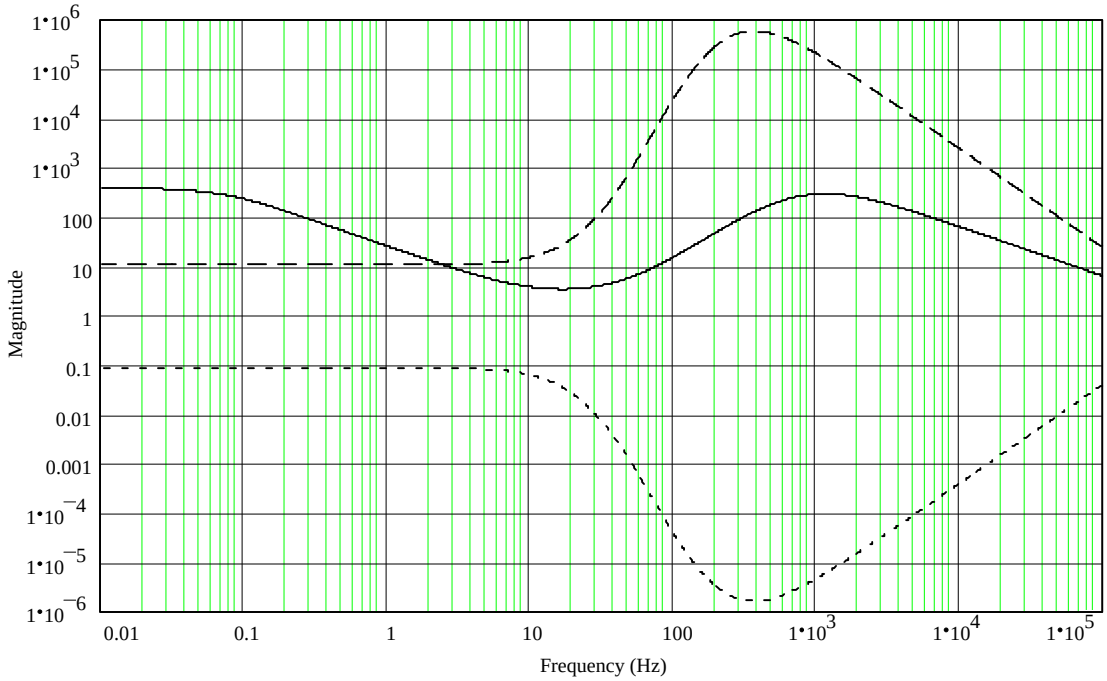


Figure 13: *L*- controller transfer function (solid line), example whitening filter (dashed line), example unwhitening filter (dotted line). The whitening filter has 7 zeros at 30 Hz and 9 poles at 200 Hz.

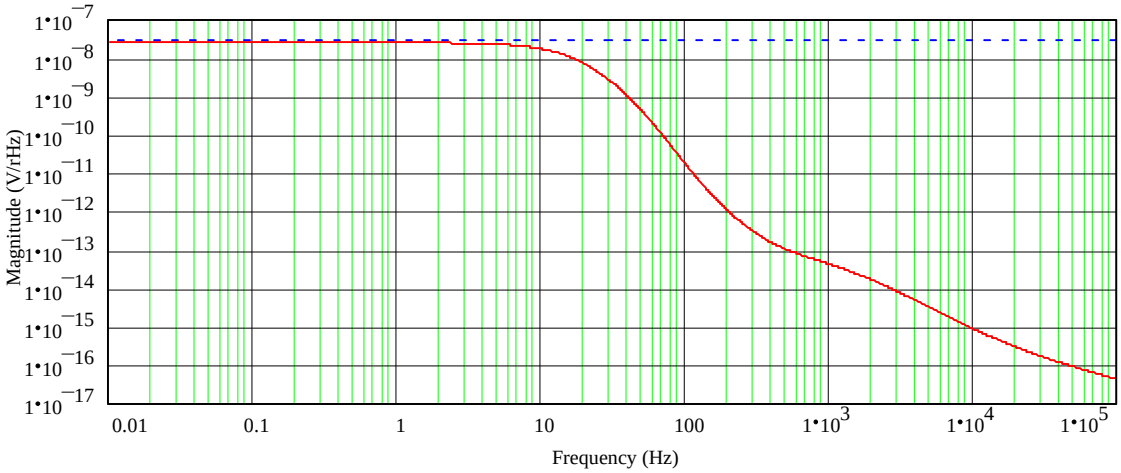


Figure 14: ADC quantization noise (solid line) at the photodiode. *L*- electronic noise requirement at the photodiode.

Figure 15 is an approximate analytical model of the seismic noise plus shot noise referred to the test mass in m/rtHz. This noise is input into the closed loop equation at the test mass to find the noise spectrum at the input to the ADC (Figure 16 solid line) with the above whitening filter in place. The dotted line in figure 16 represents the ADC input without a whitening filter. The dashed line is the digitization noise due to a 1 µsec clock jitter. The dash-dot line ADC quantization noise from figure 14.

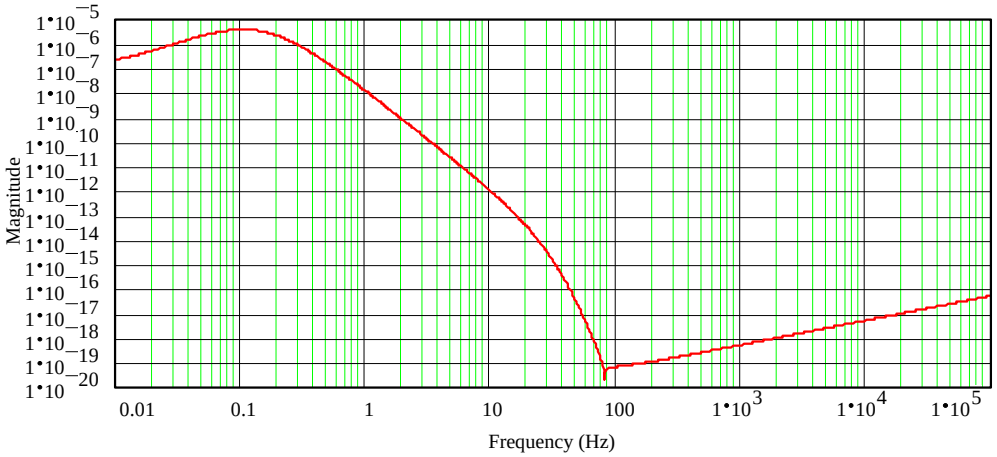


Figure 15: Approximate model of the seismic noise plus shot noise used as input to the closed loop servo model. Magnitude is in m/rtHz.

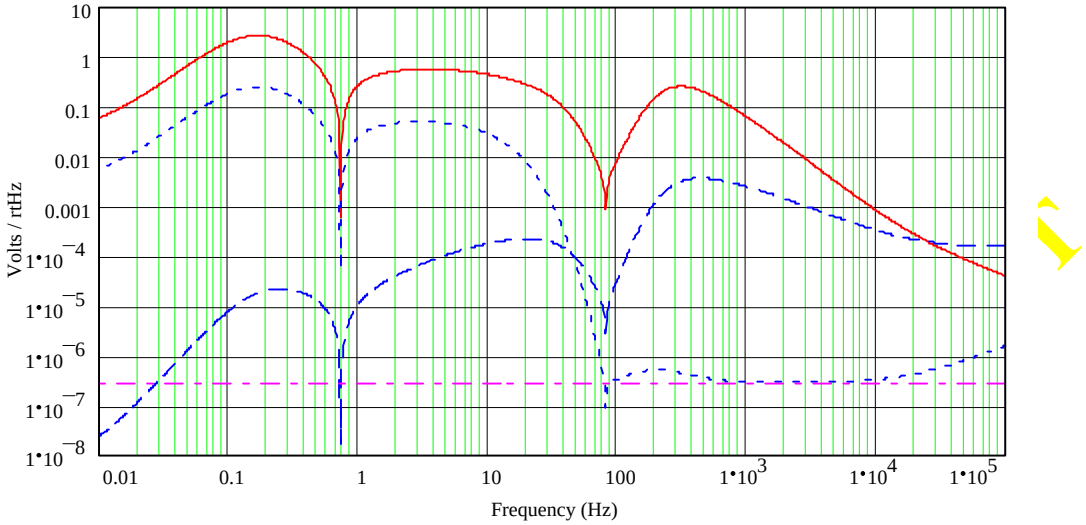


Figure 16: Seismic and shot noise at the input to the ADC after whitening filter (solid line), with no whitening filter (dotted line), digitization noise due to 1µsec clock jitter (dashed line), and quantization noise from figure 14 (dash-dot line).

The digitization noise due to clock jitter can be obtained from

$$N_j = S(f) \cdot \frac{\pi f t_j}{\sqrt{2}}$$

where $S(f)$ is the input spectrum, f is the frequency component and t_j is the time jitter of the clock. For this example the DC gain of the whitening filter was set to reduce the quantization noise at the photodiode to a level below the electronic noise requirement. Note that the DC gain will then determine amplitude of the noise spectrum at the input to the ADC. A somewhat vague criteria was set for the clock jitter to put the noise "comfortably" below the seismic/shot noise curve at all frequencies out to the first test mass resonance (6.79 KHz). This is easily met with the one micro-second clock jitter shown. However, the whitening filter has 7 zeros and 9 poles. This will be very difficult to match with an unwhitening filter of 9 zeros and 7 poles. A brief modeling effort using MATLAB showed that with this many poles and zeros a mismatch of 1% between components could cause phase shifts of several degrees. Therefore we may not be able to whiten the input so much which means that the clock jitter specification would more restrictive. The clock jitter of the GPS modules that we will use for other systems is expected to have a clock jitter of 100 ns to 200 ns. It is not clear at this point whether this will meet our requirements. In this example the quantization noise is not a limiting factor.

Obviously measuring these effects on real hardware needs to be completed to set some boundary conditions. As modeling efforts progress we will have a better understanding of the trade-offs involved.

5.5. Diagnostics and Calibration

For a detailed description of the diagnostics and calibration of the LSC see the LSC PDR (T970122-00).

5.6. Plans for testing Hardware

A series of tests have been initiated to begin testing various pieces of hardware for the LSC controllers. The testing methodology has been divided into open loop bench tests and later, when we have selected suitable modules and devices, closed loop tests using a real or simulated suspended optic TBD. For further discussion of the hardware test plans refer to the LSC PDR.

5.6.1. Open Loop Tests

5.6.1.1 CPU Tests

We are currently in the process of testing CPUs from different manufacturers. in our testing we are considering:

- CPU speed
- Data input and output rates
- Ease of programmability

- integration with other system components

5.6.1.2 ADC / DAC Tests

We are testing ADCs and DACs from a number of commercial vendors in order to measure performance characteristics such as:

- Dynamic range limits
- Overall noise parameters
- Input/output data rates and latencies
- Ease of programmability
- Compatibility with various CPUs and reflective memories

5.6.1.3 Quantization Noise

For each ADC and DAC we will measure the quantization noise as a function of sampling frequency. This will not only provide a selection criteria for the modules but will help determine the requirements for the sampling clock.

5.6.1.4 Clock Jitter Noise

For each ADC and DAC we will also measure the quantization noise as a function of sample clock jitter. There will be a constant aperture jitter from the circuit under test that will be mixed with the clock jitter measurement. It is not known at this point whether the quantization noise floor will be from sample clock frequency or clock jitter. This may vary from one manufacturer's model to the next. This will provide a specification on the sample clock generator as well as selection criteria for the ADCs and DACs.

5.6.2. Closed Loop Tests

Refer to the LSC PDR.

6 RELATED SUBSYSTEMS AND INTERFACES

6.1. Suspension System

The design of this interface is TBD.

6.2. Input Optics and Prestabilized Laser

The design of this interface is TBD.

6.3. Alignment Sensing and Control

The design of this interface is TBD.

6.4. Data Acquisition

The design of this interface is TBD.

6.4.1. ADC Channels

6.5. Interferometer Diagnostics

The design of this interface is TBD.

7 SAFETY

This item shall meet all applicable NSF and other Federal safety regulations, plus those applicable State, Local and LIGO safety requirements. A hazard/risk analysis shall be conducted in accordance with guidelines set forth in the LIGO Project System Safety Management Plan LIGO-M950046-F, section 3.3.2.

APPENDIX 1 ACRONYMS

- ADC - Analog to Digital Converter
- CDS - Control and Data System
- DAC - Digital to Analog Converter
- IFO - LIGO Interferometer
- IOO - Input / Output Optics
- LIGO - Laser Interferometer Gravitational Wave Observatory
- LSC - Length Sensing and Control
- PSL - Prestabilized Laser
- QMPU - Quadrant Monitor Processing Unit
- SEI - Seismic Isolation
- SRD - LIGO Science Requirements Document
- SUS - Suspension Control
- TBD - To Be Determined
- WPU - Wavefront Processing Unit