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- LIGO -
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ASC CDS Conceptual Design	
Jay Heefner	

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California Institute of Technology
LIGO Project - MS 51-33
Pasadena CA 91125
Phone (818) 395-2129
Fax (818) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project - MS 20B-145
Cambridge, MA 01239
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

WWW: http://www.ligo.caltech.edu/

1   INTRODUCTION

1.1. Document Organization

This document describes the ASC CDS conceptual design and was produced as a result of the ASC CDS DRD (LIGO T970061). The conceptual design presented shows how the ASC CDS system for one interferometer at the Washington site could be organized. The design for the second interferometer and the Louisiana site would be similar. The complete designs for the Washington and Louisiana sites will be developed during the preliminary design.

The document is organized as follows:

- Section 2: Wavefront Processing Unit Design provides a description of the systems that would used to provide to implement the wavefront processing subsystem.
- Section 3: Quadrant Monitor Processing Unit Design provides a description of the systems that would be used to implement the quadrant monitor photodiode subsystem.
- Section 4: Optical Lever Design provides a description of the systems that would be used to implement the optical lever subsystem.
- Section 5: Camera System Design provides a description of the systems that would be used to implement the video camera subsystem.
- Section 6: ASC CDS System Level Design provides a description of the systems that would be used to provide higher level processing and functionality. Typically information from each of the ASC CDS subsystems (wavefront sensors, quadrant monitor photodiodes, optical levers and cameras) is collected and processed at this level.
- Section 7: ASC CDS Prototype Setup provides a brief description of the prototype test setup that will be used to verify the ASC and ASC CDS designs. This prototype test setup is more fully described in D. Sigg's document (LIGO T970TBD).

1.2. System Overview

A block diagram showing the ASC CDS system in relation to the ASC system and other LIGO systems is shown in the figure below.

Figure 1: ASC CDS Product Perspective
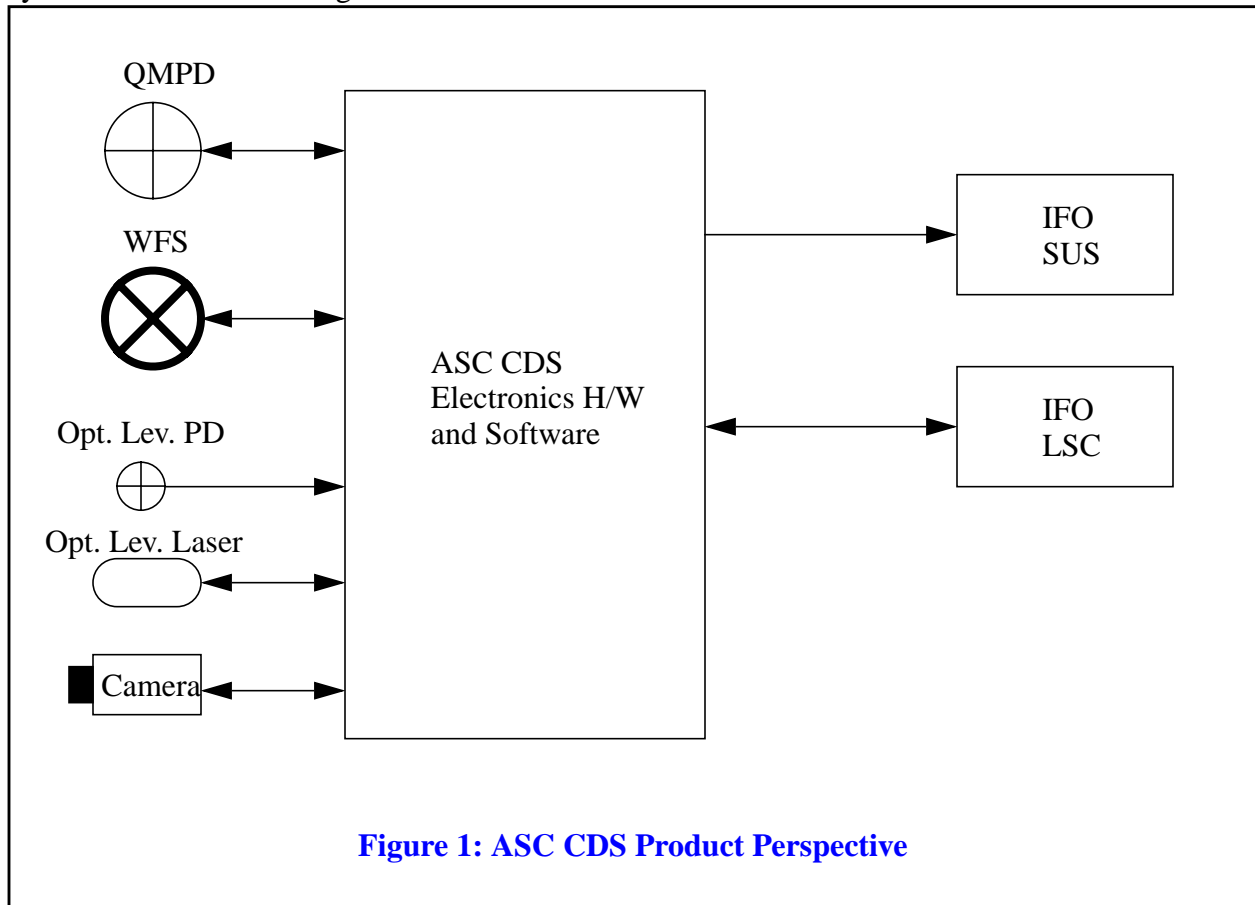
The figure below shows the functional layout of the ASC CDS system with respect to the LIGO optical layout.
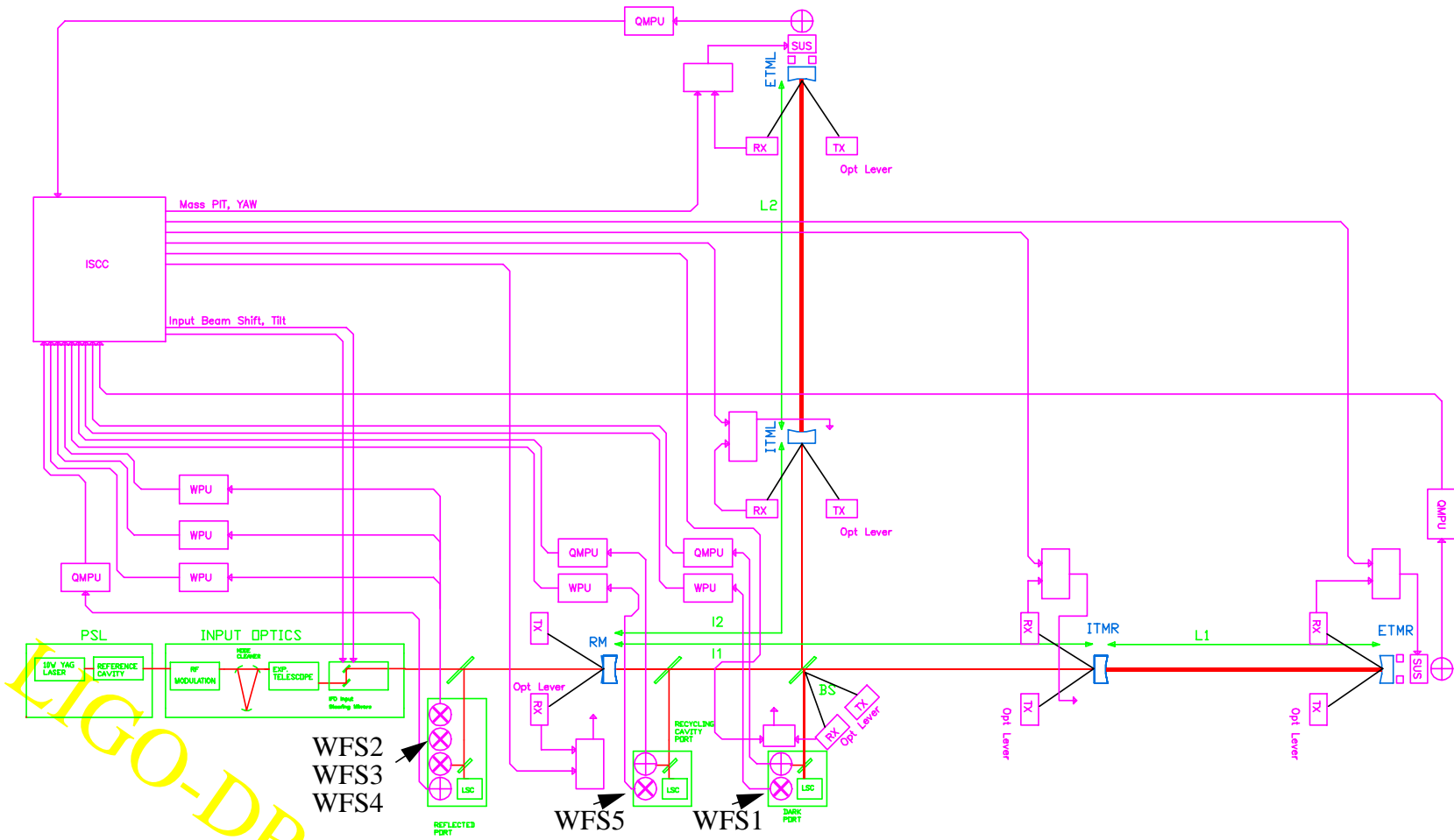
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Figure 2: ASC CDS Functional Layout

1.3.   Acronyms

- ADC- Analog to Digital Converter
- ASC- Alignment Sensing and Control
- BSC- Beam Splitter Chamber
- CDS- Control and Data System
- CPU- Central Processing Unit
- DAQ- LIGO CDS Data Acquisition
- EPICS- Experimental Physics Industrial Control System
- ETM- End Test Mass
- F/O- Fiber Optic
- HAM- Horizontal Access Module
- IFO- Interferometer
- IOO- Input/Output Optics
- ITM- Input Test Mass
- LA- Louisiana Site
- LIGO- Laser Interferometer Gravitational-wave Observatory
- LPF- Low Pass Filter
- LSC- Length Sensing and Control
- LVEA- Laser Vacuum and Equipment Area
- MUX- Multiplexer
- QMPD- Quadrant Monitor Photodiode
- QMPU- Quadrant Monitor Processing Unit
- SUS- Suspension System
- TBD- To Be Determined
- VEA- Vacuum Equipment Area
- WA- Washington Site
- WFS- Wavefront Sensor
- WPU- Wavefront Processing Unit

2   WAVEFRONT PROCESSING UNIT DESIGN

Wavefront sensor photodiodes are located on common ASC/LSC optical tables in the LVEA. The rough placement of the optical tables is depicted in Figure 2: ASC CDS Functional Layout. The table below lists the location of each sensor.

Table 1: WFS Number vs. Location

WFS Number	Location
1	ASC/LSC Dark Port Optical Table
2	ASC/LSC Reflected Port Optical Table
3	ASC/LSC Reflected Port Optical Table
4	ASC/LSC Reflected Port Optical Table
5	ASC/LSC Recycling Cavity Pick-Off Optical Table

The figure below is a block diagram of one wavefront processing unit.

Figure 3: Wavefront Processing Unit Block Diagram
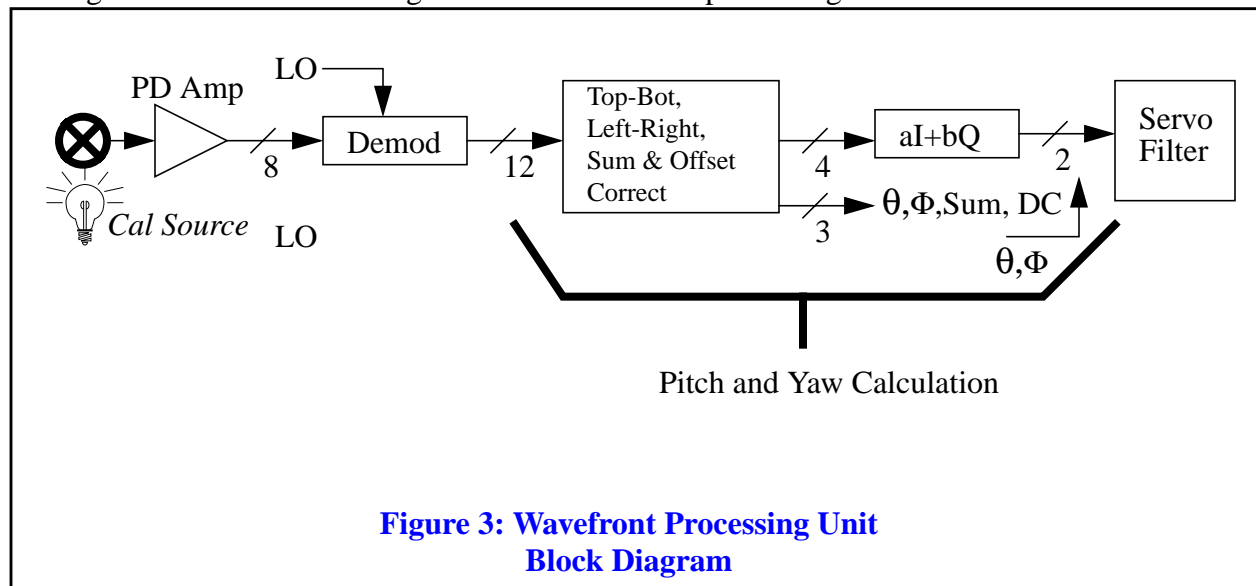
As can be seen from the figure the WPU consists of the following parts:

- Photodiode amplifier
- Demodulator Module
- Pitch and Yaw Calculation
- Servo Filtering
- Motorized Mirror, Calibration Source and Shutter Control (not shown)

Filtered pitch and yaw data from the WPU is passed to the basis transformation described in the ASC CDS system level section.

2.1. Photodiode Amplifier Design

It is currently envisioned that the photodiode amplifier design that was used for the FMI WFS prototype testing will be modified and used for the LIGO photodiode amplifiers. During the preliminary design phase the design will be modified to match the LIGO ASC CDS requirements. The design will be tested using an ASC prototype setup.

The current design meets most of the requirements outlined in the ASC CDS DRD but some changes may be required. These changes include:

- Retuning of front end tank circuit and traps to LIGO frequencies.
- Transimpedance (Gain) changes to meet LIGO requirements.
- Addition of operator selectable gain changes.
- Circuit packaging changes to meet LIGO CDS design specifications and standards.

2.2. Demodulator Design

It is currently envisioned that the demodulator design (LIGO D950TBD) that was used for the FMI WFS prototype testing will be modified and used for the LIGO demodulators. During the preliminary design phase the design will be modified to match the LIGO ASC CDS requirements. The design will be tested using an ASC prototype setup.

The current design meets most of the requirements outlined in the ASC CDS DRD but some changes may be required. These changes include:

- Gain changes to match LIGO requirements.
- IF filter tailoring to match demodulator output to WPU ADC inputs. (This filtering may be used as a combination anti-alias and whitening filter.)
- Addition of operator selectable gain changes.
- Circuit packaging changes to meet LIGO CDS design specifications and standards.

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2.3. Pitch and Yaw Processing and Filtering Section Design

The figure below is a block diagram of the pitch and yaw processing and servo filtering section for the demodulated outputs from the demodulator module.
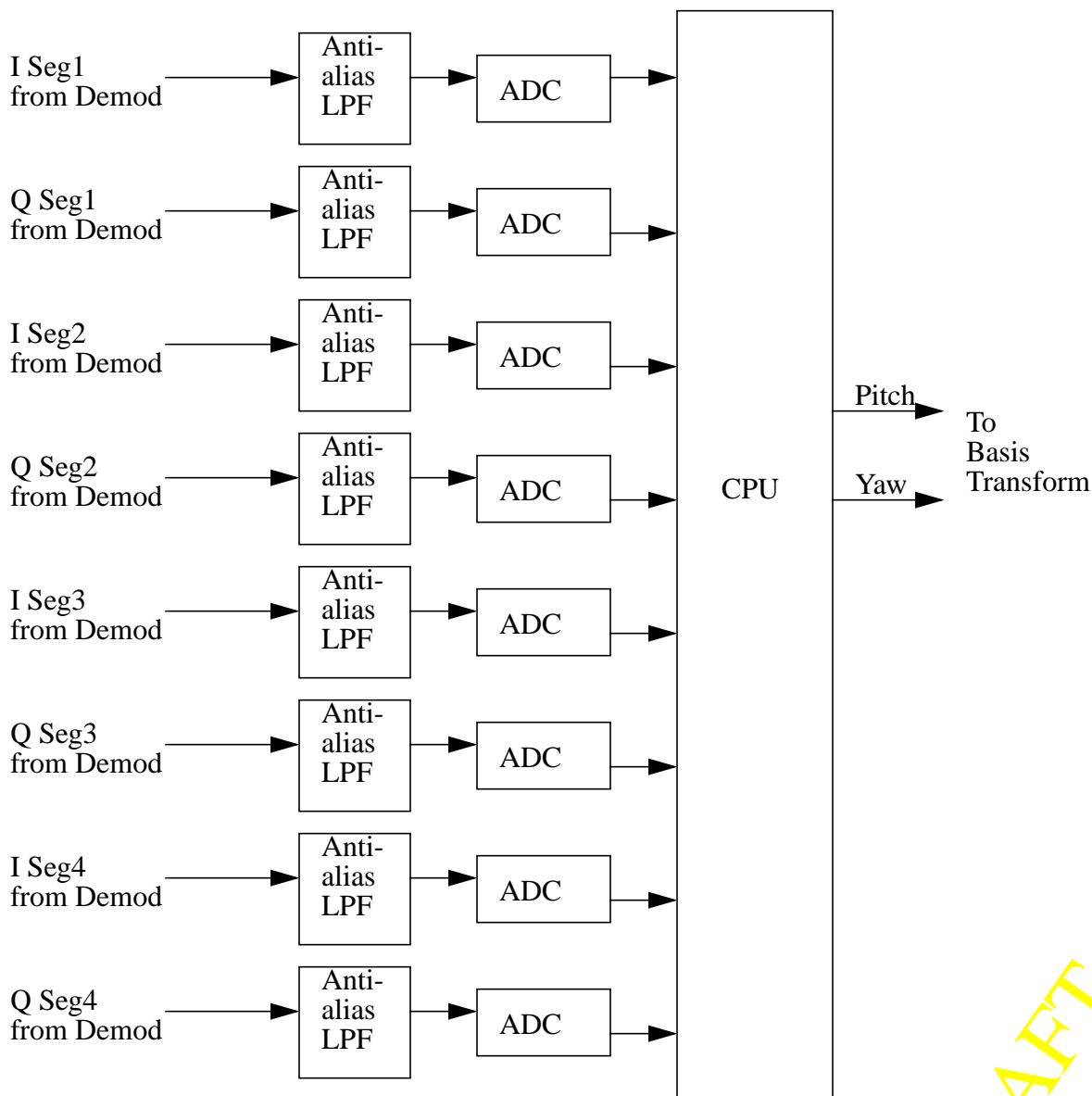
Figure 4: Pitch and Yaw Processing and Filtering Section Block Diagram for One WPU

The ADCs shown in the figure are one channel each of a VMIC model 3123, 16 bit, 32 channel module located in the ASC VME crate in the LVEA. The sampling rate for the ADCs will be 10 Ksamples/second. Testing done within the CDS group and data sheets obtained from the manufacturer show that the input referred noise for the VMIC 3123 will be less than $(10uV)/(\sqrt{Hz})$

when the input voltage range is set to +/- 10 volts, which is less than the required $(100uV)/(\sqrt{Hz})$.

The CPU is a Heurikon model baja 4700 VME processor in the ASC CDS VME crate in the LVEA. Data from the ADCs is passed to the CPU via the VME backplane. Initial calculations and estimates show that the baja 4700 processor operating under the VxWorks operating system should be adequate to perform the processing for at least 2 WPUs. Testing during the preliminary design phase will verify these estimates.

The block diagram and components for monitoring the DC outputs from the demodulator module will be similar to the figure shown above, with the exception that the ADCs will be model TBD, multi-channel, 16 bit ADC modules sampling at 10 (TBR) samples per second.
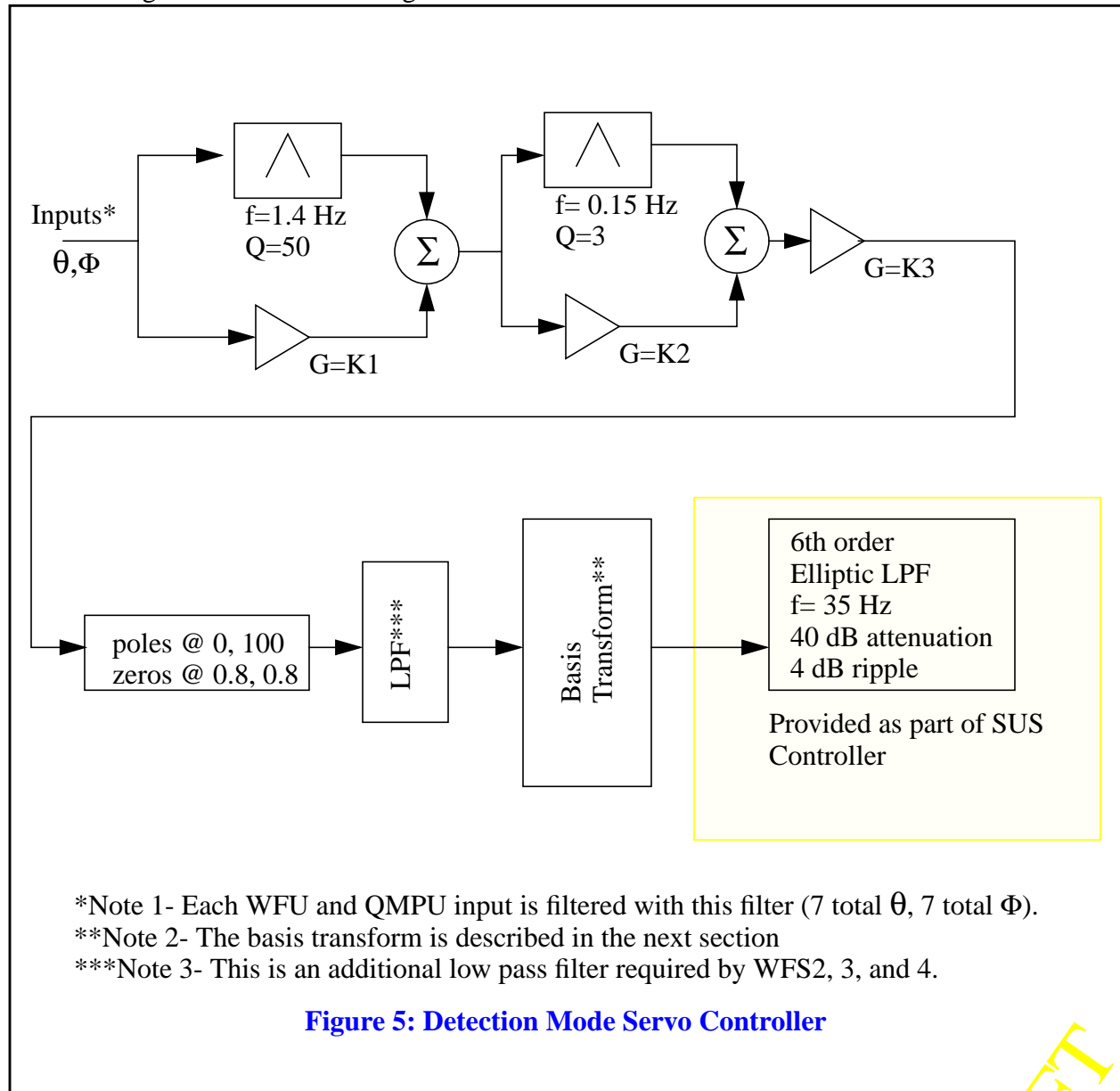
The table below is a list of the signals to be acquired and processed by each WPU.

Table 2: WPU Signals and Sampling Rates

Signal	*Sample Rate (samples/sec)*
I segment 1	10 K
Q segment 1	10 K
I segment 2	10 K
Q segment 2	10 K
I segment 3	10 K
Q segment 3	10 K
I segment 4	10 K
Q segment 4	10 K
DC segment 1	10
DC segment 2	10
DC segment 3	10
DC segment 4	10
TOTAL PER WPU	Fast (10K) Channels = 8 Slow (10) Channels = 4

The pitch and yaw calculations and the servo filtering will be as specified in the ASC CDS DRD. A block diagram is shown in the figure below.

Inputs*
θ,Φ

f=1.4 Hz
Q=50

G=K1

Σ

f= 0.15 Hz
Q=3

G=K2

Σ

G=K3

poles @ 0, 100
zeros @ 0.8, 0.8

LPF***

Basis
Transform**

6th order
Elliptic LPF
f= 35 Hz
40 dB attenuation
4 dB ripple

Provided as part of SUS
Controller

*Note 1- Each WFU and QMPU input is filtered with this filter (7 total θ, 7 total Φ).
**Note 2- The basis transform is described in the next section
***Note 3- This is an additional low pass filter required by WFS2, 3, and 4.

Figure 5: Detection Mode Servo Controller

2.4. Motorized Mirror and Shutter Control

Each WPU will have motorized mirrors and shutters that must be controlled by the operator. The motorized mirror and shutter controls will be provided using VME analog input, output and binary input and output modules and EPICS software running on a CPU such as the Motorola MVME162-333.

2.5. Calibration Procedures

As the system designs and requirements are refined during the preliminary design phase, the on and off line calibration procedures will be developed.

3   QUADRANT MONITOR PROCESSING UNIT DESIGN

Quadrant monitor sensor photodiodes are located on optical tables in the LVEA and VEAs. The rough placement of the optical tables is depicted in Figure 2: ASC CDS Functional Layout. Photodiodes in the LVEA are located on the same optical tables as the LSC and wavefront photodiodes.

3.1. Photodiode Amplifier Design

A four quadrant photodiode amplifier will be developed to meet the requirements outlined in the ASC CDS DRD. The QMPD requirements versus operating mode are repeated in the table below.

**Table 3: QMPD Requirements vs. Operational Modes**

IFO State	Transimpedance gain (each element)	Output Noise Density (f>30 Hz)	Bandwidth (3 dB)
2. Recycled Michelson	10 Mohm	N/A	>100 Hz
3. Recycled Michelson + one arm	10 Mohm/250 Kohm	N/A	>100 Hz
4. Detection Mode	500 ohm	$(20nV)/(\sqrt{Hz})$	> 1 KHz

Gain selection will be operator controlled and be in nominal 6 dB and 20 dB steps from 500 ohms to 10 Mohms. The output filtering may be tailored to perform the anti-aliasing and whitening required before the QMPU ADC shown in Figure 6: Pitch and Yaw Processing and Filtering Section Block Diagram for One QMPU.

3.2. Pitch and Yaw Processing and Filtering Section Design

The figure below is a block diagram of the pitch and yaw processing and servo filtering section for the QMPD outputs from the photodiode amplifier.
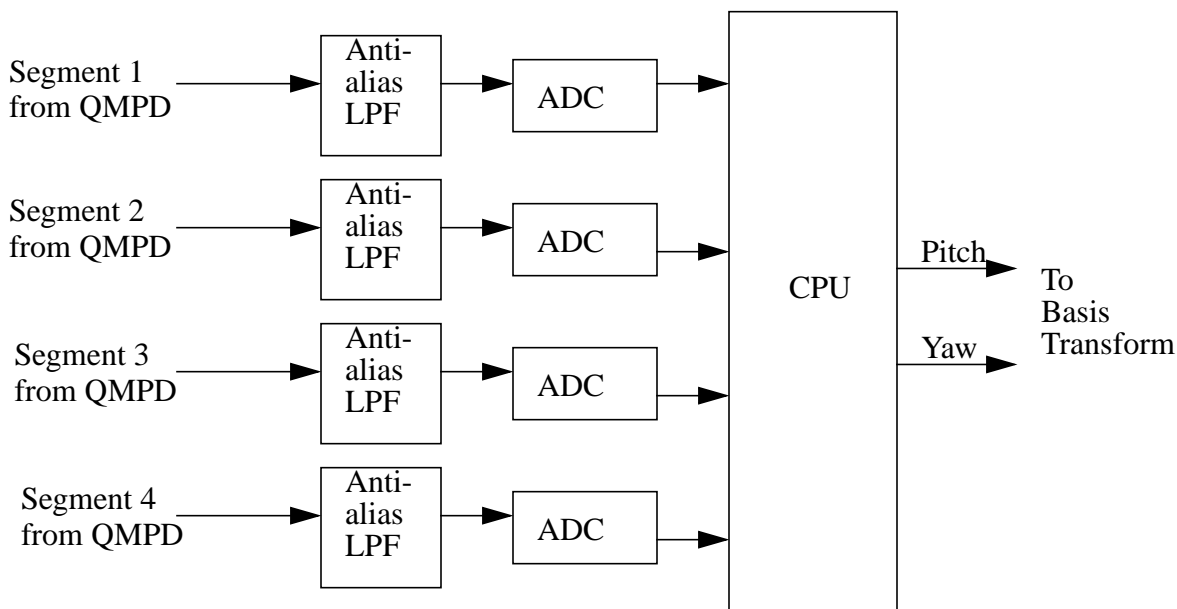
**Figure 6: Pitch and Yaw Processing and Filtering
Section Block Diagram for One QMPU**

The ADCs shown in the figure are one channel each of a VMIC model 3123, 16 bit, 32 channel module located in the ASC VME crate in the LVEA. The sampling rate for the ADCs will be 10 Ksamples/second. Testing done within the CDS group and data sheets obtained from the manufacturer show that the input referred noise for the VMIC 3123 will be less than $(10uV)/(\sqrt{Hz})$ when the input voltage range is set to +/- 10 volts, which is less than the required $(100uV)/(\sqrt{Hz})$.

The CPU is a Heurikon model baja 4700 VME processor in the ASC CDS VME crate in the LVEA. Data from the ADCs is passed to the CPU via the VME backplane. Initial calculations and estimates show that the baja 4700 processor operating under the VxWorks operating system should be adequate to perform the processing for more than one QMPU. Testing during the preliminary design phase will verify these estimates.

The pitch and yaw calculations and the servo filtering will be as specified in the ASC CDS DRD.

The pitch, yaw and sum calculation is shown in the following equations,

$$Y_{Position} = \frac{K_{Top}(Top - Top_{offset}) - K_{Bottom}(Bot - Bot_{offset})}{Sum}$$

$$X_{Position} = \frac{K_{Left}(Left - Left_{offset}) - K_{Right}(Right - Right_{offset})}{Sum}$$

$$Sum = (K_{Top}Top) + (K_{Bot}Bot) + (K_{Left}Left) + (K_{Right}Right) - \sum_{Top}^{Right} offsets$$

where the offsets for each channel are obtained during a calibration procedure in which the beam to quad photodiode is blocked and the offset voltage for each channel is measured and stored for use in the calculations listed above. The gain constants are obtained during a calibration procedure in which the quad photodiode is uniformly illuminated and the output of each channel is measured. The relative gain for each channel is then calculated once the offsets are subtracted.

The filtering function will be the same as for the WPU data shown in Figure 5: Detection Mode Servo Controller.

4   OPTICAL LEVER DESIGN

A block diagram of a typical optical lever is shown in the figure below.
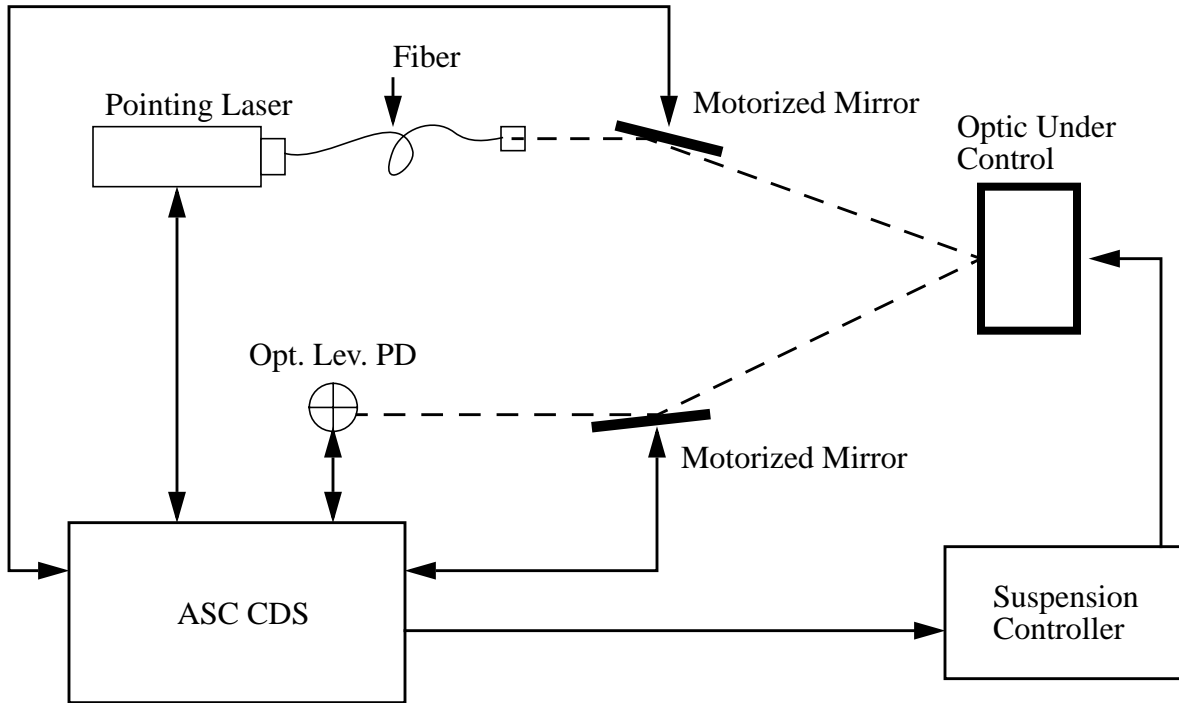
Figure 7: Optical Lever Block Diagram

Optical levers are located on the following optics:

- Recycling Mirror
- Beam Splitter
- X Arm ITM
- Y Arm ITM
- X Arm ETM
- Y Arm ETM
- 2 Folding Mirrors for 2 Km IFO

4.1.   Photodiode Amplifier Design

A four quadrant photodiode amplifier will be developed to meet the requirements outlined in the ASC CDS DRD. This amplifier will be similar in design to the amplifiers that are currently used on the 40 meter and Phase Noise Interferometers. The specifications for the amplifier are:

- Gain: 1000 ohms
- Frequency Response: > 1KHz
- Input Referred Noise: $< 6 \times 10^{-12} \dfrac{A}{\sqrt{Hz}}$ for frequencies > 40 Hz

4.2. Optical Lever Control and Monitoring Design

The figure below is a block diagram of a typical optical lever receiver.
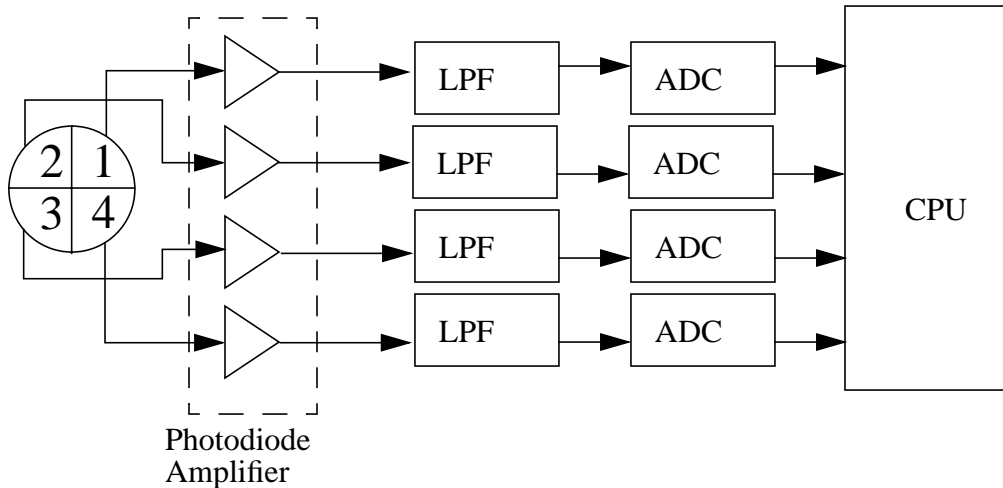
Figure 8: Optical Lever Receiver Block Diagram

Motorized mirrors and the pointing lasers (see Figure 7: Optical Lever Block Diagram) will be controlled via analog input and output and binary input and output modules in the ASC CDS VME crates.

The X and Y position and Sum calculations including the offset and gain adjustments described in the ASC CDS DRD will be performed in software.

The ADCs shown in the figure will be multiple channel, 16-bit VME modules. The CPU will be a Motorola MVME162.

5   CAMERA SYSTEM DESIGN

The nominal placement of cameras for one interferometer at the Washington site is shown in the table below.

Table 4: Nominal Camera Locations for One WA IFO

Location	Number of Cameras	Nominal Viewing
LVEA; at BSC1	2-4	interior of BSC1
LVEA; at BSC2	2-4	interior of BSC2
LVEA; at BSC3	2-4	interior of BSC3
End Station; X Arm/Y Arm	2-4/2-4	interior of BSC9/BSC10
LVEA; at BSC1	1	surface of Y-arm ITM
LVEA; at BSC2	1	surface of beamsplitter
LVEA; at BSC3	1	surface of X-arm ITM
End Station; X Arm/Y Arm	1/1	surface of X-arm/Y-arm ETM
LVEA; at HAM3	1	surface of recycling mirror
LVEA; at HAM2	1	surface of MC mirror
LVEA; at HAM1	1	surface of MC mirror
ISC Table; Rec Cav sample	1	recycling cavity beam
ISC Table; Anti-symmetric port	1	Anti-symmetric beam
ISC Table; Reflected port	1	Reflected beam
ISC Table; ETM transmission, X/Y Arm	1/1	X/Y Arm ETM transmitted beam
ISC Mode Cleaner Table	1	MC transmitted beam

The figure below is a block diagram of how the ASC camera video outputs can be displayed on operator screens. The AVA-300 is a multimedia encoder that will interface as many as six cameras to a 155 Mbps ATM link. Any operator console running the SVA software can then view the out-

put of any camera (each console can view a different camera output). Both the AVA-300 and the SVA software are available from Nemesys Research Ltd. (A subsidiary of Fore Systems Inc.).

Cameras located on chamber ports, ISC optics tables, etc.
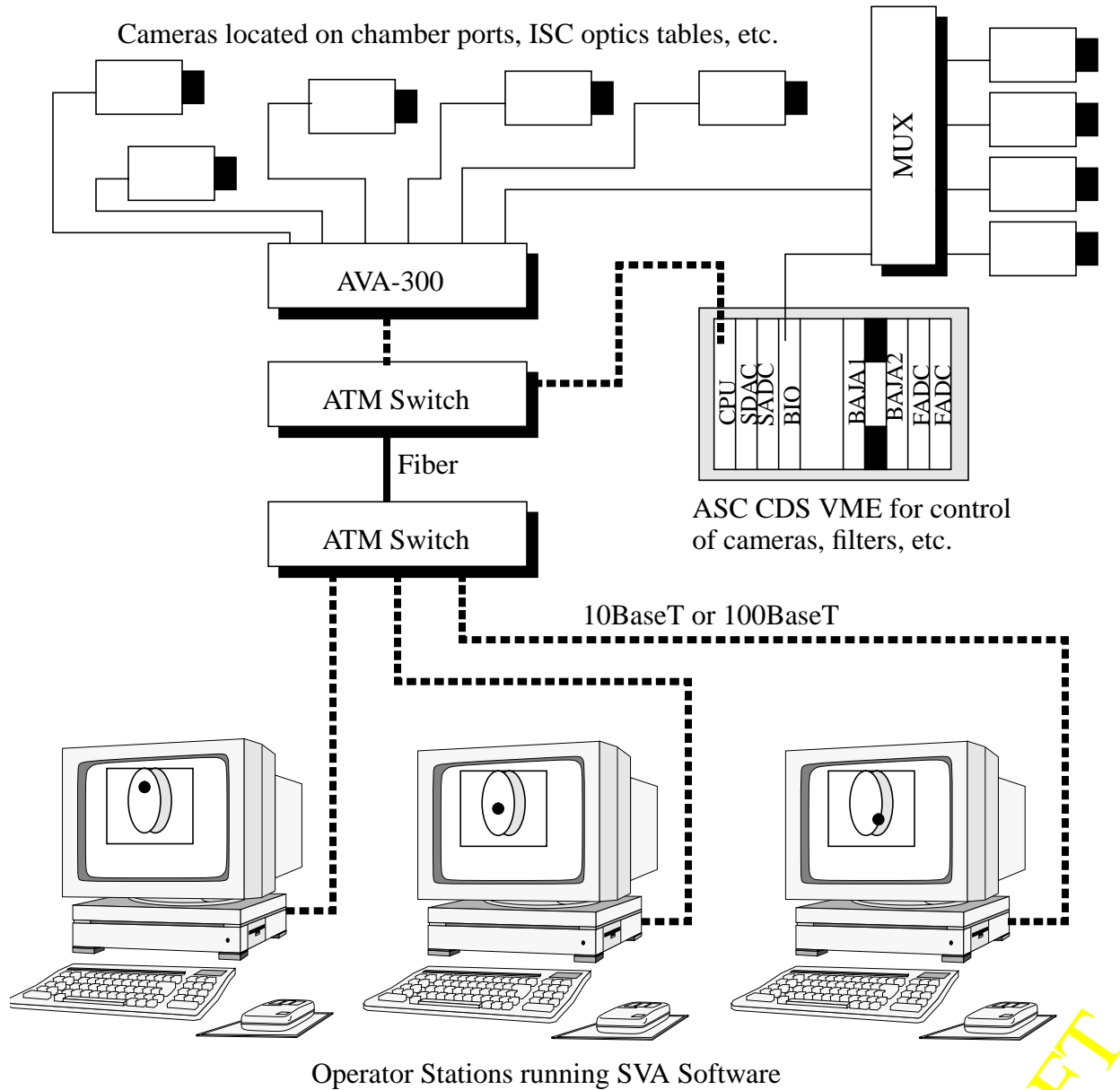
Figure 9: ASC CDS Camera Connections

Each AVA-300 will handle as many as six video inputs. One AVA-300 would be placed in each building. The six inputs would be adequate for the mid and end station buildings, but the LVEA has many more than six cameras. Cameras in the LVEA will be run through multiplexers prior to connection to the AVA-300 unit as shown on the right hand side of the figure. The multiplexers will be controlled by the operator via binary output modules in the ASC CDS VME crates.

Images on the operator consoles will then be captured using tools such as "snapshot" available on the workstation.

Camera controls such as panning, zooming IR filters and test mass illuminators will be provided using VME analog input, output and binary input and output modules and EPICS software running on a CPU such as the Motorola MVME162-333.

6 ASC CDS SYSTEM LEVEL DESIGN

6.1. Design Description

The figure below is a block diagram wavefront sensor and quadrant monitor portions of the ASC CDS system. Blocks within the shaded region are part of the system level design. Other blocks are described in the sections that follow.
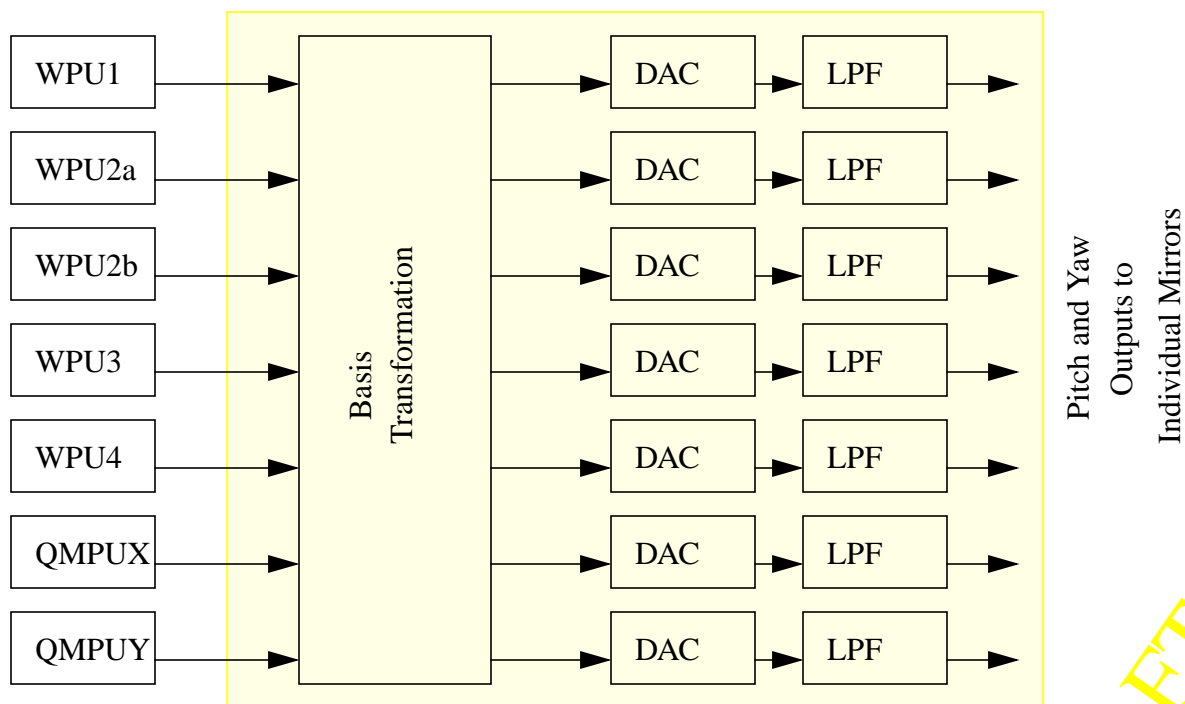
Figure 10: WFS and QMPD Block Diagram

The basis transformation is a 7x7 matrix conversion of the pitch and yaw information from the WPUs and QMPUs. The basis transformation matrix is depicted in the following equations,

$$
\begin{bmatrix} \Theta_{WFS1} \\ \Theta_{WFS2} \\ \Theta_{WFS3} \\ \Theta_{WFS4} \\ \Theta_{WFS5} \\ \Theta_{QMPU1} \\ \Theta_{QMPU2} \end{bmatrix} \times \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} & a_{15} & a_{16} & a_{17} \\ a_{21} & a_{22} & a_{23} & a_{24} & a_{25} & a_{26} & a_{27} \\ a_{31} & a_{32} & a_{33} & a_{34} & a_{35} & a_{36} & a_{37} \\ a_{41} & a_{42} & a_{43} & a_{44} & a_{45} & a_{46} & a_{47} \\ a_{51} & a_{52} & a_{53} & a_{54} & a_{55} & a_{56} & a_{57} \\ a_{61} & a_{62} & a_{63} & a_{64} & a_{65} & a_{66} & a_{67} \\ a_{71} & a_{72} & a_{73} & a_{74} & a_{75} & a_{76} & a_{77} \end{bmatrix} = \begin{bmatrix} \Theta_{ITM1} \\ \Theta_{ETM1} \\ \Theta_{ITM2} \\ \Theta_{ETM2} \\ \Theta_{RM} \\ \Theta_{BS} \\ \Theta_{IB} \end{bmatrix}
$$

$$
\begin{bmatrix} \Phi_{WFS1} \\ \Phi_{WFS2} \\ \Phi_{WFS3} \\ \Phi_{WFS4} \\ \Phi_{WFS5} \\ \Phi_{QMPU1} \\ \Phi_{QMPU2} \end{bmatrix} \times \begin{bmatrix} b_{11} & b_{12} & b_{13} & b_{14} & b_{15} & b_{16} & b_{17} \\ b_{21} & b_{22} & b_{23} & b_{24} & b_{25} & b_{26} & b_{27} \\ b_{31} & b_{32} & b_{33} & b_{34} & b_{35} & b_{36} & b_{37} \\ b_{41} & b_{42} & b_{43} & b_{44} & b_{45} & b_{46} & b_{47} \\ b_{51} & b_{52} & b_{53} & b_{54} & b_{55} & b_{56} & b_{57} \\ b_{61} & b_{62} & b_{63} & b_{64} & b_{65} & b_{66} & b_{67} \\ b_{71} & b_{72} & b_{73} & b_{74} & b_{75} & b_{76} & b_{77} \end{bmatrix} = \begin{bmatrix} \Phi_{ITM1} \\ \Phi_{ETM1} \\ \Phi_{ITM2} \\ \Phi_{ETM2} \\ \Phi_{RM} \\ \Phi_{BS} \\ \Phi_{IB} \end{bmatrix}
$$

where ITM= input test mass, ETM= end test mass, RM= recycling mirror, BS= beam splitter, and IB= input beam.

The conversion matrix elements are TBD. This conversion will be done in a CPU designated as the ISCC (ISC Computer, Figure 2: ASC CDS Functional Layout). This CPU will be a Heurikon Model Baja 4700 located in the ASC VME crate in the LVEA near HAM 2. Data from each of the WPUs will be passed via Reflective Memory. Data from the QMPUs (located in VME crates in the end station VEA) will also be passed via Reflective Memory.

The DACs shown in the figure will be located in VME crates near the suspension controller controlling each of the optics under control. These DACs will be 16 bit PMC module DACs, model TBD. The output sample rate will be 10 Ksamples/second. Data is passed from the ISCC VME crate to DAC VME crates via Reflective Memory.

The low pass filters will be 6th order 35 Hz, 4 dB ripple, 60 dB stopband attenuation filters implemented in hardware inside the suspension controller. The interface will be as described in the ASC CDS DRD.

6.2. System Layout

The block diagram in Figure 11: ASC CDS System Layout for One IFO shows how the ASC CDS
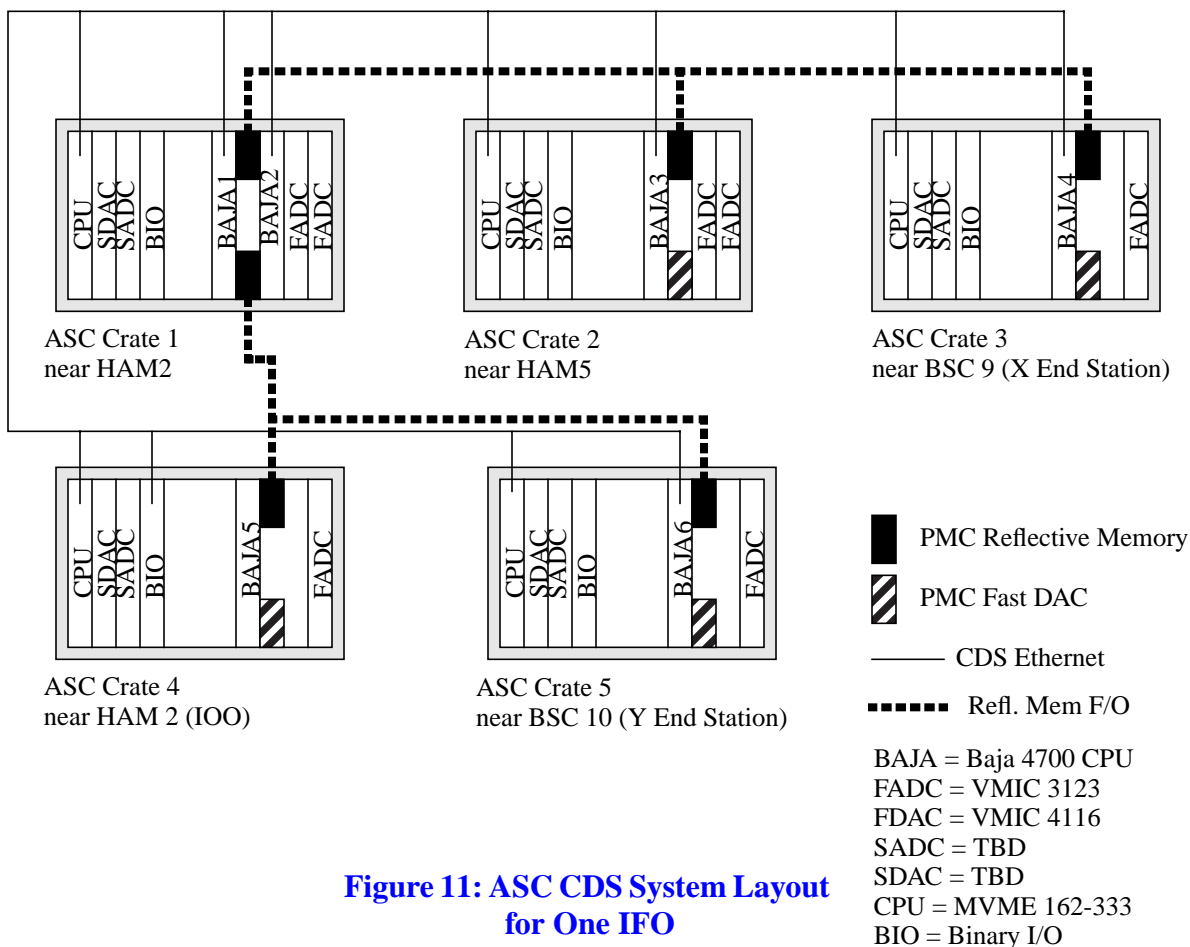
Figure 11: ASC CDS System Layout for One IFO

system can be configured to meet the requirements outlined ASC CDS DRD.

The processor assignments are as follows:

- BAJA1 - WPU and QMPU basis transformation and output angle calculation and WPU 2 functions.
- BAJA2 - WPU 3 and WPU 4 functions.
- BAJA3 - WPU 5 functions and control of DAC for X and Y Arm ITM angle outputs.
- BAJA4 - X Arm QMPU functions and control of DAC for X Arm ETM angle outputs.
- BAJA5 - WPU 1 functions and control of DAC for Input Beam, Recycling Mirror and Beam Splitter angle outputs.
- BAJA6 - Y Arm QMPU functions and control of DAC for Y Arm ETM angle outputs.

The PMC reflective memory modules are Systran model H-AS-DPMCN reflective memory modules plugged into one PMC slot of the Baja 4700 processor.

The PMC Fast DAC modules are TBD model TBD multi-channel, 16-bit DAC modules plugged into one PMC slot of the Baja 4700 processor.

The CPU, SDAC (slow DAC), SADC (slow ADC) and BIO (binary input/output) modules are standard VME modules available from commercial manufacturers. The SDAC and SADC modules will be multi-channel, 16 bit modules. These modules will be used to control and monitor motorized mirrors, optical levers, cameras, shutters, etc. located near each of the VME crates. Typically the motorized mirrors and DC readbacks from a particular WFS or QMPD will be assigned to the VME crate that houses the WPU processor for that particular unit.

6.3. System Software

Two types of software will be developed for the ASC CDS system. The first type of software is the typical EPICS based slow control and monitoring software that is currently be developed for other LIGO systems and currently in use on the 40 meter interferometer.

The second type of software that will be developed is the high speed signal processing software that is required by the WPUs, QMPUs and ISCC. This software will be modeled using the Alta Group SPW software currently in use by the CDS group. The code will be written in the C programming language and compiled for operation on the Baja 4700 processor running under the VxWorks operating system. EPICS channel access will be used to provide network connection and communications between the processor and other CDS systems such as operator consoles, servers and other processors.

Operator interfaces, backup and restore functions and alarm handlers will be developed using the standard LIGO CDS tools.

6.4. ASC CDS Modes of Operation

The ASC CDS system hardware and software will be designed to support the various modes of operation described in the ASC PDD and the ASC CDS DRD. These modes of operation include:

- Initial Alignment Mode -
  - •• Optical Lever Zero Setting
  - •• Initial Beam Direction Zero
- Transition to Acquisition Alignment Mode -
  - •• Unlocked Recycled Michelson
  - •• Resonating Short Michelson (state 2)
  - •• Recycled Michelson and One Arm Locked (State 3)
- Detection Mode
  - •• Establish Center of Rotation for Masses
  - •• Detection Mode Hold

For the most part the various modes of operation put no requirements on the system design that are not required for the Detection Mode or "normal" of operation of the system. The different modes only require that individual pieces of the system be operational during the commissioning

phase of the interferometer. The installation and commissioning schedule for the ASC CDS system will be adjusted to ensure support of each mode of operation as it is required.

7   ASC CDS PROTOTYPE SETUP

A combined ASC and ASC CDS prototype test setup will be developed during the preliminary design phase. This prototype will include:

- A suspended optic and suspension controller,
- a laser source,
- at least one WFS and WPU, including motorized mirrors,
- at least one QMPD and QMPU,
- the ISCC,
- at least one camera and video dispaly system,
- at least one optical lever.

This test setup is fully described in D. Sigg's document (LIGO T970TBD). Ablock diagram of the proposed setup from this document is included below for reference.
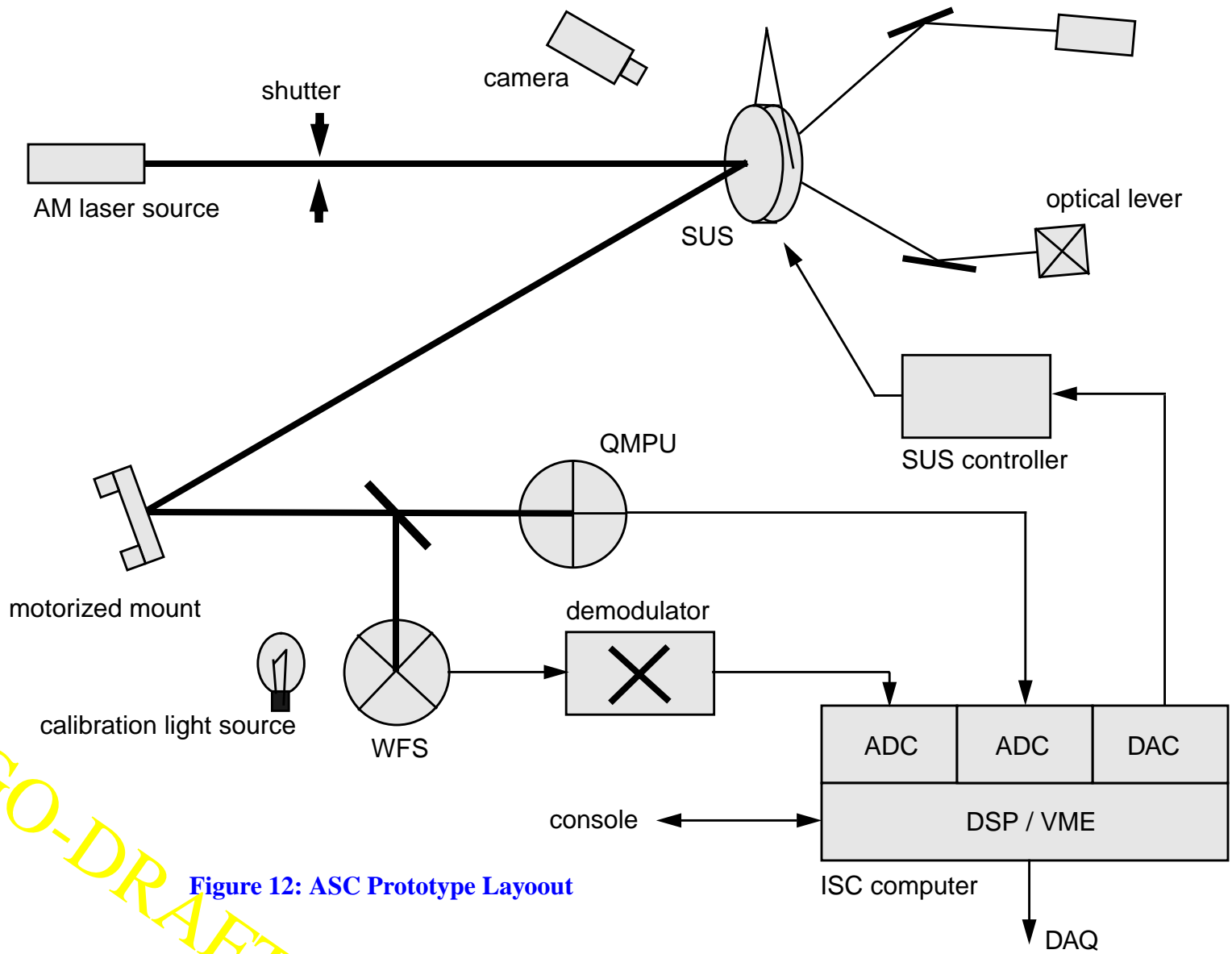
Figure 12: ASC Prototype Layoout