LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

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UK PUM Driver Pre-Production Prototype Bench Test and Evaluation		
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1 Introduction

This report documents the bench test results and evaluation of the AdL Suspension PUM Driver chassis supplied as a pre-production prototype by the University of Birmingham. Bench tests were conducted in accordance with LIGO document number T080024-00-C, "AdL UK PUM Coil Driver Pre-Production Test Plan". A link to the completed test plan with results is included in Appendix A of this document. The design requirements for the PUM Driver can be found in LIGO document number T060067-00-C, "AdL Quad Suspension UK Coil Driver Design Requirements".

The format of this report roughly follows the format of LIGO document T070288-00-C, "Adl Noise Prototype Electronics Test Plan". The tests outlined in T0700288-00-C are a series of tests and evaluations that will be used to evaluate the full set of electronics provided by the University of Birmingham for the AdL Quad Suspension system. The major categories of the plan are:

- Manufacturing
- Operational
- Performance

This test report covers relevant portions corresponding to each of these categories.

2 Manufacturing

2.1 Quality of Manufacture

The PUM Driver chassis provided to LIGO for testing and evaluation is a pre-production prototype and should be treated as such. Many of the comments and suggestions in this section relate to the prototype nature of the driver and should not be taken as criticism, but as general recommendations. The photos below are front and rear views of the PUM Driver with the cover removed.

Figure 1: PUM Driver Chassis Front View

Figure 2: PUM Driver Chassis Rear View

2.1.1 Chassis Labeling and Identification

As can be seen from the photos, front and rear panel labels have been made using a label maker. In the full production units these labels should be implemented in a more permanent manner such as engraving or permanent stenciling. The drawing number associated with the chassis assembly drawing should also be added to front or rear panel labels.

Power indicators are included on the front panel, but the power indicators for the monitor board are inside the chassis and there are no indicators on the rear panel. It would be advantageous if there were some indication of power status on the rear of the chassis near the power switch.

2.1.2 Circuit Boards

The photo below is a closer view of the PUM Driver board. As can be seen from the picture, the circuit board is multi-layer, professionally manufactured circuit board. The larger silver objects running down the middle of the board are capacitors. Several blue capacitors are installed laying down because they were added to the design following the design of the circuit boards. This is expected in a pre-production prototype, and it is expected that these capacitors will be added to the board design prior to production. These capacitors can be seen more clearly in Figure 4. Additionally, the purple wiring leading from the driver board to the fuseholders mounted on the rear of the chassis is soldered directly into the board and the wires routed to the fuse holders. Prior to production, wire attachment and routing and fuseholder placement should be rethought and if possible, the wires eliminated by using some type of board mounted fuseholder that protrudes from either the front or rear panel of the chassis. This could require a significant amount of board layout and chassis redesign. Each channel of the circuit board flows from the front to the rear of the chassis and appears to have been produced using the multi-channel design features available in Altium. This is a very efficient and convenient way to produce designs that utilize the same circuit topology for multiple channels. When this feature is used, the logical designators for each component in the design are the same since the channel number portion of the physical designator is suppressed on the silkscreen. Therefore, it is very important that the channels be clearly identified and distinguished on the board. This can be done easily by adding lines and channel designation text to the silkscreen layer of the board. It is highly recommended that these lines and text be added to the production design.

The Monitor board was manufactured in a similar fashion and the only circuit board issue observed was that the mounting hole size for the 37 pin sub D connector were not correct. This should be corrected prior to production. Both boards (driver and monitor) are identified in the space provided

with the drawing number, revision number and serial number for the board. The circuit board (pcb artwork) revision number is included on the silkscreen for each board.

It can not be clearly seen in any of the included pictures, but each of the circuit boards (Driver and Monitor) have many test points that are clearly labeled. These test points are the same SMT style that has been used in many LIGO and AdL designs. Due to procurement problems, some of the test point components were not stuffed on the initial PUM Driver, but it is assumed that production units will be fully populated. The only recommendation in this area would be to, if possible, include a few more ground test points located around the boards. These additional test points would aid in board test and debug.

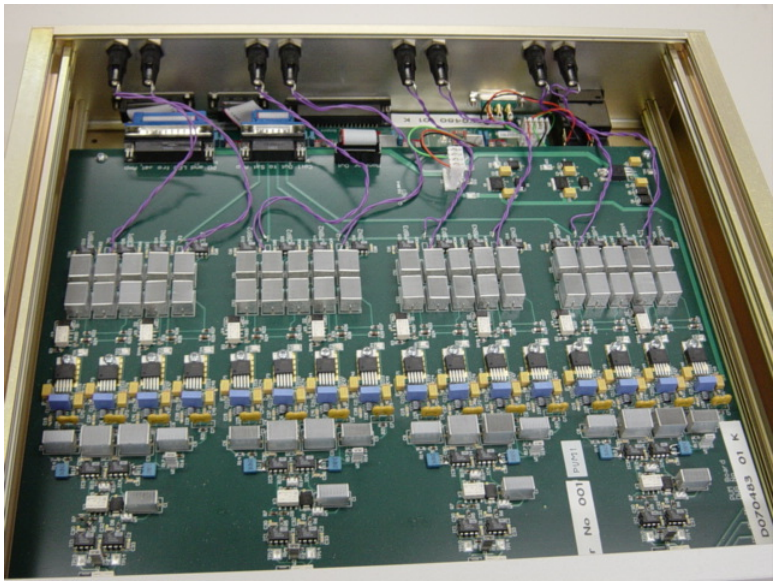

Figure 3: PUM Driver Circuit Board

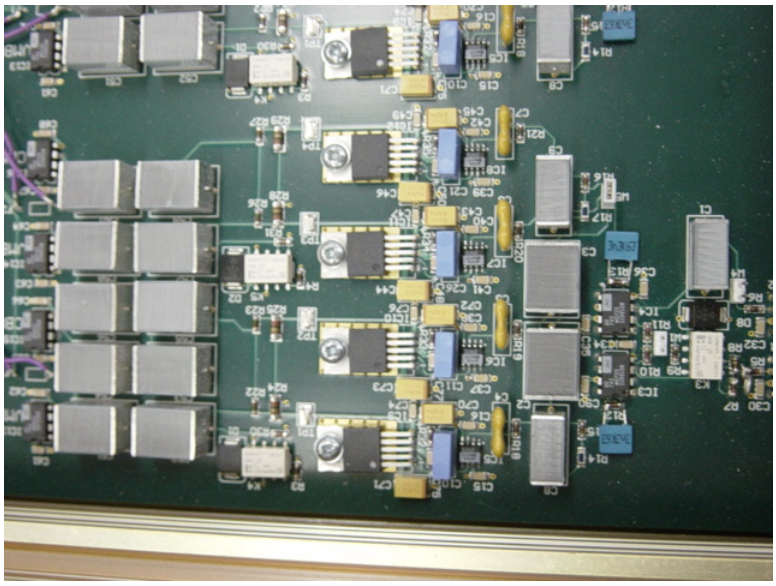

Figure 4: Close up of Added Capacitors

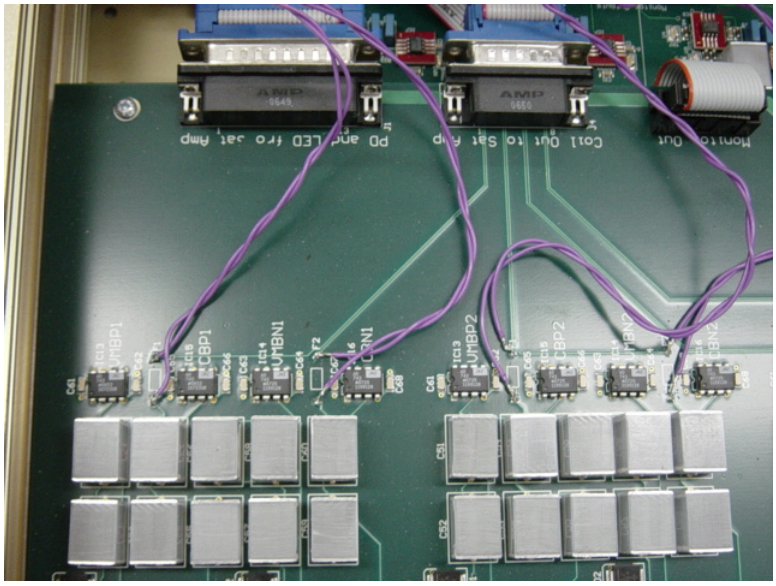

Figure 5: Fuse Wire Connections to Board

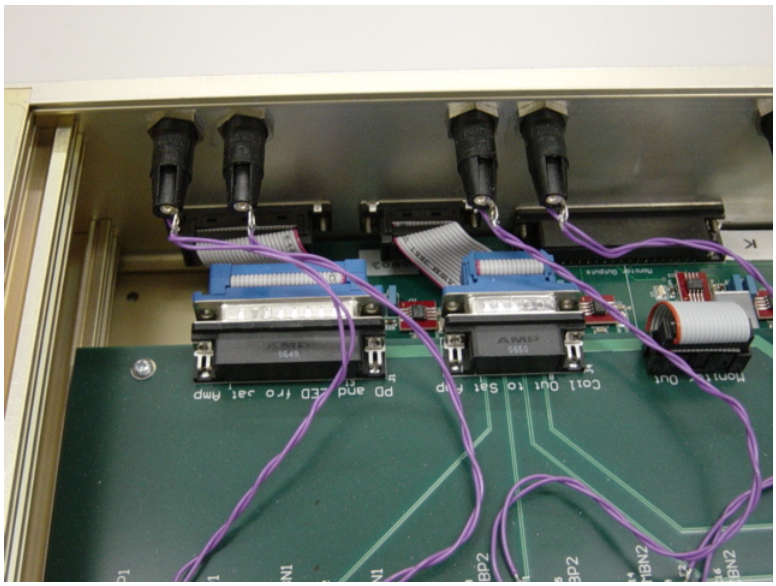

Figure 6: Rear Panel Mounted Fuse Holders

The PUM Driver Board is capable of producing currents in excess of 400 mA per channel. The trace widths for these high currents paths appear to be 10-12 mils. Although this may be adequate, it is recommended that these widths be increased to a minimum of 25mils (0.635 mm). In general, it is recommended that all circuit board traces be oversized if possible. Many of the board designs used in AdL will be changed and modified as the project progresses. These design changes will require component changes and board rework and larger traces are less prone to damage.

2.1.3 Cabling, Connectors and Harnesses

The photo below is a closer view of the input power connections and chassis power wiring. As can be seen from the picture, the solder connections to the rear mounted power connectors are not adequate and wire colors used do not follow the LIGO power wiring color code. In this case, the positive voltage, return and negative voltage wire colors should be white, black and green, respectively. Heat shrink should be included over the power connector pins to prevent inadvertent shorting of the pins. Additionally, the Molex connectors used for connection to the header are the

IDC style without the retaining clip installed. It is strongly recommended that these connectors be replaced with the crimp pin version.

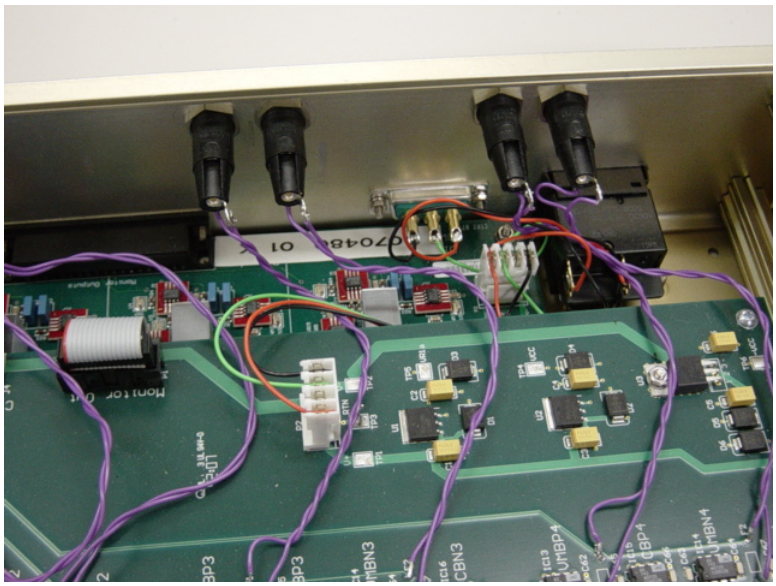

Figure 7: Close-up View of Power Wiring and Connectors

The connectors used for incoming and outgoing field cables are sub D connectors. These connectors all have jack screws used for retaining the field cables and are acceptable for the production units. Some of the sub D connectors were not the threaded insert type and used nuts and lock washers to retain the jack screws. Threaded insert style sub D connectors should be used for the production units. Internal cabling, with the exception of the power wiring noted above, is either IDC sub D or keyed header/receptacle and is acceptable for the production units.

2.2 Serviceability

The chassis used for the prototype is a Metec chassis similar, if not identical to the chassis initially used for LIGO electronics. Experience with these chassis has shown that they are very difficult to work with and subject to breakage when removing the top and bottom covers. It is strongly recommended that these chassis be replaced with a chassis that has a more easily removable top cover. If possible, it would be preferred if the LIGO chassis available from Hamilton Metalcraft Inc. were used. These chassis are readily available to both US and UK customers.

After the PUM Driver and Monitor boards had been designed, it was discovered that the 8 pin DIP package of the AD743 op amp was no longer in production and that there was no direct replacement available. These components were replaced with an SOIC version of the LT1792 mounted to an SOIC to DIP converter. These are the red components seen in some of the board pictures. Prior to production, the Driver and Monitor boards will need to be redesigned so that the converters are not necessary.

Although a complete bill of materials was not provided, a check of the availability of the capacitors used in the critical portions of the circuit showed that they may not be readily available in the US. If this is the case, then an adequate number of spares need to be provided with the production units. The same can be said of any other components used in the designs. This possibility will need to be evaluated when a complete set of documentation is supplied.

The layout of the boards in the chassis, and positioning of the connectors and fuseholders does not allow for easy removal or access to some of the components on the boards. Some thought should be given to this prior to producing the production units. The monitor board is mounted beneath the PUM

Driver board inside the chassis is essentially inaccessible. If there is a failure on the monitor board or the monitor board is suspected to have failed and requires testing or the board requires rework, the PUM Driver board must be removed completely. This could be a very labor intensive and time consuming activity given the BUF634 heat sink attachments. It is strongly recommended that the chassis design be modified to allow greater access to the monitor board. This may be as simple as mounting the monitor board on top of the driver board and/or reducing the size of the driver board. Another option that may be needed is to include some of the monitor board whitening on the driver board itself and then use a separate chassis for the rest of the monitor board filter function.

The BUF634 buffers used in the design for the high current output drivers appear to be tied to a heatsink bar or other material under the board. If this is the case and there are any special mounting requirements such as thermal washer, special screws, heat sink compound, etc. then these materials and the assembly/disassembly procedure for the unit need to be described in the documentation provided.

2.3 Adequacy of Documentation

An incomplete set of schematics was provided with the pre-production units. No bill of materials, test plans, test results, quick start guide or other documentation was provided. Prior to production all materials listed in Electronics Requirements document (T060067) and LIGO document T000053-04-D, "Universal Suspension Subsystem Design Requirements Document" will need to be evaluated.

3 Operational

3.1 Interfaces

The interfaces (connector types, pinouts, signal levels) between the University of Birmingham electronics and the AdL Electronics appear to be in compliance with Universal Design Requirements document (T000053).

3.2 Test Inputs and Monitoring

The design of the PUM Driver includes test inputs for each channel. These test inputs are connected to the input and can be enabled or disabled via an external control signal or a local board connection. When the test input is connected, the input from the control system is disconnected and visa versa. The use of the normally closed contact for the test input allows this relay to be used as a fail-safe enable/disable for the control input. The second set of contacts for these relays and for all relays used in the design provide a separate read back of the actual relay position in accordance with the requirements. One observation worthy of mentioning is that when link W2 is left open and the test input switch in the normally closed position, there is no bias return path for op amps IC1 and IC2. This leads to amplifier offsets and drifts that may not be acceptable in AdL. It is recommended that W2 be installed or bias return resistors added to the inputs.
Other monitors included in the design and in accordance with the requirements are:

- Low noise monitor of the driver output
- Fast output current monitor
- RMS current monitor

These appear to be adequate for use in AdL.

3.3 Long Term Reliability and Stability

The tests conducted on the PUM Driver took place over a two week time frame where the unit was intermittently powered and turned off for testing. While no failures or stability issues were observed, this time period is inadequate to determine if there are any long term reliability or stability issues. Additionally, no overheating or heat management issues were observed. Noise Prototype testing at LASTI should last for many months and may provide addition information in this category.

4 Performance

Performance of the chassis was measured using the set of tests outlined in LIGO document T080024-00-C. The completed report is can be viewed via the link provided in Appendix A. The sections below summarize the tests results.

4.1 Noise and Dynamic Range

4.1.1 Driver Noise

The noise requirements for the low noise mode of operation are outlined in T060067. For convenience the summary table from T060067 is repeated below.

Table 1: PUM Driver Current Noise Requirements (Low Noise Mode)

Frequency	Current Noise Requirement
1 Hz	20 nA/√Hz
10 Hz	4 pA/√Hz
100 Hz	5 nA/√Hz
1000 Hz	1000 nA/√Hz

Note that the requirements are given in units of current spectral density. Measuring current noise directly is very difficult so the tests performed measured the output voltage noise of the driver and the current noise was inferred by dividing by the load impedance at the frequency of interest. Assuming a 20 ohm coil load and the particular design chosen by the University of Birmingham the noise requirements in terms of output voltage noise can be calculated for each of the frequencies in the table. It should be noted that the design chosen by the University of Birmingham uses dual-differential output stages so the output noise voltage must be measured using a sum and difference method. This method is described in section 3.2 of the test plan. The voltage noise requirements are shown in the table below.

Table 2: PUM Driver Output Voltage Noise Requirements (Low Noise)

Frequency	Voltage Noise Requirement
1 Hz	60 uV/√Hz
10 Hz	12.1 nV/√Hz
100 Hz	15 uV/√Hz
1000 Hz	3000 uV/√Hz

The plot below shows the measured and simulated output noise versus frequency for the PUM Driver. The simulated noise data was generated using Altium Designer 6.

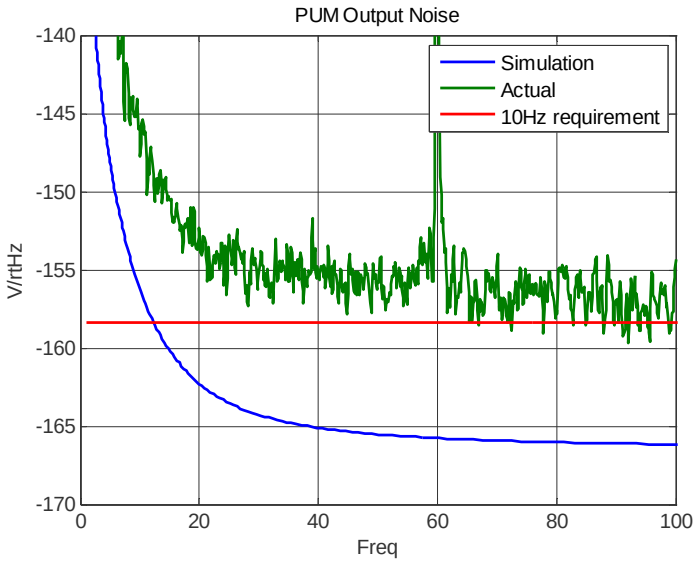

Figure 8: PUM Driver Output Noise

Note that the simulation predicts that the design submitted by the University of Birmingham is slightly worse than the requirement, 15.8nV/√Hz instead of 12.1 nV/√Hz at 10 Hz. The measured noise (green) is approximately 12 dB higher than the requirement at 10 Hz. This may be due to difficulty in making the sum and difference noise measurement described in the test plan or it may be that the noise is higher than predicted by the simulation. In either case, this needs to be investigated further once the design of the driver has been finalized (see comments in the dynamic range section of this report, section 4.1.3).

4.1.2 Monitor Noise

One of the requirements for monitors on the PUM driver is a noise monitor capable of "seeing" output referred noise voltage of the driver at 10Hz (hardest requirement) in the low noise mode of operation. In an effort to do this, the University of Birmingham has designed a noise monitor that is a high gain AC coupled differential amplifier tied to the voltage output legs of the driver. The noise monitor circuit only looks at one of the output legs for each side of the differential stage and so it does not truly measure the full output noise of the driver. The design should be corrected so that the noise monitor actually measures the sum and difference voltage of the dual differential driver design. That being said, the design submitted by the University of Birmingham was tested and the actual noise measured compared to the simulation results. These tests and the results are documented section 3.5.2 of the test plan. It was found that the measured noise was consistently more than a factor of 2 higher than predicted by the simulation. Given that the design of the noise monitor is actually only looking at one half of the total output and any noise generated in stages prior to the final stage would add linearly, this result appears to confirm the excess driver noise described in the previous section of this report.

Additionally, a simulation of the noise monitor circuit itself shows that the input-referred noise for the noise monitor is approximately 17.5 nV/√Hz at 10 Hz and would therefore be incapable of seeing the required driver output noise (15.8 nV/√Hz). If this is a firm requirement, then the noise monitor will need to be redesigned.

4.1.3 Dynamic Range

The dynamic range requirement for the PUM Driver is 16 mA_{rms} for frequencies from 200Hz to 5KHz. The dynamic range of the driver was tested in section 3.1.3 of the test plan. During these tests a design issue was discovered. Close examination of the PUM schematic and circuit board shows that resistors R14 and R17 which are unlabelled on the schematic are in actuality zero ohm resistors. This

creates a totally capacitive load for IC3 and IC4. At frequencies higher than a few Hz these ICs are incapable of driving the low impedance presented by the capacitive load which in turn means that the output stage will not meet the dynamic range requirements at high frequencies. This stage of the driver will need to be redesigned. It is worthy of mentioning that this is potentially a source of the excess noise measured and reported in the previous sections of this report.

4.1.4 Transfer Function Measurements

4.1.4.1 Driver Transfer Function

The transfer function of the PUM driver from input to current output was measured and compared to the Altium simulation. The figure below shows the simulated transfer function for one channel in the low noise mode.

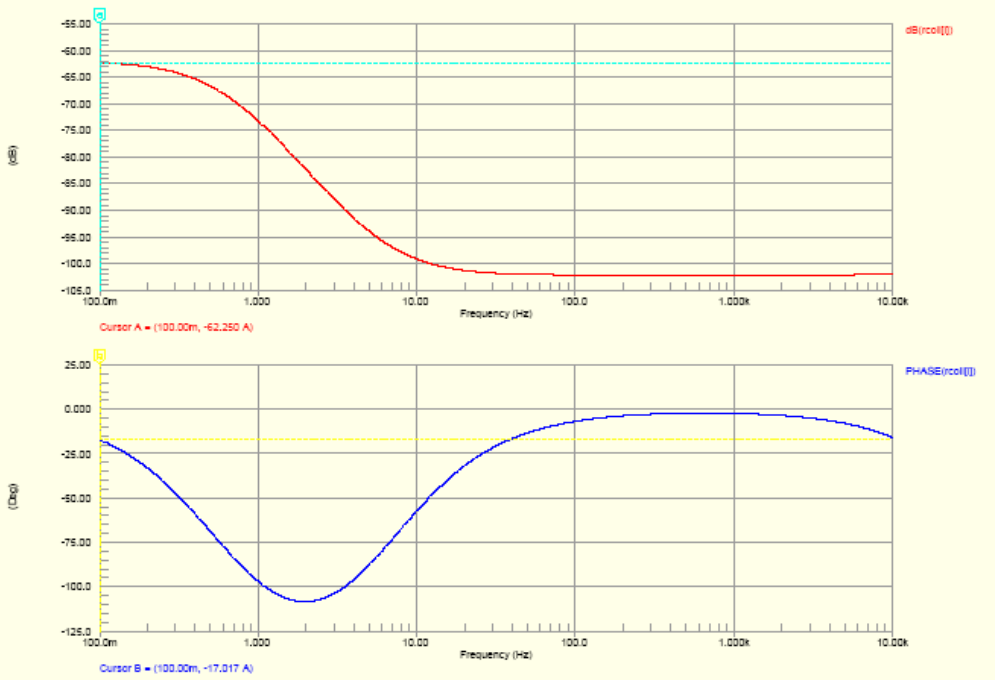

Figure 9: PUM Driver Response (Low Noise Mode)

Testing confirmed that measured response and simulated response were very similar for the low noise mode of operation; however there were deviations in the measured response and simulated response for the high dynamic range mode of operation for frequencies above 1KHz. This is likely due to the capacitors added around R12 and R13 which were not included in the simulation. The high dynamic range response is achieved by energizing relays K4 and K5. Energizing these relays adds a zero at 2Hz and pole at 145Hz to the response of the driver. This large separation in the zero/pole pair violates the order of magnitude switching requirement called out in section 2 of the requirements document (T060067). This portion of the circuit will need to be redesigned to meet the requirements.

As was stated in the previous section of this report, the stage preceding the output stage will need to be redesigned. Once this has been done, and the output mode switching has been changed, transfer function tests on the new design will need to be repeated.

4.1.4.2 Noise Monitor Transfer Function

The transfer function from the input of the driver to the output of the noise monitor circuit was measured in section 3.5.1 of the test plan. A plot of the expected transfer function for the design submitted is shown in the figure below.

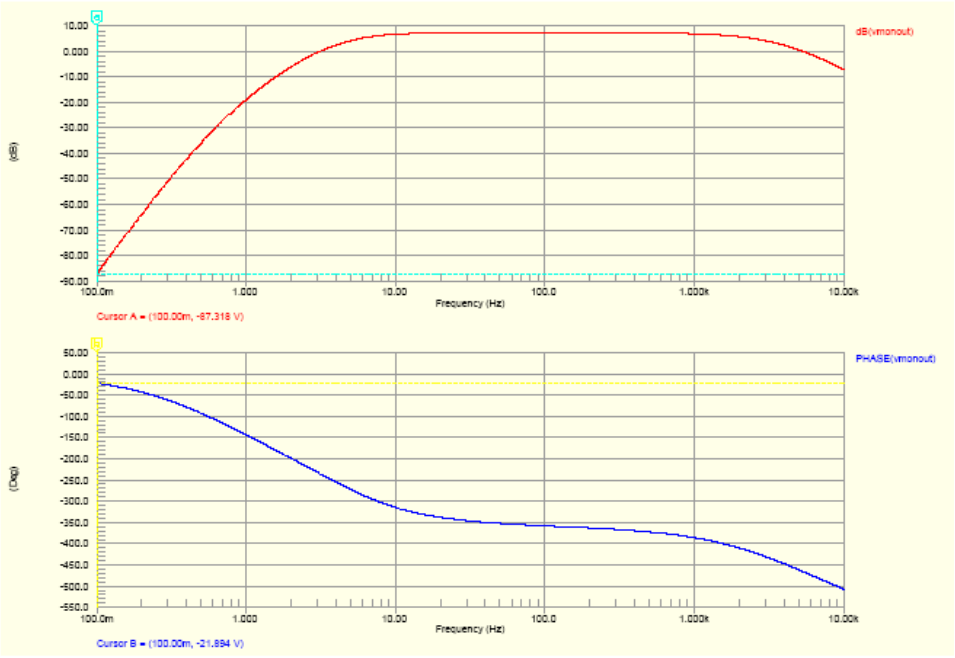

Figure 10: Noise Monitor Transfer Function, Measured from Driver Input to Monitor Output

The measured transfer functions for all four channels were found to be in close agreement with the Altium simulation, but as was previously stated in section 4.1.2 of this report, the noise monitor circuit needs to be redesigned to measure the full output noise of the driver at 10Hz. Once the circuit has been redesigned, the transfer function tests will need to be repeated.

4.2 Cross-Coupling

The cross coupling from one channel input to the output of the other channels on the driver board was measured using the procedure in section 3.3 of the test plan. The plot below shows the typical coupling observed from the input of one channel to noise monitor output of another channel on the board.

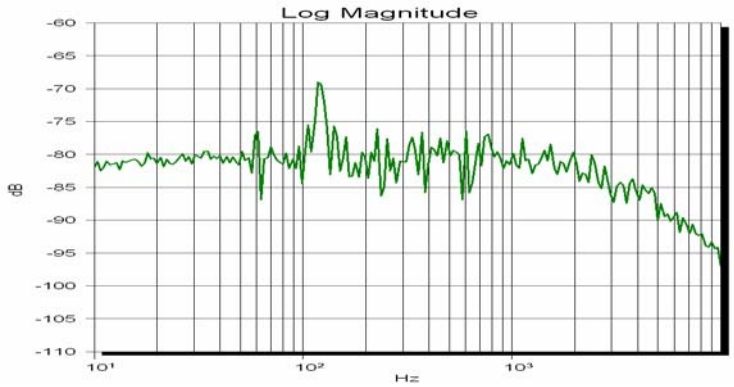

Figure 11: Typical Cross Coupling Measurement Results

As can be seen from the plot, the highest coupling measured was approximately -80dB above 10Hz. The gain of the noise monitor above 10Hz is greater than 40dB. This leads to an isolation of approximately 120dB from the input of one channel to the output voltage of another channel on the board. This should be acceptable for AdL. Note that the peak see at 120Hz is most likely a line harmonic, not cross-coupling and was therefore ignored.

4.3 Mode Switching and Glitch Tests

The design of the PUM Driver provides for multiple relays that can be used to switch each channel from what can be called "acquire" mode to the lowest noise "run" mode. The design is such that the relay can be switched using either a set of contacts or an open-collector output from the US provided control system. The design also uses another set of contacts from each relay (K3, K4 and K5) to monitor the relay position. The design meets the requirements called out in the Suspension Universal Design Requirements document (T000053).

An attempt was made to measure any glitches or transients in the current output of the driver caused by the switching of relays K3, K4 and K5. These tests are described and the results documented in section 3.4 of the test plan. During the tests no glitches or transients were observed. The switching time of the relays used on the board was found to be approximately 1milli-second and consistent from channel to channel. This is significantly better than the maximum 3 milli-seconds specified by the manufacturer of the relay.

Additional tests should be conducted once the entire electronics package has been assembled to control the Noise Prototype suspension at LASTI. These tests should include:

- A more sensitive test for glitches possibly using an optical cavity
- A test of the ability to coordinate the switching of a hardware mode switch with a software compensation filter. An optical cavity would also be useful during these tests.

4.4 Local Damping

This section of the test plan is not applicable and can only be conducted on a full quad suspension system.

4.5 Environmental

No environmental tests were conducted during the bench testing of the pre-production prototype. Testing at LASTI should include measurements of the sensitivity of the design to external acoustic and magnetic noise. An assessment of the grounding and shielding of the system should also be made.

Appendix A

Test Plan and Results

A copy of the completed test plan for the Pre-production PUM Driver can be found at:
http://www.ligo.caltech.edu/~jay/downloads/CompletedPUMTestPlan.pdf