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UK Top Driver Pre-Production Prototype Bench Test and Evaluation		
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1 Introduction

This tests report documents the bench test results and evaluation of the AdL Suspension Top Driver chassis supplied as a pre-production prototype by the University of Birmingham. Bench tests were conducted in accordance with LIGO document number T080014-00-C, “AdL UK Top Coil Driver Pre-Production Test Plan”. A link to the completed test plan with results is included in Appendix A of this document. The design requirements for the Top Driver can be found in LIGO document number T060067-00-C, “AdL Quad Suspension UK Coil Driver Design Requirements”.

The format of this report roughly follows the format of LIGO document T070288-00-C, “Adl Noise Prototype Electronics Test Plan”. The tests outlined in T0700288-00-C are a series of tests and evaluations that will be used to evaluate the full set of electronics provided by the University of Birmingham for the AdL Quad Suspension system. The major categories of the plan are:

- Manufacturing
- Operational
- Performance

This test report covers relevant portions corresponding to each of these categories.

2 Manufacturing

2.1 Quality of Manufacture

The Top Driver chassis provided to LIGO for testing and evaluation is a pre-production prototype and should be treated as such. Many of the comments and suggestions in this section relate to the prototype nature of the driver and should not be taken as criticism, but as general recommendations. The photos below are front and rear views of the Top Driver with the cover removed.

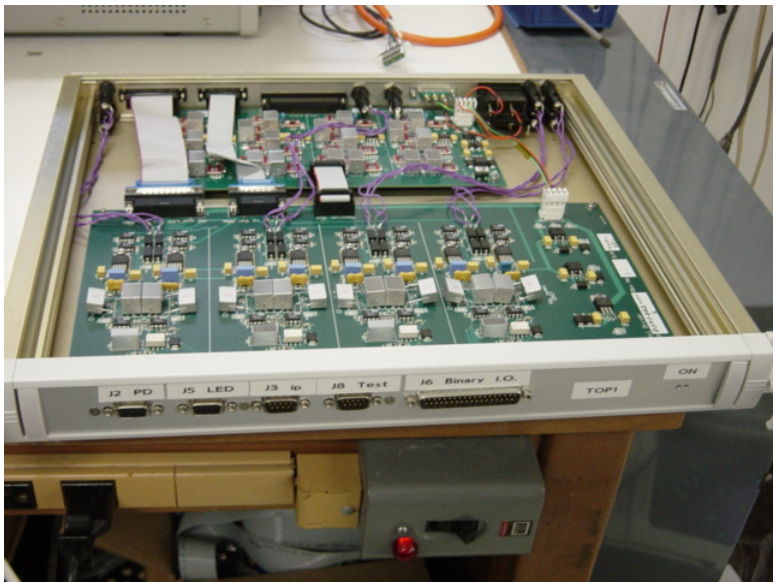

Figure 1: Top Driver Chassis Front View

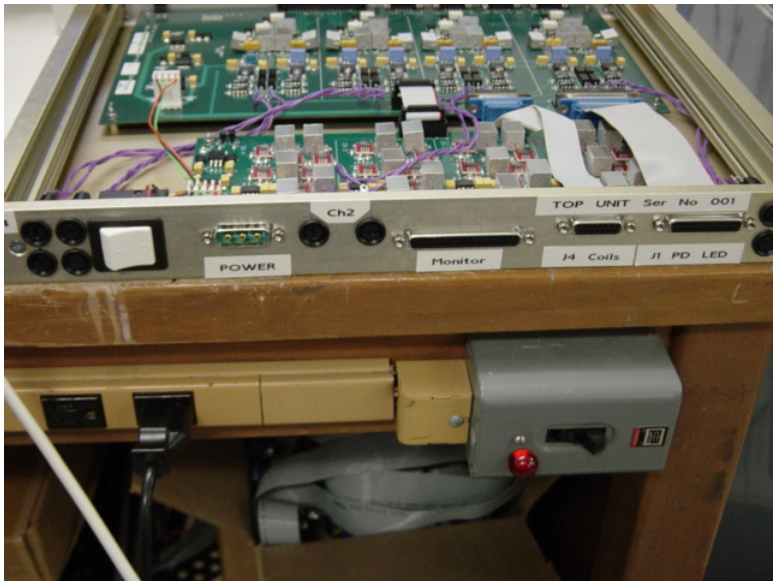

Figure 2: Top Driver Chassis Rear View

2.1.1 Chassis Labeling and Identification

As can be seen from the photos, front and rear panel labels have been made using a label maker. In the full production units these labels should be implemented in a more permanent manner such as engraving or permanent stenciling. The drawing number associated with the chassis assembly drawing should also be added to front or rear panel labels.

Power indicators are included on the front panel, but the power indicators for the monitor board are inside the chassis and there are no indicators on the rear panel. It would be advantageous if there were some indication of power status on the rear of the chassis near the power switch.

2.1.2 Circuit Boards

The photo below is a closer view of the Top Driver board. As can be seen from the picture, the circuit board is multi-layer, professionally manufactured circuit board. The larger silver objects running down the middle of the board are capacitors. Several of these capacitors are installed laying down because the footprint on the board was not correct for the component. This is expected in a pre-production prototype, but the footprints should be corrected prior to production. Additionally, the purple wiring leading from the driver board to the fuseholders mounted on the rear of the chassis is soldered directly into the board and the wires routed directly over and sometimes are in contact with the low noise circuitry of the rear mounted monitor board (see Monitor Board picture below). Prior to production wire attachment and routing and fuseholder placement should be rethought and if possible, the wires eliminated by using some type of board mounted fuseholder that protrudes from either the front or rear panel of the chassis. This could require a significant amount of board layout and chassis redesign. The board label on the silkscreen for the board also needs to be corrected. It incorrectly identifies the board as the UIM Coil Driver.

The Monitor board was manufactured in a similar fashion and the only circuit board issue observed was that the mounting hole size for the 37 pin sub D connector were not correct. This should be corrected prior to production. Both boards (driver and monitor) are identified in the space provided with the drawing number, revision number and serial number for the board. The circuit board (pcb artwork) revision number is included on the silkscreen for each board.

It can not be clearly seen in any of the included pictures, but each of the circuit boards (Driver and Monitor) have many test points that are clearly labeled. These test points are the same SMT style that has been used in many LIGO and AdL designs. Due to procurement problems, some of the test point components were not stuffed on the initial Top Driver, but it is assumed that production units will be fully populated. The only recommendation in this area would be to, if possible, include a few more ground test points located around the boards. These additional test points would aid in board test and debug.

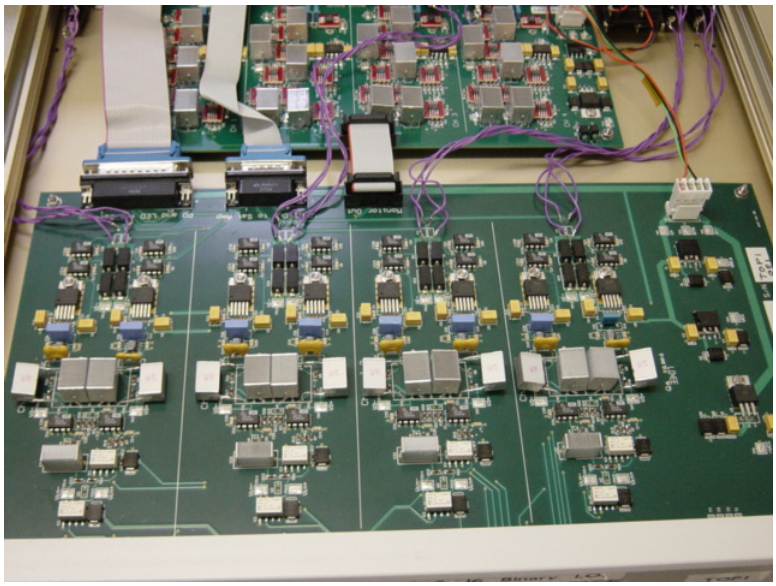

Figure 3: Top Driver Circuit Board

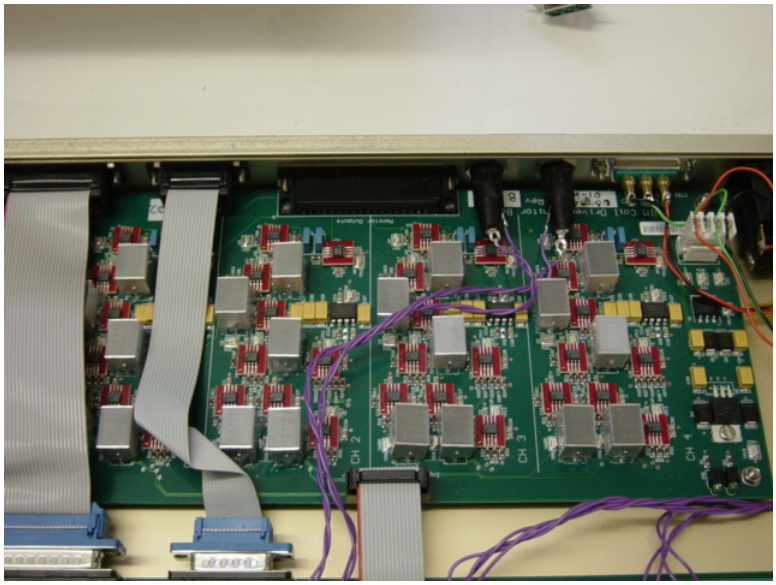

Figure 4: Top Driver Monitor Board

The Top Driver Board is capable of producing currents in excess of 200 mA per channel. The trace widths for these high currents paths appear to be 10-12 mils. Although this may be adequate, it is recommended that these widths be increased to a minimum of 25mils (0.635 mm).

2.1.3 Cabling, Connectors and Harnesses

The photo below is a closer view of the input power connections and chassis power wiring. As can be seen from the picture, the solder connections to the rear mounted power connectors are not adequate and wire colors used do not follow the LIGO power wiring color code. In this case, the positive voltage, return and negative voltage wire colors should be white, black and green, respectively. Heat shrink should be included over the power connector pins to prevent inadvertent shorting of the pins. Additionally, the Molex connectors used for connection to the header are the IDC style without the retaining clip installed. It is strongly recommended that these connectors be replaced with the crimp pin version.

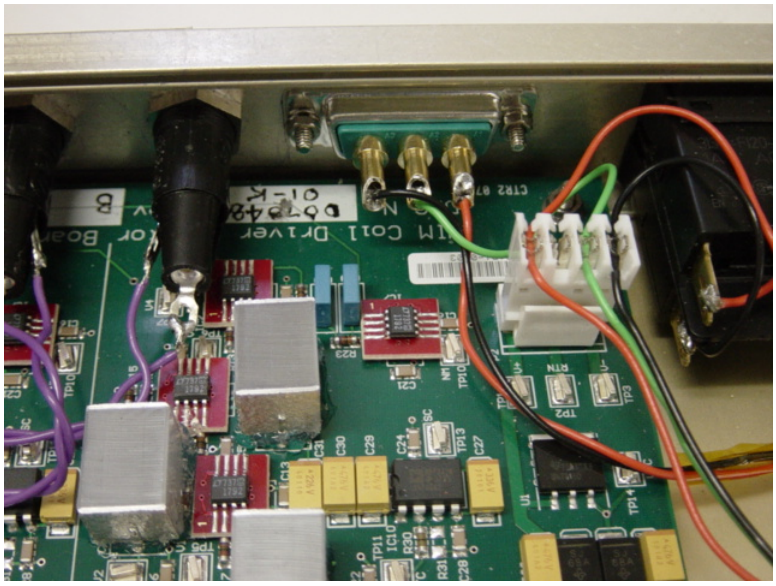

Figure 5: Close up of Top Driver Chassis Power Connections

The connectors used for incoming and outgoing field cables are sub D connectors. These connectors all have jack screws used for retaining the field cables and are acceptable for the production units. Some of the sub D connectors were not the threaded insert type and used nuts and lock washers to retain the jack screws. Threaded insert style sub D connectors should be used for the production units. Internal cabling, with the exception of the power wiring noted above, is either IDC sub D or keyed header/receptacle and is acceptable for the production units.

2.2 Serviceability

The chassis used for the prototype is a Metec chassis similar, if not identical to the chassis initially used for LIGO electronics. Experience with these chassis has shown that they are very difficult to work with and subject to breakage when removing the top and bottom covers. It is strongly recommended that these chassis be replaced with a chassis that has a more easily removable top cover. If possible, it would be preferred if the LIGO chassis available from Hamilton Metalcraft Inc. were used. These chassis are readily available to both US and UK customers.

After the Top Driver and Monitor boards had been designed, it was discovered that the 8 pin DIP package of the AD743 op amp was no longer in production and that there was no direct replacement available. These components were replaced with an SOIC version of the LT1792 mounted to an SOIC to DIP converter. These are the red components seen in some of the board pictures. Prior to production, the Driver and Monitor boards will need to be redesigned so that the converters are not necessary.

Although a complete bill of materials was not provided, a check of the availability of the capacitors used in the critical portions of the circuit showed that they may not be readily available in the US. If this is the case, then an adequate number of spares need to be provided with the production units. The same can be said of any other components used in the designs. This possibility will need to be evaluated when a complete set of documentation is supplied.

The layout of the boards in the chassis, and positioning of the connectors and fuseholders does not allow for easy removal or access to some of the components on the boards. Some thought should be given to this prior to producing the production units.

The AD634 buffers used in the design for the high current output drivers appear to be tied to a heatsink bar or other material under the board. If this is the case and there are any special mounting requirements such as thermal washer, special screws, heat sink compound, etc. then these materials and the assembly/disassembly procedure for the unit need to be described in the documentation provided.

2.3 Adequacy of Documentation

An incomplete set of schematics was provided with the pre-production units. No bill of materials, test plans, test results, quick start guide or other documentation was provided. Prior to production all materials listed in Electronics Requirements document (T060067) and LIGO document T000053-04-D, "Universal Suspension Subsystem Design Requirements Document" need to be evaluated.

3 Operational

3.1 Interfaces

The interfaces (connector types, pinouts, signal levels) between the University of Birmingham electronics and the AdL Electronics appear to be in compliance with Universal Design Requirements document (T000053).

3.2 Test Inputs and Monitoring

The design of the Top Driver includes test inputs for each channel. These test inputs are connected to the input and can be enabled or disabled via an external control signal or a local board connection. When the test input is connected, the input from the control system is disconnected and visa versa. The use of the normally closed contact for the test input allows this relay to be used as a fail-safe enable/disable for the control input. The second set of contacts for these relays and for all relays used in the design provide a separate read back of the actual relay position in accordance with the requirements. One observation worthy of mentioning is that when link W2 is left open and the test input switch in the normally closed position, there is no bias return path for op amps IC2 and IC6. This leads to amplifier offsets and drifts that may not be acceptable in AdL. It is recommended that W2 be installed or bias return resistors added to the inputs.
Other monitors included in the design and in accordance with the requirements are:

- Low noise monitor of the driver output
- Fast output current monitor
- RMS current monitor

These appear to be adequate for use in AdL.

There was a discrepancy between the predicted and measured values for the voltage, fast current and RMS current monitors for the chassis (Section 3.5.3 of the test plan). The actual monitors appear to have a lower than expected value. This could be due to a difference in the assumed component values used for the simulation and the actual component values used on the board. Once a schematic for the monitor board used in the chassis is provided, the units should be retested. In addition, the value for several other inputs should be tested in an effort to make sure the monitors are linear. This should be checked and fixed, if necessary, by the University of Birmingham prior to production.

3.3 Long Term Reliability and Stability

The tests conducted on the Top Driver took place over a two week time frame where the unit was intermittently powered and turned off for testing. While no failures or stability issues were observed, this time period is inadequate to determine if there are any long term reliability or stability issues. Additionally, no overheating or heat management issues were observed. Noise Prototype testing at LASTI should last for many months and may provide addition information in this category.

4 Performance

Performance of the chassis was measured using the set of tests outlined in LIGO document T080014-00-C. The completed report is included in Appendix A. The sections below summarize the tests results.

4.1 Noise and Dynamic Range

4.1.1 Driver Noise

The noise requirements for the low noise mode of operation are outlined in T060067. For convenience the summary table from T060067 is repeated below.

Frequency	**Current Noise Requirement**
1 Hz	1 nA/√Hz
10 Hz	73 pA/√Hz
100 Hz	1000 nA/√Hz
1000 Hz	1000 nA/√Hz

Note that the requirements are given in units of current spectral density. Measuring current noise directly is very difficult so the tests performed measured the output voltage noise of the driver and the current noise inferred by dividing by the load impedance at the frequency of interest. Assuming a 20 ohm coil load and the particular design chosen by the University of Birmingham the noise requirements in terms of output voltage noise can be calculated for each of the frequencies in the table. These voltage noise requirements are shown in the table below.

Frequency	**Voltage Noise Requirement**
1 Hz	108 nV/√Hz
10 Hz	7.9 nV/√Hz
100 Hz	108 uV/√Hz
1000 Hz	108 uV/√Hz

The plot below shows the measured and simulated output noise versus frequency for the Top Driver. The simulated noise data was generated using Altium Designer 6.

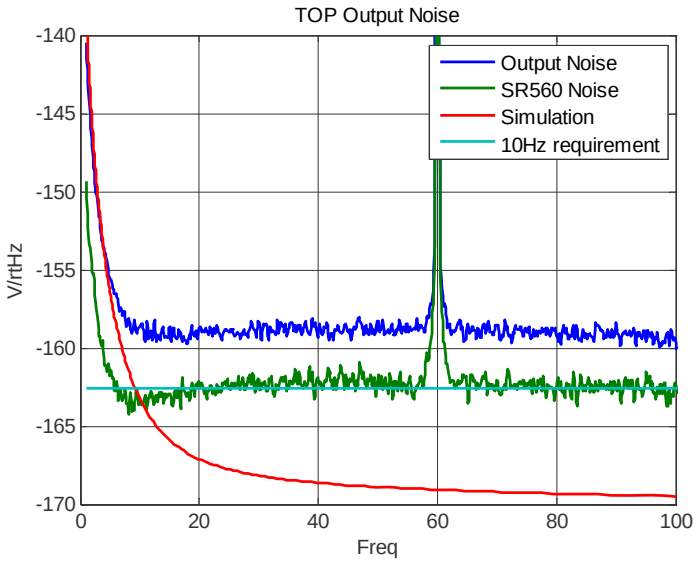

Figure 6: Measured and Simulated Top Driver Output Noise

Note that the simulation predicts that the design submitted by the University of Birmingham should meet the requirements. The measured noise (blue) is approximately 3 dB higher than the requirement, but the noise floor of the SR560 amplifier used during the test falls right on the 10Hz requirement line. Assuming that noise of the SR560 and the Top Driver are not correlated and add in quadrature, this would imply that the Top Driver noise is equal to the SR560 noise and therefore meets the 10Hz requirement. The driver noise is below the requirements at the other frequencies.

During testing it was noticed that installing link W1 and W2 seemed to relieve an oscillation seen before capacitors C100 and C101 were installed. It is recommended that this oscillation be investigated to determine if it has been eliminated completely and is not causing additional noise when large voltages are present. This can be checked by applying a large, low noise DC voltage to the driver inputs and repeating the output noise measurements in section 3.2 of the test plan.

4.1.2 Monitor Noise

One of the requirements for monitors on the Top driver is a noise monitor capable of "seeing" output referred noise voltage of the driver at 10Hz (hardest requirement) in the low noise mode of operation. In an effort to do this, the University of Birmingham has designed a noise monitor that is a high gain AC coupled differential amplifier tied to the voltage output legs of the driver. The output referred noise of the driver at 10Hz should be less than 8nV/√Hz. This was tested, confirmed and described in the section above. A simulation of the noise monitor circuit coupled to the driver circuit shows that the input-referred noise voltage of the monitor, where the input is defined as the output legs of the driver, is approximately 17.5nV/√Hz at 10Hz. The figure below is a plot of the output referred noise of the monitor simply divided by the gain of the monitor at 10Hz (42.4dB). Note that this plot is only valid at 10Hz. For example, the gain at 100Hz is 46dB so the monitor noise voltage at 100Hz is really 3.6dB lower than what is shown in the plot.

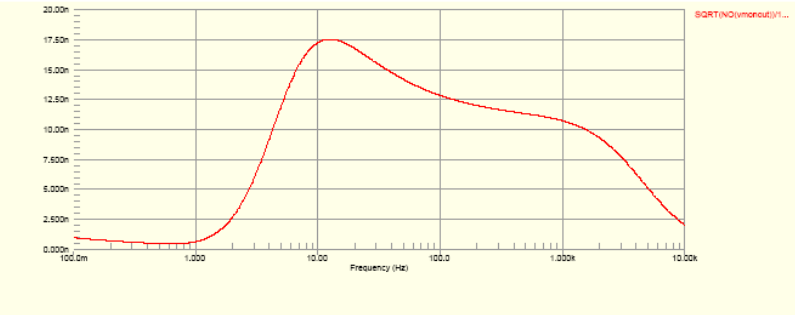

Figure 7: Noise Monitor Noise Referred to Driver Output

The tests results in section 3.5.2 of the test plan appear to confirm the simulation. If the simulation is correct and the requirement is a "firm" requirement, then the noise monitor circuit will need to be redesigned such that the input-referred noise of the noise monitor circuit is below 8nV/√Hz. Note that the input of the noise monitor is defined as the point that ties to the output legs of the driver circuit.

4.1.3 Dynamic Range

The dynamic range requirement for the Top Driver is +/-200 mA at DC. The dynamic range of the driver was tested in section 3.1.3 of the test plan. In these tests a load resistor of 20 ohms was used. The current output versus voltage input appears to be approximately 10% lower than the circuit diagram would suggest for a 20 ohm load. This may be due to component tolerances, but the source should be identified. In actuality, the OSEM coil impedance is closer to 40 ohms. If this value is used, then the simulation predicts that the output current will be 195mA for a 20V input, just slightly short of the requirement. When the unit was tested using a 40 ohm load resistor, the actual output current for a 20V input was 175mA. Again about 10% below expected.

4.1.4 Transfer Function Measurements

4.1.4.1 Driver Transfer Function

The transfer function of the Top driver from input to current output was measured and compared to the Altium simulation. The figure below shows the simulated and actual transfer function for one channel in the low noise mode.

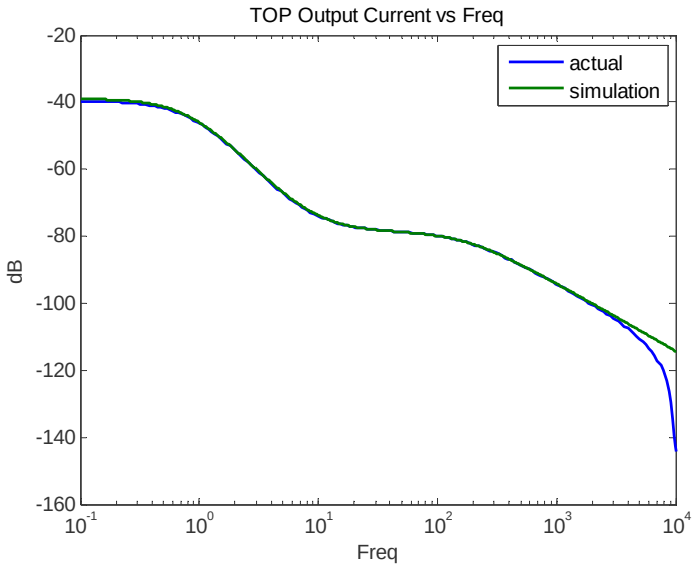

Figure 8: Simulated and Actual Transfer Function

Note that the traces agree very well. The deviation at high frequencies is due to the roll off of the AA filter used as a differential driver for the chassis. Close examination of the data taken and recorded in the test plan shows that the actual measurements are consistently 0.7dB lower than predicted for low frequencies. This is similar to the 10% deviation seen in the dynamic range tests.

4.1.4.2 Noise Monitor Transfer Function

The transfer function from the input of the driver to the output of the noise monitor circuit was measured in section 3.5.1 of the test plan. A plot of the expected transfer function is shown in the figure below.

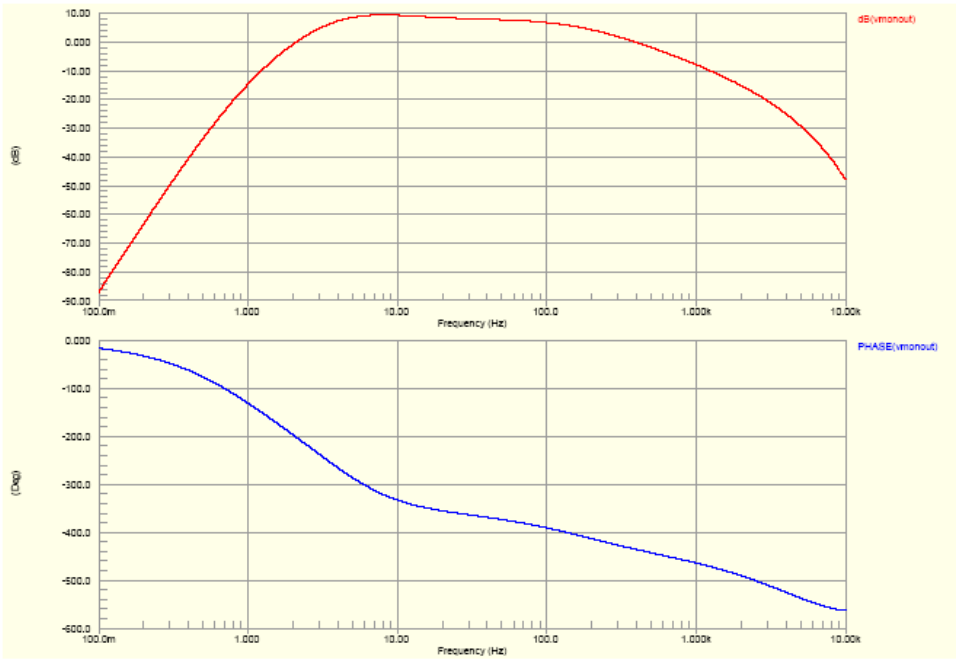

Figure 9: Noise Monitor Transfer Function, Measured from Driver Input to Monitor Output

The measured transfer functions for all four channels were found to be in close agreement with the Altium simulation.

4.2 Cross-Coupling

The cross coupling from one channel input to the output of the other channels on the driver board was measured using the procedure in section 3.3 of the test plan. The plot below shows the typical coupling observed from the input of one channel to noise monitor output of another channel on the board.

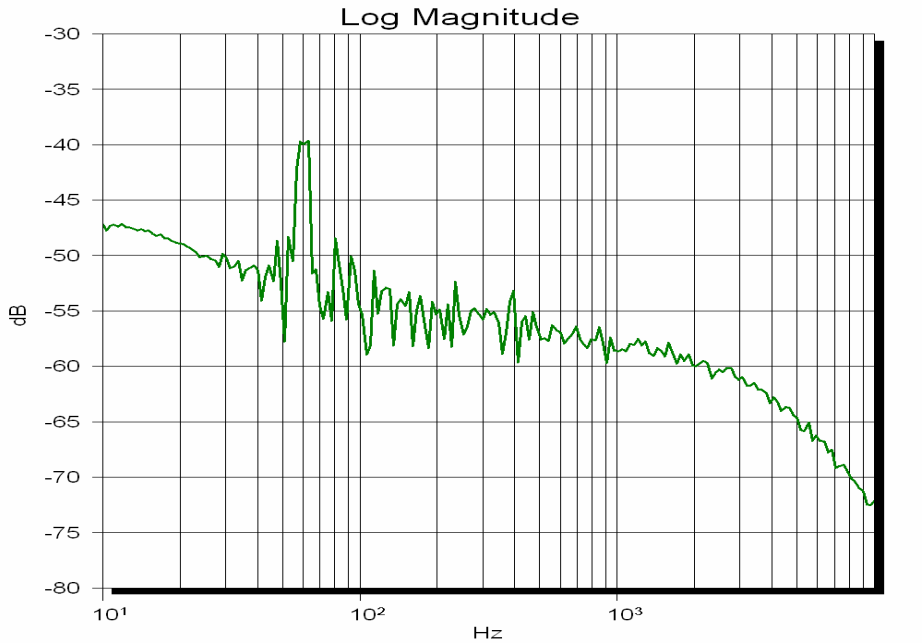

Figure 10: Typical Cross Coupling Measurement Results

As can be seen from the plot, the highest coupling measured was approximately -47dB at 10Hz. The gain of the noise monitor at 10Hz is 42dB. This leads to an isolation of approximately 89dB from the input of one channel to the output voltage of another channel on the board. This should be acceptable for AdL. Note that the peak see at 60Hz is most likely a line harmonic, not cross-coupling and was therefore ignored.

4.3 Mode Switching and Glitch Tests

The design of the Top Driver provides for one relay that can be used to switch each channel from what can be called “acquire” mode to a lower noise “run” mode. The design is such that the relay can be switched using either a set of contacts or an open-collector output from the US provided control system. The design also uses another set of contacts from the mode switch relay (K3) to monitor the relay position. The design meets the requirements called out in the Suspension Universal Design Requirements document (T000053).

An attempt was made to measure any glitches or transients in the current output of the driver caused by the switching of relay K3. These tests are described and the results documented in section 3.4 of the test plan. During the tests no glitches or transients were observed. The switching time of the relays used on the board was found to be approximately 1milli-second and consistent from channel to channel. This is significantly better than the maximum 3 milli-seconds specified by the manufacturer of the relay.

Additional tests should be conducted once the entire electronics package has been assembled to control the Noise Prototype suspension at LASTI. These tests should include:

- A more sensitive test for glitches possibly using an optical cavity

- A test of the ability to coordinate the switching of a hardware mode switch with a software compensation filter. An optical cavity would also be useful during these tests.

4.4 Local Damping

This section of the test plan is not applicable and can only be conducted on a full quad suspension system.

4.5 Environmental

No environmental tests were conducted during the bench testing of the pre-production prototype. Testing at LASTI should include measurements of the sensitivity of the design to external acoustic and magnetic noise. An assessment of the grounding and shielding of the system should also be made.

Appendix A

Test Plan and Results

A copy of the completed test plan for the Pre-production Top Driver can be found at:
http://www.ligo.caltech.edu/~jay/downloads/CompletedTopTestPlan.pdf