Tip/Tilt Driver -Quick Start Guide
LIGO- T060253-00-C
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20 October, 2006

Hardware Revision Applicability – Rev. A1

1. Overview

1.1. The Tip/tilt driver chassis (LIGO-D060287) provides the high voltage (0 to 150V) drive and monitoring functions for two separate piezo positioning stages. Each stage has two axes for a total of 4 independent axes of control. **This chassis contains potentially lethal voltages. Extreme care must be used.**

1.2. Each axis of the piezo drive can be modulated for dither locking at frequencies from 2 to 20 kHz. Dither modulation can be applied from a DAC (Digital to Analog) interface, or from a front panel BNC.

1.3. Each axis has separate piezo voltage monitors. As a single axis requires two high voltage amplifiers, there are a total of 8 high voltage amplifiers in the chassis. Each high voltage amplifier has a separate voltage monitor.

1.4. Monitoring is provided for a strain-gage on each axis. The chassis provides the needed excitation and differential readback of measured strain.

2. Electrical Interfaces

2.1. All **front panel inputs** are true-differential, bipolar +/- 10 volt range. The input impedance is 10k ohms on all inputs. Inputs voltages should be limited to +/- 15 volts to avoid damage.

2.2. All **DAC outputs** are fully differential +/- 10 volt range. Load impedances should be greater than 1k ohm.

2.3. The required **low voltage power supply** is nominally +/- 18 VDC @ 0.5 amps. A range of voltages from +/-16 to +/- 19 is acceptable.

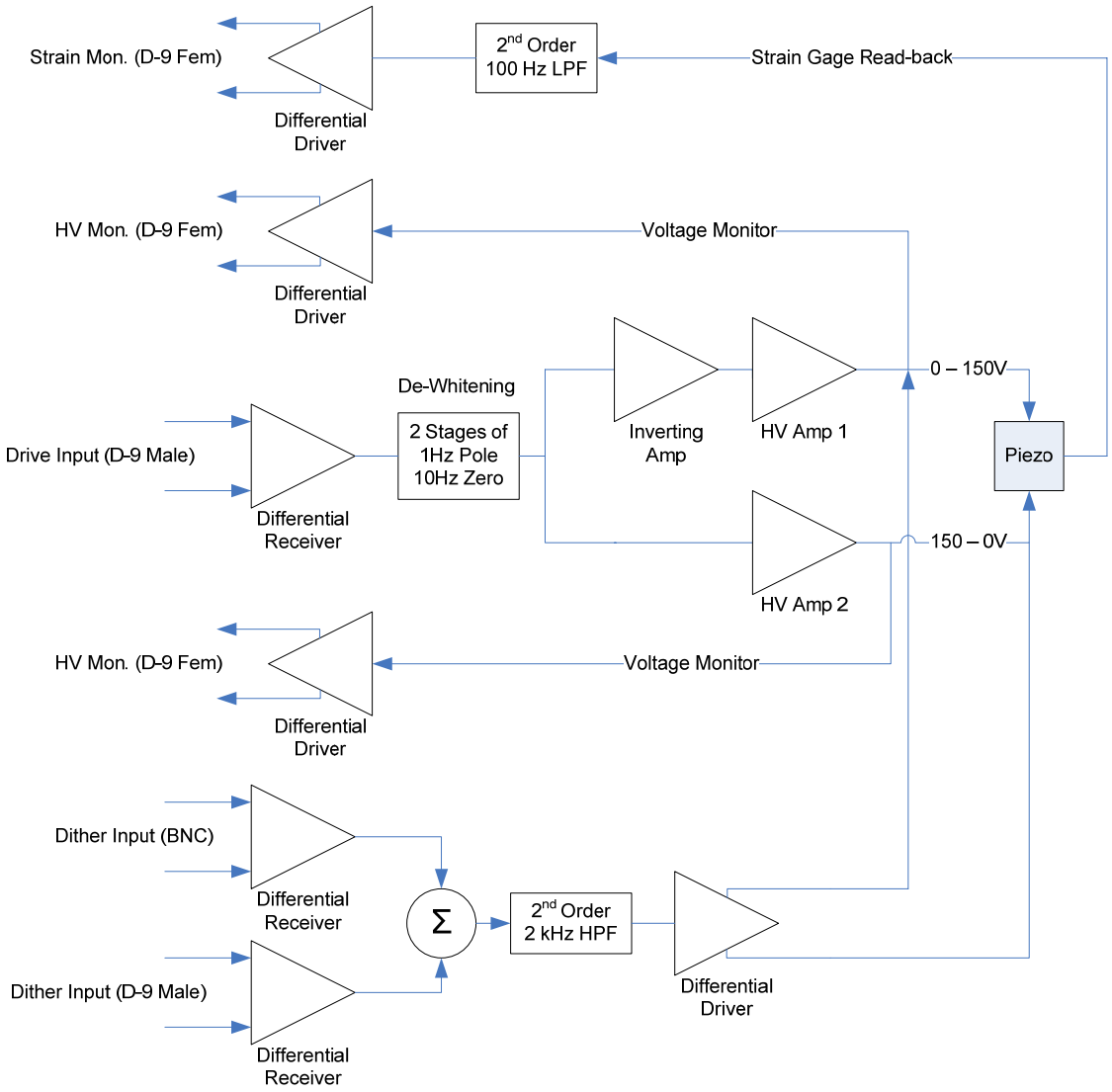
2.4. The required **high voltage power supply** is 150 VDC +/- 5% with a current capacity of at least 20mA.

2.5. The nominal **piezo load capacity** is 1uF +/- 20%

2.6. Detailed **electrical schematics** are available in LIGO document D060287

3. **Figure 1** shows an overview of one axis

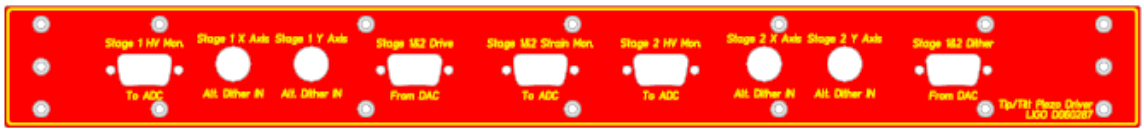
Figure 1



4. Figure 2 and Figure 3 show the front and rear of the Tip/tilt driver chassis. A functional description of each connector is provided.

4.1. **Front Panel diagram**

Figure 2, Front Panel



4.2. Front Panel Functions

4.2.1. **Stage 1 (2) HV Mon** – Monitoring for each high voltage output. 1V at monitor is 15V at the HV output. No internal filtering of signal.

4.2.2. **Alt. Dither IN** – A BNC input providing an alternate path for injecting a 2 kHz to 20 kHz modulation signal used to dither-lock a particular axis. Path includes a second order, 2 kHz high-pass filter.

Drive Frequency	Maximum Peak-to-peak Input Voltage	Output across 1uF Piezo
5 kHz	20 Vp-p	900 mVp-p
10 kHz	20 Vp-p	900 mVp-p
20 kHz	12 Vp-p	520 mVp-p

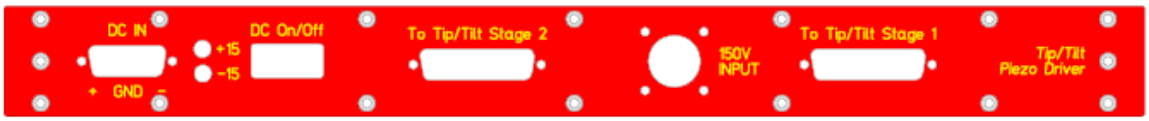
4.2.3. **Stage 1&2 Drive** – A D-9, male input for differential voltage drive to each axis. Normally fed by a DAC output. A 1 volt signal at this input changes the voltage across the piezo by 20 volts. The quiescent output voltage of each complimentary drive rests at 75V +/-5% when there is no input (0V). A de-whitening filter consisting of 2 poles at 1 Hz and 2 zeros at 10 Hz is included in this path. The current at each HV output is limited internally to 6.7mA +/- 5%, and is short-circuit-protected.

4.2.4. **Strain Mon** – D-9, female voltage monitor of each piezo's integral strain gage. Path includes a second order 100 Hz filter for noise reduction, and an amplifier with a gain of 2. 1 volt at the monitor corresponds to 0.5 volts of strain-gage output.

4.2.5. **Stage 1&2 Dither** – This input has the same electrical characteristics as section 4.2.2 (BNC Dither Input). This input is designed to be interfaced to a DAC, and provides interface to all 4 axes of dither capability

4.3. **Rear Panel Diagram**

Figure 3, Rear Panel



4.4. Rear Panel Functions

4.4.1. **DC IN** – A three terminal input in a D-15 shell. This input supplies the DC power to the chassis. The nominal input is +/- 18 VDC @ 0.5 amps, but a range from +/- 16 to +/- 19 VDC is acceptable. This range allows sufficient overhead for the internal low-dropout regulators, but is not so high as to cause a thermal dissipation issue with the regulators.

4.4.2. **+15 & -15 volt LEDs** – When lit, indicate the presence of DC power at the output of the internal regulator board. The power regulator has Poly-fuses that are rated at 2 amps. Cycling power to the chassis via the DC On/Off switch will reset the Poly-fuse provided the fault condition is clear

4.4.3. **DC On/Off** – Switch to turn power on and off. Switch removes power from the input of the power regulator board.

4.4.4. **Tip/Tilt Stage 1 (2)** – D-25, female connector providing interface to one dual axis Tip/Tilt stage. ***Potentially lethal high voltages (150VDC) are present on this connector***. Extreme care must be employed when working with this connection.

4.4.5. **150V Input** – This is the high voltage power supply input to the chassis. 150 VDC @ 20 mA is required.