LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

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Shutter Timing Module Test Procedure

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1 Overview

The following procedure refers to D050214-A, the ASPD Shutter Timing Module. The photodetectors on the anti-symmetric port of the interferometer are protected from high optical power pulses associated with loss of arm cavity lock by a mechanical shutter. The mechanical shutter is triggered to close once the detected light levels exceed a predetermined threshold. The ASPD Shutter Timing Module measures the time taken for a mechanical shutter to close relative to the trigger signal.

Details of the Shutter Timing Module theory of operation can be found in document T050106-00-C

1.1 Test Equipment

The following test equipment is necessary:

Dual DC power supply (capable of ± 24VDC)
Shutter Timing Module test pulse generator board
Scope with scope probe
Function Generator (DS345)
25 pin D connector breakout for applying power and reading output voltages
Multimeter

1.2 Test Setup

Connect DC power supply that has been previously adjusted to ± 24VDC.

25 PIN D-SUB CONNECTOR PIN	FUNCTION
Pin 1 and 2	+24VDC
Pin 3 and 4	-24VDC
Pin 14 through 25 inclusive	Ground

1.3 Test Overview

The test procedure is divided into the following sections:

- DC power supply checks
- Trigger threshold adjustment potentiometer verification
- Signal continuity check by application of sine wave stimulus
- On-board clock divider verification
- DAC output verification
- Timing Operation Verification

1.4 DC Power Supply Checks

Turn on the power supply and record the following data in Table 1 and Table 2.

Table 1

Supply	Nominal Current	Actual Current	Check if OK
-24 V	150 mA (± 20 mA)		
+24 V	120 mA (± 20 mA)		

Table 2

Test Point	Nominal Voltage	Actual Voltage	Check if OK
TP1	15VDC (± 100 mV)		
TP2	-15VDC (± 100 mV)		
TP9	5VDC (± 100 mV)		

1.5 On-board Clock Divider Verification

Using the shorting jumper on JP1, verify that each position produces the required clock division ratio as viewed with an oscilloscope at TP22 per Table 3

Table 3

JP1 Jumper Setting	Measurement point	Requirement	Check if OK
1-2	TP22	10.0 MHz (±2kHz)	
3-4	TP22	5.0 MHz (±2kHz)	
5-6	TP22	2.5 MHz (±2kHz)	
7-8	TP22	1.25 MHz (±2kHz)	

- ❑ Check box to verify that the shorting jumper on JP1 is left in the “7-8” position

1.6 Trigger Threshold Potentiometer Verification

While observing the voltage using a Multimeter at the indicated monitoring points, adjust each potentiometer in accordance with the instructions in Table 4.

Table 4

Potentiometer to adjust	Measurement point	Requirement	Check if OK
R12, One extreme to the other	Front Panel BNC J6	± 14 VDC (± 1 V tolerance)	
R12	Front Panel BNC J6	0 VDC (± 50mV)	
R13, One extreme to the other	Front Panel BNC J7	± 14 VDC (± 1 V tolerance)	
R13	Front Panel BNC J7	0 VDC (± 50mV)	

1.7 Signal continuity check by application of sine wave stimulus

Using the signal generator create a 1kHz, 10Vpp sine wave and carefully verify that the applied signal is indeed what you think, (this because some generators have displayed numbers that assume a certain load impedance, therefore it's best to check this assumption with a scope to be sure). Sequentially apply the signal to the front panel inputs J1, J2, J3, J4, and J5 BNC connectors while monitoring each channels respective monitoring points. In the interest of time, toggle the polarity inversion switch associated with each channel while observing the square wave signals to verify operation of the polarity inversion switch.

- ❑ Set R12 and R13 to 0VDC.

Table 5

Input 1kHz, 10Vpp Sine Wave	10Vpp ± 100mV Sine Wave TP17	0-5V ± 100mV Square Wave TP18	Phase Flip OK	Check if OK
J1				
Input	TP13_X	TP14_X	Phase Flip OK	Check if OK
J2				
J3				
J4				
J5				

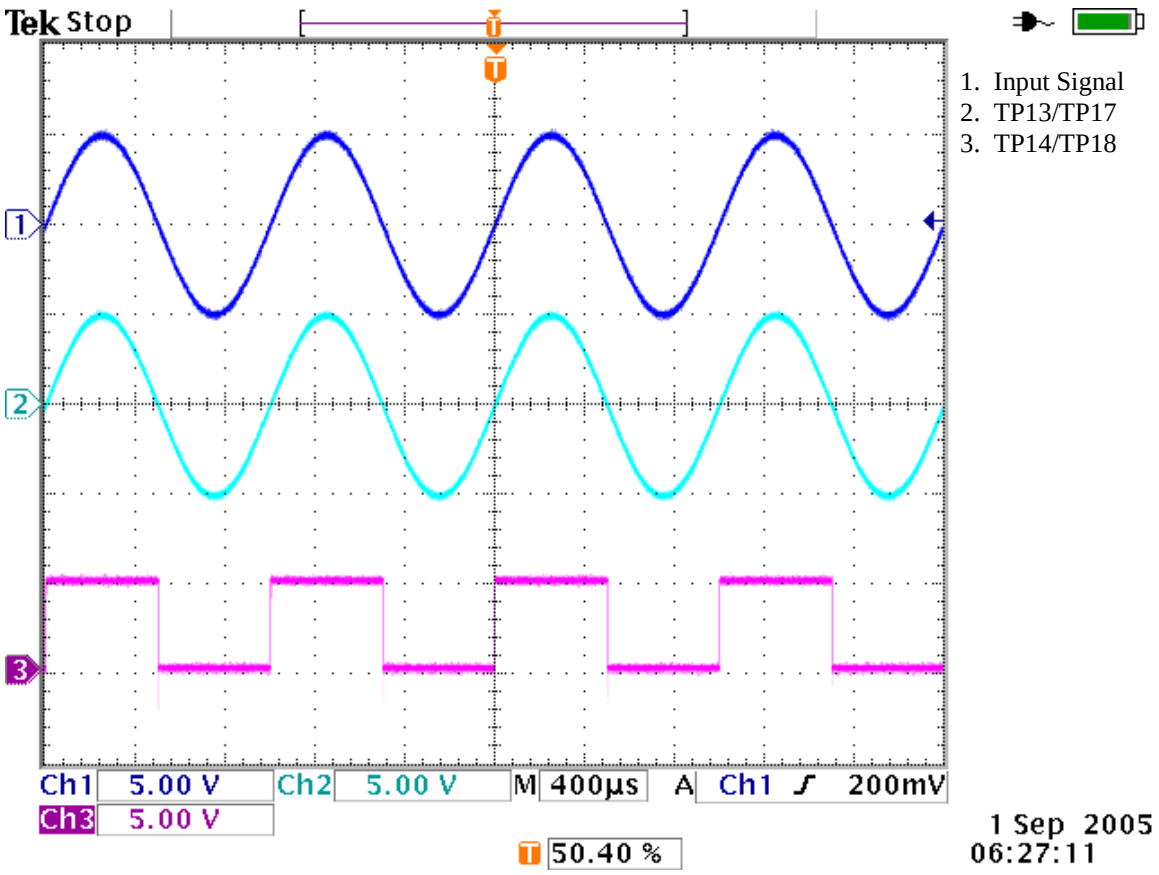

Figure 1

1.8 DAC Output Verification

Apply a 5Vp-p, 1Hz square wave into front panel BNC J1. Verify waveforms as indicated in Table 6 and Figure 2 using an oscilloscope

- ❑ Set R12 to 0 VDC and R13 to 2.5VDC. Set all switches to the down position.

Table 6

Measurement Point	Requirement	Measured Volts p-p	Check if OK
TP15_1	20Vp-p, ± 100mV		
TP15_2	20Vp-p, ± 100m V		
TP15_3	20Vp-p, ± 100m V		
TP15_4	20Vp-p, ± 100m V		

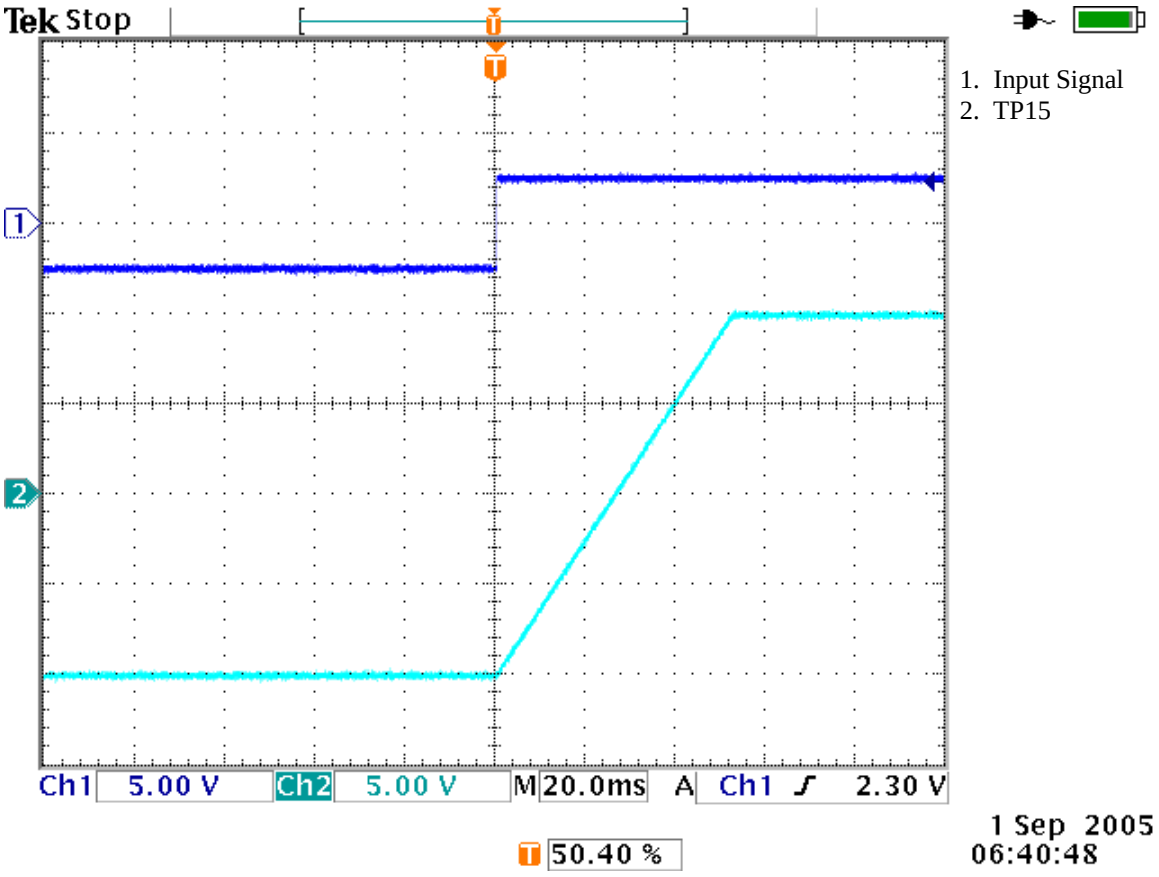

Figure 2

1.9 Timing Operation Verification

Use D050340, the Shutter Timer Tester Board, to generate a 40ms pulse on Out 1 and a 80ms pulse on Out 2 as shown below. A 1Hz, 0-5V square wave should be used as the input for the tester board. Connect Out 1 and Out 2 to J1 and J2 respectively of the board being tested and measure the response using a 25 pin breakout cable. Verify the response matches the traces shown in Figure 3 and record the peak voltage with respect to ground in Table 7, then repeat for channels 2, 3, and 4 (Out 1 remains connected to J1 for all tests). TP16_X may be used for monitoring the output, however it is strongly preferred that a breakout cable be used for a complete end-to-end test.

- ❑ Set R12 and R13 to 2.5VDC. Set all switches to the up position.

Table 7

Input	Measurement Point	Requirement	Measured Volts	Check if OK
J2	Breakout cable channel 1 (TP16_1)	+5.2VDC, ± 100mV		
J3	Breakout cable channel 2 (TP16_2)	+5.2VDC, ± 100mV		
J4	Breakout cable channel 3 (TP16_3)	+5.2VDC, ± 100mV		
J5	Breakout cable channel 4 (TP16_4)	+5.2VDC, ± 100mV		

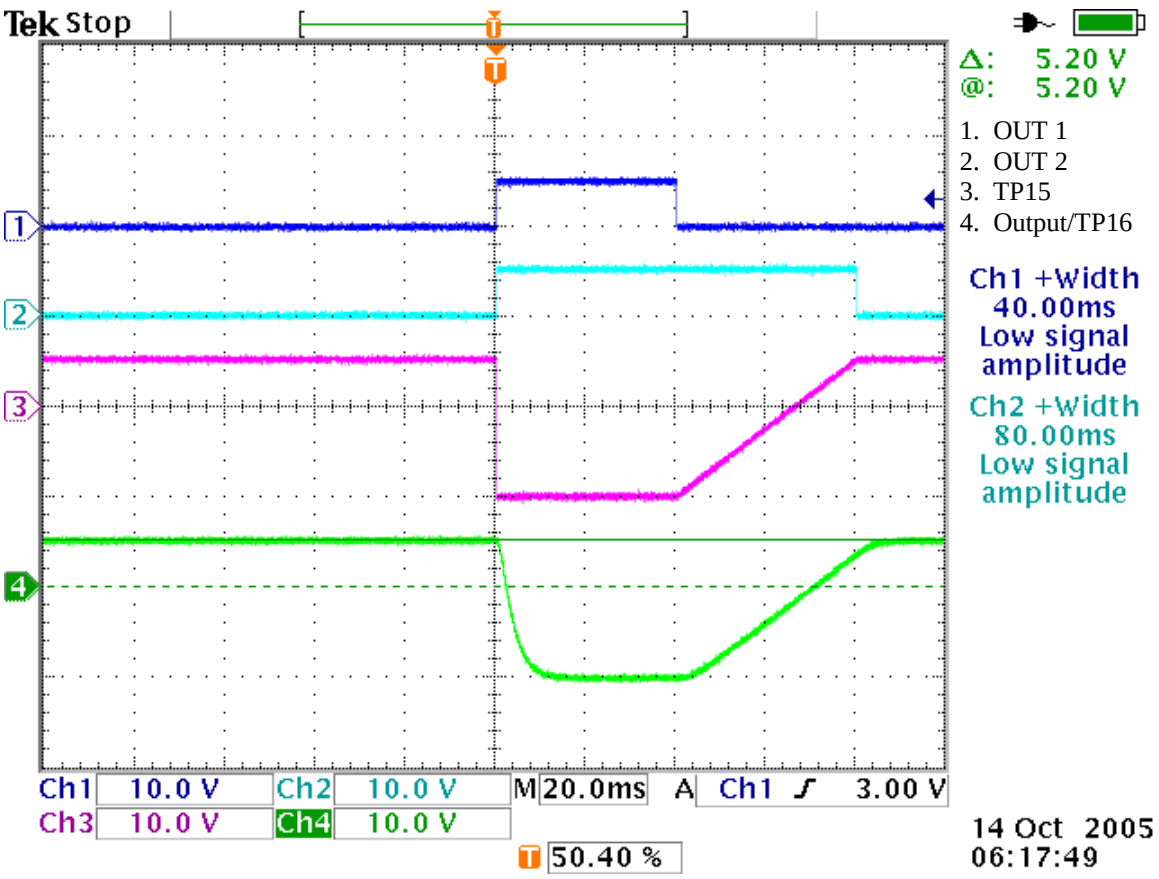

Figure 3