**LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY**

*LIGO Laboratory / LIGO Scientific Collaboration*

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# Retrospective Analysis of Testing Failure, ISS#115

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# 1 Introduction

ISS circuit board; SN115 was shipped in mid July 2005 to Livingston as a replacement for the installed circuit board. Prior to shipment, unit was tested in accordance with the test procedure (LIGO-T030184-00-C). Upon receipt at Livingston the unit was again tested and problems were found. The unit was shipped back to CIT for analysis and re-testing. The procedure used to test this board has been reviewed and the mistakes made during testing have been incorporated into lessons learned.

# 2 Summary of Deficiencies and Observations

During testing at LLO, and after the unit was returned to Caltech, the following were noted:

1. A resistor (R62) used in the main servo signal path was not re-installed on the board after being removed as part of the test procedure
2. The outer loop analog excitation input op-amp (U57) was oscillating at 22 MHz due to the compensation capacitor (C202) not being installed
3. The inner loop servo transfer function calls for a pole at 80 Hz. A measurement performed at LLO measured this pole at 40 Hz
4. Numerous components labeled “TBD” are not installed on the board creating an environment conducive to uncertainty
5. The test procedure does not appear to be approved in any formal sense
6. Inner loop servo transfer function taken on the electronics shows peaking around 4 MHz
7. During testing at LLO, a THS4151 differential driver chip (U22) was damaged and replaced with a THS4131 differential driver chip
8. A 100pF chip capacitor was added in place of TBD components to compensate AD-829 stages. C107, C226, C223, C224, C105, C121, C202, C83, C108, C93, C109, C89
9. Outer loop “Test Out Ch2” AD-829 driver op-amp’s compensation capacitor (C108) was incorrectly installed as a 3k ohm resistor, the part was nominally designate “TBD” and is designated to receive a capacitor

# 3 Analysis and Resolutions for Discrepancies and Observations

In response to the observations made at LLO and Caltech, the following outlines the suggested response and lessons learned in a case-by-case fashion referring to the items listed above

1. The missing resistor, R62, was caused by an error in the test procedure. The procedure calls for removing this resistor during testing and never explicitly requires its replacement. Human error was allowed to enter the testing by this omission. This error is corrected by a modification to the test procedure. In general, it is not satisfactory to remove a component from a finished assembly in order to accomplish testing. Effort will be made to see if the same testing functionality can be accomplished without component removal
2. The 22 MHz oscillation on U57 stage was due to a missing compensation capacitor. This stage is part of the outer loop feedback path, which, to date, has never been implemented at

the observatories. There are numerous components on the board that provide hooks to activate this feature, but more system testing is required to establish the correct values. This problem has been addressed by the following actions:

a. Compensation for U57 will be achieved by the addition of a 47pF capacitor in place of C202

b. The test procedure will be modified to include spectral analysis above 100 kHz to check for out-of-band circuit oscillations. Feedback has been given to those involved in testing to make them aware of this pitfall for all designs

c. A DCN is being written that outlines a stable configuration for all of the outer loop components awaiting more suitable component values as determined by system testing

d. Checking for out-of-band oscillations will be added to all future test procedures as a standard test

3. The 80 Hz pole and associated zero at DC are implemented by an RC network consisting of a 1uF series capacitor (C25) and a 2k-ohm shunt resistor (R23). An observation was made that the pole was erroneously at 40 Hz. It was suggested that the component values be checked by removal and direct measurement. Measurement of the components revealed that they were the correct value. Upon replacement of these components, a follow-up measurement showed that the pole was at 80 Hz. The best explanation available here is measurement error because in order to shift the pole by a factor of 2, and preserve the zero at DC, a component value would have to change. It's unlikely that re-soldering could cause the resistor value to change from 2k to 4k or the capacitance to change from 1uF to 2uF.

4. The components on this design that were labeled TBD are being edited to read, "Omit" or to have an appropriate value assigned. Those components associated with the yet unused "Outer Loop" functions have been chosen to prevent any misbehavior. In cases where components can safely be omitted, this is the chosen option to allow easy rework should we choose to activate this function at a later date. The parts lists associated with this design will be appropriately amended

5. The uncertainty in administrative approval for the ISS test procedure is more far reaching. It is not likely that an administrative approval process would have caught the type of errors or omissions present in this design. As a minimum, a test procedure should probably be marked in some fashion to indicate it is an approved procedure and include the names of the reviewer(s). This will be a topic for ongoing debate.

6. The observation of 4 MHz peaking in the main servo path amplitude response was investigated. An analysis of the designer's poles and zeros shows a zero at 806 kHz, and a pole at 3.35 MHz as part of the nominal design. These functions are realized in the U13 stage of the servo amplifier chain. The system block diagram does not reflect this design choice and will be modified to better document this. The function of this pole-zero pair is to compensate the PMC pole included in the overall open loop transfer function

7. The cause of the damage that occurred during testing at LLO to the THS4151 (U22) differential driver chip is unknown. The chip was replaced with a THS4131 differential driver. The replacement chip has lower noise, but a lower slew rate. At this plane in the ISS servo (this is the output driver to the current shunt), the demands of slew rate are

highest. For this reason, a THS4151 will be used again. Institutionally, we must avoid the temptation to make substitutions that are not reviewed or documented based on schedule pressure. This practice can easily lead to extremely labor intensive trouble-shooting efforts that require boards be physically removed from the system. The DCN and review process is needed for all changes to a design

8. The addition of 100pF chip capacitors to replace the "TBD" values used on the board will be documented in a DCN. A review of the datasheet for the associated op-amp (AD-829) reveals that the maximum compensation capacitor recommended by the manufacturer is 68pF for the "voltage follower" configuration. To minimize rework in the future, either the correct value taken from the data sheet will be used, or 68pF compensation capacitors will be used in cases of uncertainty. A review of all other compensation capacitors used in this design reveals several that are possibly overcompensated. Testing will be performed to see if there is any measurable adverse impact resulting from this overcompensation, and a DCN will cover any findings
9. The insertion of a 3k resistor in place of a "TBD" capacitor is a simple case of human error. As the test procedure doesn't test any of the functionality of the "Outer Loop" circuitry, this error went unnoticed. The test procedure will be amended to include some form of testing on the Outer Loop components to allow some verification that things are stuffed in accordance with the current design. Upon implementation of the Outer Loop control function, the test procedure will be modified to include appropriate testing

# 4 Summary

In many cases, experience gained in the field results in the useful exposure of deficiencies in our testing program. This should not come as much of a surprise. How we respond to this information will directly impact the future of our electronics effort. Some starting points that may be of use are:

1. When we find deficiencies in electronics, a reasonable and constructive method should be used to close the loop on the discovery and see to it that our procedures are updated, and our staff is educated to minimize the chance of repeating the mistake.
2. Little is gained through vilification or blame. It's probably better to foster a sense of inclusion in the commissioning process that spreads the feeling of ownership
3. In our environment, schedule pressure abounds. Using replacement parts conveniently on-hand that differs from the nominal design values can create a documentation problem and lengthy troubleshooting sessions that may well add to schedule pressure. This and other seemingly small factors create the all to familiar equilibrium of errors we often live with
4. This recent failure of ISS SN115 has yielded some procedural and technical deficiencies that if properly addressed will improve the future results of LIGO electronics