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Electrostatic Drive Amplifier for noise prototype tests

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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1 Introduction and scope

1.1 Purpose

This document covers the assessment of high voltage amplifiers intended for the noise prototype tests of quad suspensions for Advanced LIGO.

1.2 Contents

- Design philosophy
- Circuit diagram
- Operation
  - Gain compensation
  - ESD performance: full-power bandwidth, and DC
  - ESD performance: noise
  - A modification to the ESD circuit
  - Thermal issues

2 References

LIGO-E040109-00-K: Electrostatic drive amplifier for controls prototype tests.

LIGO-E040379-01-K: Electrostatic Actuator Drive Electronics Interface Control Document.

LIGO-E05075-00-K: Advanced LIGO electrostatic drive voltage and noise issues.

Apex PA94 data sheet is available on: http://eportal.apexmicrotech.com/mainsite/pdf/pa94u.pdf

"Composite Amplifier has Low Noise and Drift", Electronic Design, 12 June, 2000, by Paul Brokaw (Analog Devices).

3 Design philosophy

This work follows on from that carried out with the electrostatic drive amplifier for the controls prototype tests, as detailed in document LIGO-E040109-00-K. In that work two identical amplifier units were supplied, each designed to drive one 4 quadrant electrostatic drive panel based loosely on the design used in GEO 600. These amplifiers had 5 identical output channels, one for the bias voltage, and one for the signal for each quadrant. The channels were DC coupled, but designed with the option of using AC bias and signals if required. Each channel was based upon an Apex high-voltage op-amp, part number PA94, and was configured with a gain of 40 and a full-power bandwidth extending from DC–16 kHz.

However, after analyzing the function of the electrostatic drive (ESD) the following conclusions were reached by K. Stain, as detailed in document LIGO-E05075-00-K: that greater flexibility and control accuracy in steering the suspended mirrors using electrostatic control would be afforded by moving to

(i) two counter-electrodes for each quadrant array of electrodes patterned on the reaction masses, one strongly-coupled to the quadrant electrodes, and one weakly-coupled; and

(ii) a two-level drive output from the electrostatic driver electronics for each electrode, via paired controlling DACs. One DAC output could then provide coarse control, the other fine control, of the mirror.

Both (i) and (ii) would individually have the effect of greatly increasing the dynamic range of the electrostatic control—needed because of the dual requirements for the ESD: to provide short term peaks of feedback force for acquisition, and to provide continuous high frequency (above 1 Hz) feedback in science mode.

Therefore, the baseline for this work was an electrostatic amplifier—again based upon the Apex PA94 device (which were available from Glasgow Uni.), but now having 6 output channels rather than 5, in order to accommodate the additional weakly-coupled counter electrode. In addition, each ESD channel would now have two control inputs: a 'Hi' level input for coarse control, and a 'Lo' level input for fine control, such that both could be applied simultaneously via the single high-voltage output from that channel. The High and Low level inputs for each ESD channel would be electrically identical, allowing for differential input control voltages in the range of either ±10 V, or 0–10 V (TBD).

It was decided to split the function of each channel between two PCBs: a low-voltage Analog PCB to carry out signal conditioning functions, and a High Voltage PCB to carry a PA94 and its associated circuitry.

As the distance between each mirror and reaction mass may be ~5 mm in Advanced LIGO, as compared with 3 mm in GEO 600, a high value of ±400 volts was assumed for the eventual target working output for each ESD channel. This implies supply voltages of at least ±425 V, since in practice up to ±25 V may be lost across the PA94 (±450 V are the maximum allowed supply voltages for the PA94 devices, ±50 V being the minimum).

It was also assumed that the ESD would have to operate at DC, as well as at fixed frequencies of 8.192 or perhaps 16.384 kHz (TBD).

As regards thermal issues, Apex provides a thermal design spreadsheet (powerdesign_rev14.zip) which can be downloaded from

http://eportal.apexmicrotech.com/mainsite/design/pages/design_software.asp

This software was used to assess the need for heat-sinking at the highest frequency (16.384 kHz), using both the maximum supply voltages available locally (±307 V, from two Delta Elektronika ES0300-0.45 PSUs), and using the final target supply voltages of ±425 V. A target capacitive load of nominally 1300 pF was assumed, corresponding to a length of approximately 13 m of coax cable. A 0.13°C/W fan-cooled heatsink was selected, to be shared by two HV driver channels. Although fan-cooling will not be suitable for the final application, it was nevertheless used here in order to save time and space.

The amplifier has been designed conservatively so that it can drive over 10 m of coax cable at 16 kHz, with ultimately an 800 Vp-p sine wave, if necessary. However, Jay Heefner has pointed out that when using an AC drive at a fixed frequency, or over a limited bandwidth, it is possible to put an inductor in parallel with even a long (100+ m, say) cable, in order to turn it into a "transmission" line. Provided the source impedance of the driver is low (Jay mentions that he used a 75 Ω series resistor, although I think that up to ~200 Ω may be acceptable), then the current sourced by the ESD will be reduced considerably. Moreover, the heat dissipated by the PA94s will be reduced in proportion. It may also be possible to reduce the power dissipated in the ESD by replacing the PA94 op-amps by PA95s, which have a more limited bandwidth, but a quiescent current an order of magnitude smaller (1.6 mA (PA95), compared with 17 mA

(PA94)). This could reduce the static dissipation in the ESD by the same factor. This is currently under investigation. Thermal issues are discussed further in §5.5.

The concept for the prototype 6-channel amplifier is shown below in Fig.1, and the instrument itself as constructed is shown in Fig.2.

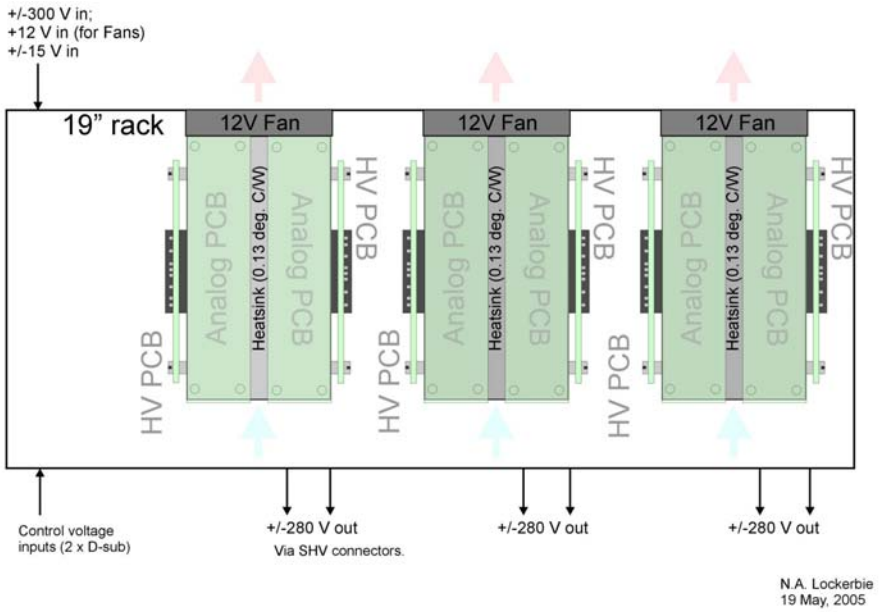

Figure 1. Design concept for prototype 6-channel ESD amplifier.

Figure 2. The prototype ESD amplifier showing the Analog PCB mounted on top of the slotted-heatsink, and one HV PCB mounted on its RH side (two HV PCBs were ultimately mounted on the heatsink).

4 Circuit diagram

The circuit diagram for one channel of the ESD is shown in Fig.3, below. It was divided between two PCBs: an Analog PCB, and an HV (High Voltage) PCB. On the Analog PCB the

Hi and Lo level inputs were buffered by INA 128 instrumentation amplifiers from Texas Instruments (Burr-Brown), configured to have ×1 gain. The outputs from these amplifiers were therefore single-ended ±10 V for a differential ±10 V input range, when the ref. inputs of these amplifiers were linked to ground. Alternatively, the ref. inputs could be linked to a precision –5.000 volt reference level, which translated the outputs to ±5 V for a 0–10 V input range. Inverting OP-27 – based amplifiers subsequently provided link-selectable gains of –1 for the ±10 V input range, or –2 for the 0–10 V input range. Thus the outputs of the inverting amplifiers could be arranged to span ∓ 10 V in both cases.

On the HV PCB the Hi level and Lo level outputs were then added together at (effectively) the summing input of an op-amp comprising an OP-27 op-amp and a high voltage PA94, in cascade. The Hi level input voltage was amplified here by a factor ×40, whilst the Lo level voltage was attenuated by a factor ×0.4. The weighting of these two signals was therefore in the ratio100:1.

The final high voltage output from this PCB was then routed to an SHV bulkhead connector, a 10 Ω resistor limiting the output current to a peak value of 100 mA.

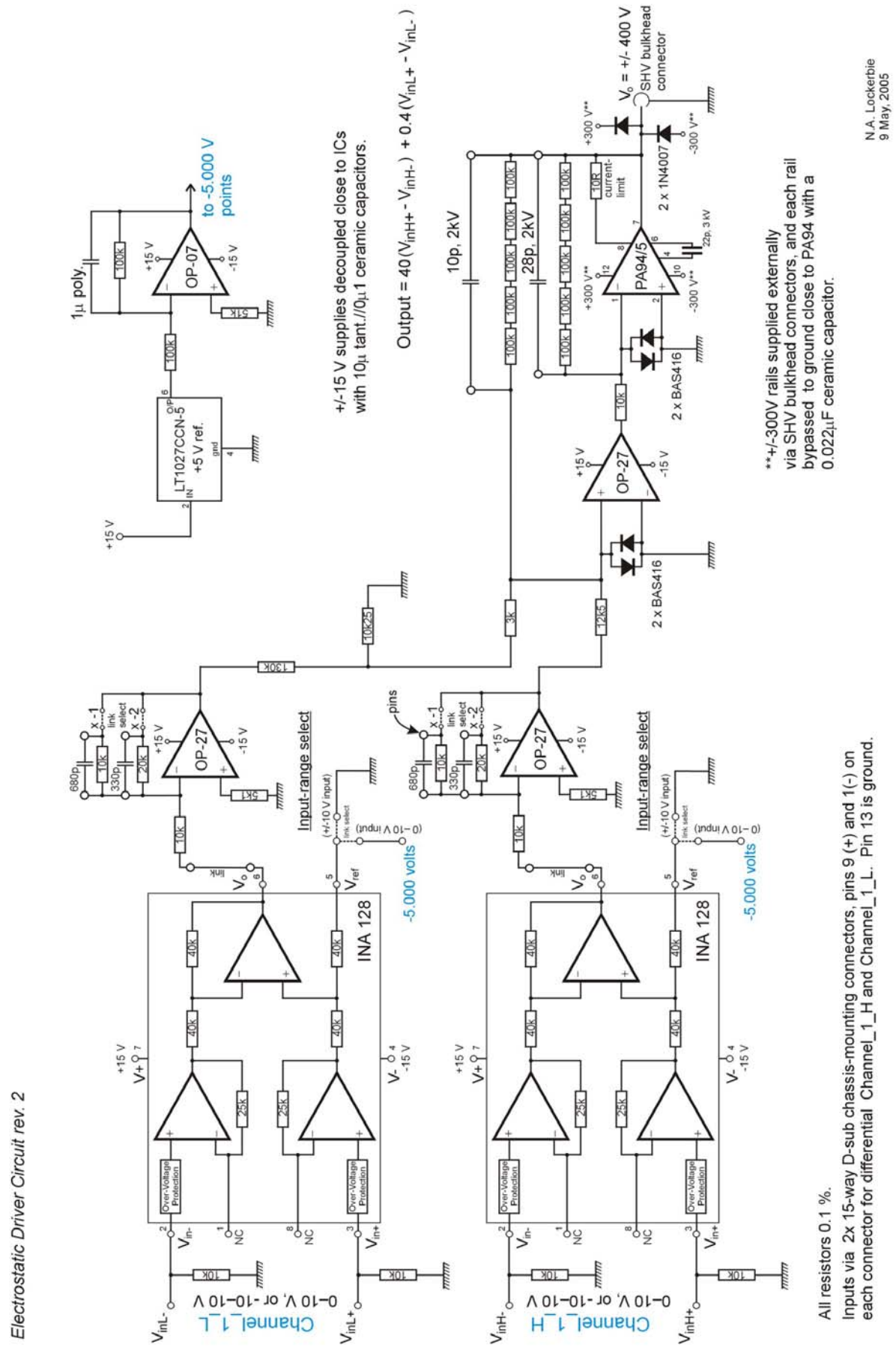

Figure 3. Circuit diagram of 1 channel of the ES Driver. Two HV output boards were built.

5 Operation

The power supply requirements were for both low voltage (± 15V), and high voltage, symmetrical supplies. The HV supply *had to be energized symmetrically* as the HV op-amp performance can be permanently degraded by operation with only one supply, even briefly. The minimum useful supply voltage for the PA94 is ±50V and the maximum permissible is ±450V. However, it is recommended that split supplies much above 300V should be used with caution, as tests at Strathclyde were carried out only up to 307V, the highest available, locally.

Current consumption from the HV rails for two HV driver channels (under no load conditions) was 33 mA (i.e., 10.1 W per channel at ±307V), rising to 62 mA at 16.384 kHz, with a nominal 1300 pF load (19 W per channel).

5.1 Gain compensation

The frequency response of one channel (Hi level input) is shown by the red trace in Fig.6, where the gain has been rolled-off deliberately at approximately 30 kHz, for reasons of stability. However, it was felt that the ~15% loss of signal amplitude at 16.384 kHz due to this roll-off could be compensated, and so the gain-compensation circuit shown in Fig.4 was incorporated into the driver in the form of a small PCB between the Analog and HV sections (located between the two PCBs) of one ESD channel.

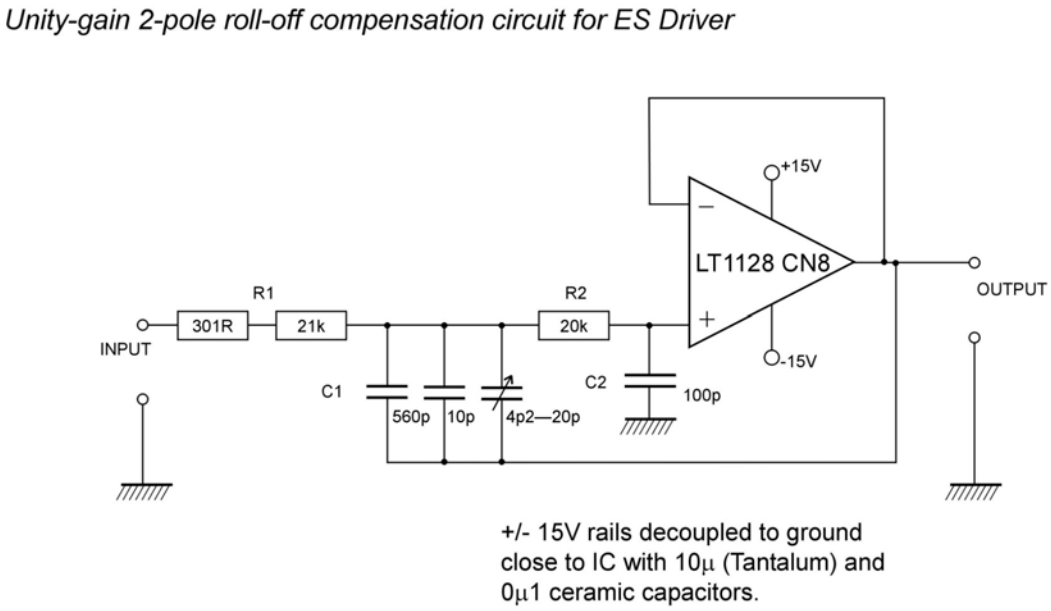

Figure 4. Gain compensation circuit.

The theoretical gain and phase response of this circuit are given in Fig.5, showing that in order to lift the gain in the frequency region of interest (8–16 kHz) the circuit creates an additional phase-lag of ~15° at 8 kHz, rising to ~30° at 16 kHz.

The measured frequency response of the compensated ESD is shown by the black trace in Fig.6. The full-power frequency response is seen to be quite flat up to 20 kHz, giving here a 574 Vp-p signal across a 1300 pF load.

The DC responses for the Hi and Lo level inputs are shown in Figs. 7 and 8, respectively.

Clearly, at DC the ESD was very linear up to and beyond ±290 V using the Hi level input, and using ±307 V power rails, and the gain was very close to the anticipated value of +40. The expectation is that this circuit would generate the desired ±400 V for an input of ±10 V (or 0–10 V), were ±425 V power rails available.

Similarly, an output of very close to the expected ±4 V was generated from a ±10 V change at the Lo level input of the ESD.

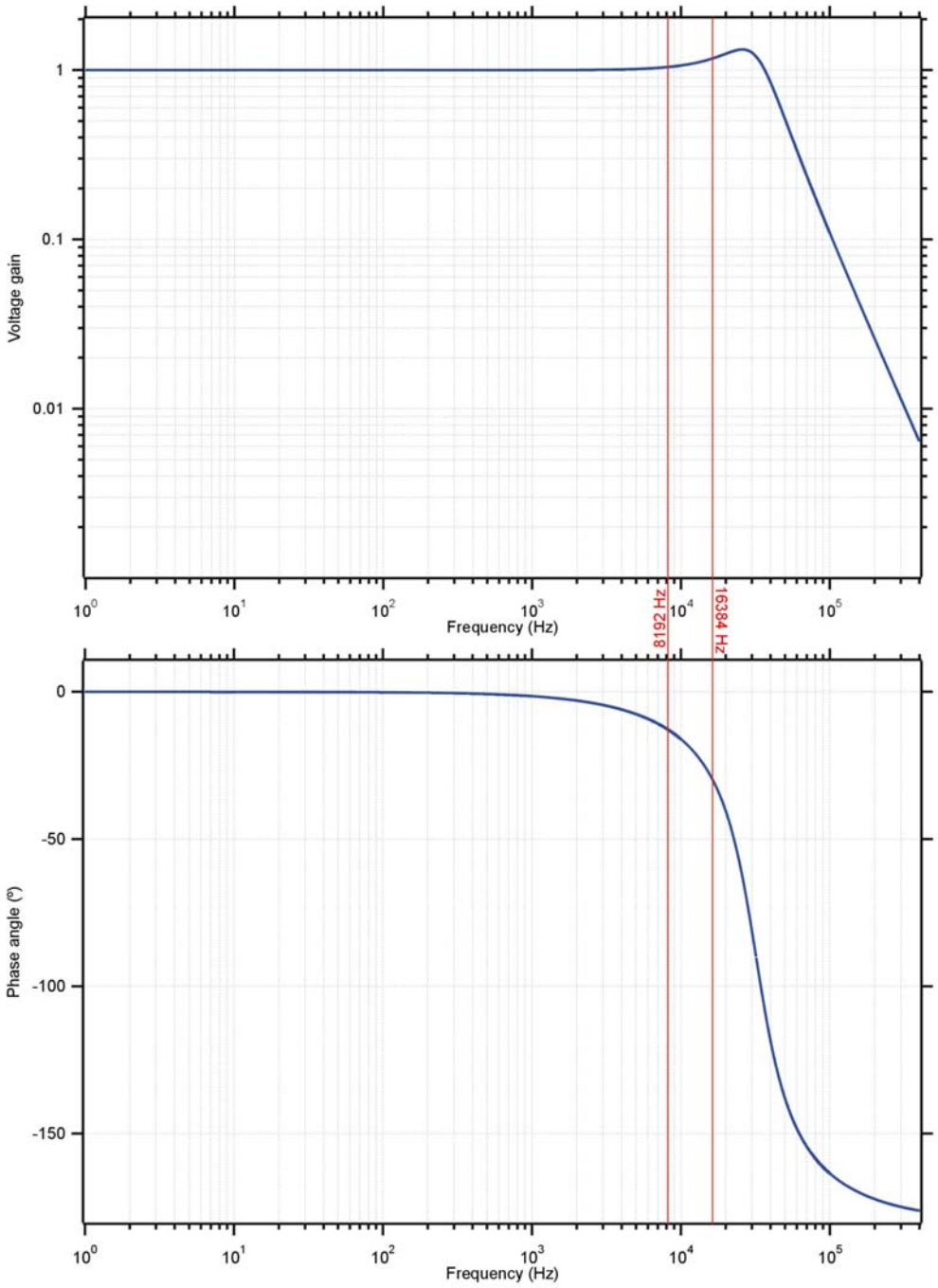

Figure 5. Theoretical amplitude and phase responses of the gain compensation circuit.

5.2 ESD performance: Full-power bandwidth and DC

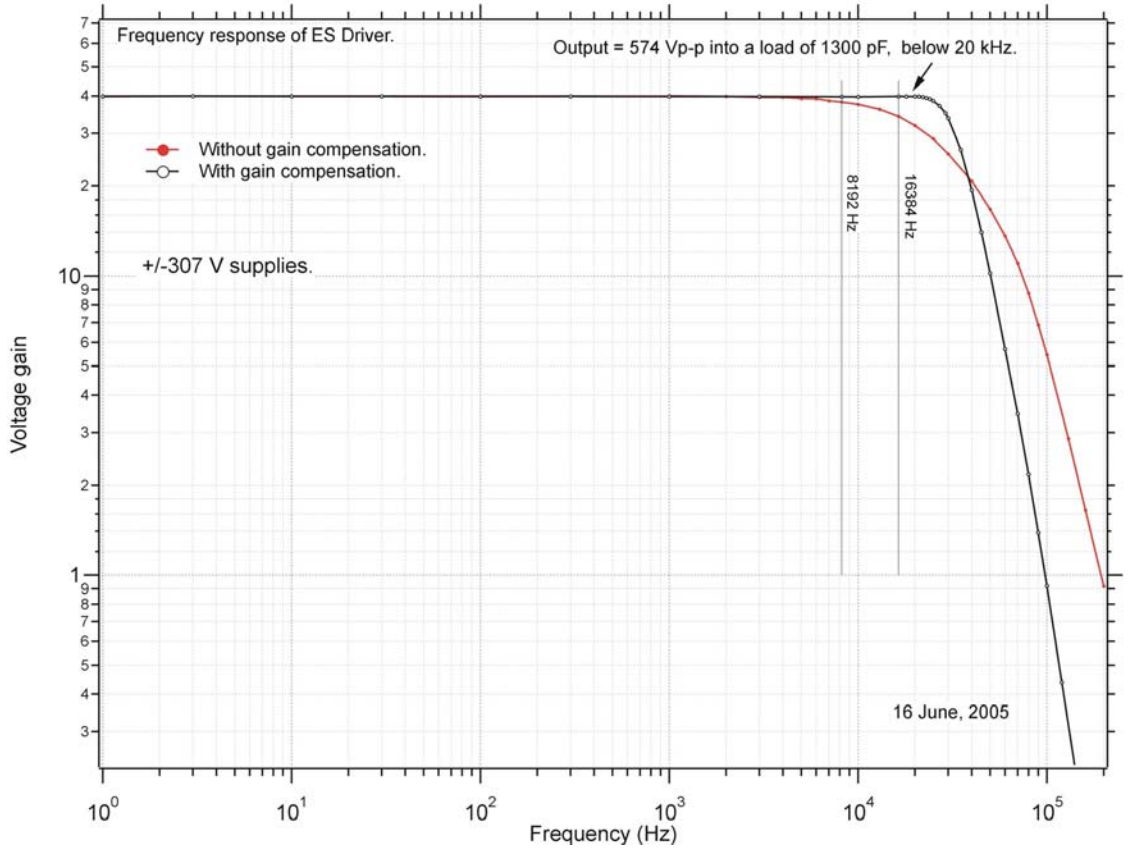

Figure 6. Measured frequency response of the ES Driver circuit without (red trace), and with (black trace), the gain compensation circuit of Figure 4.

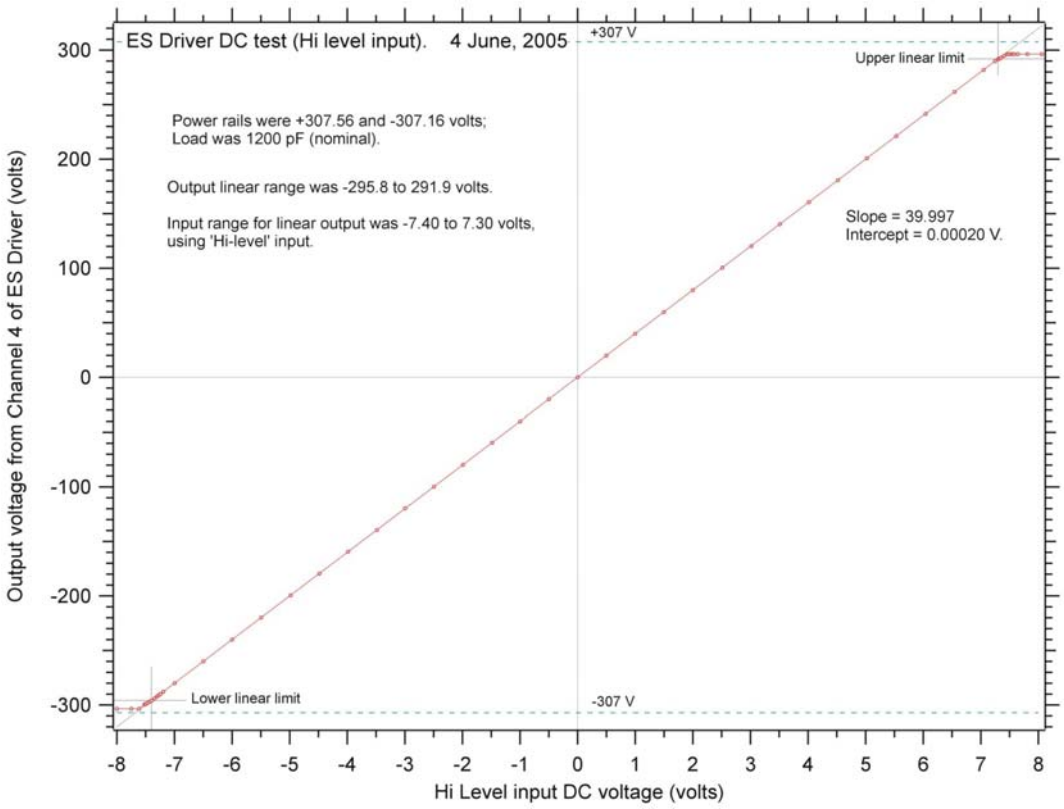

Figure 7. DC response of the ESD, using the Hi level input. Conversion slope = 40.00 ± 0.02.

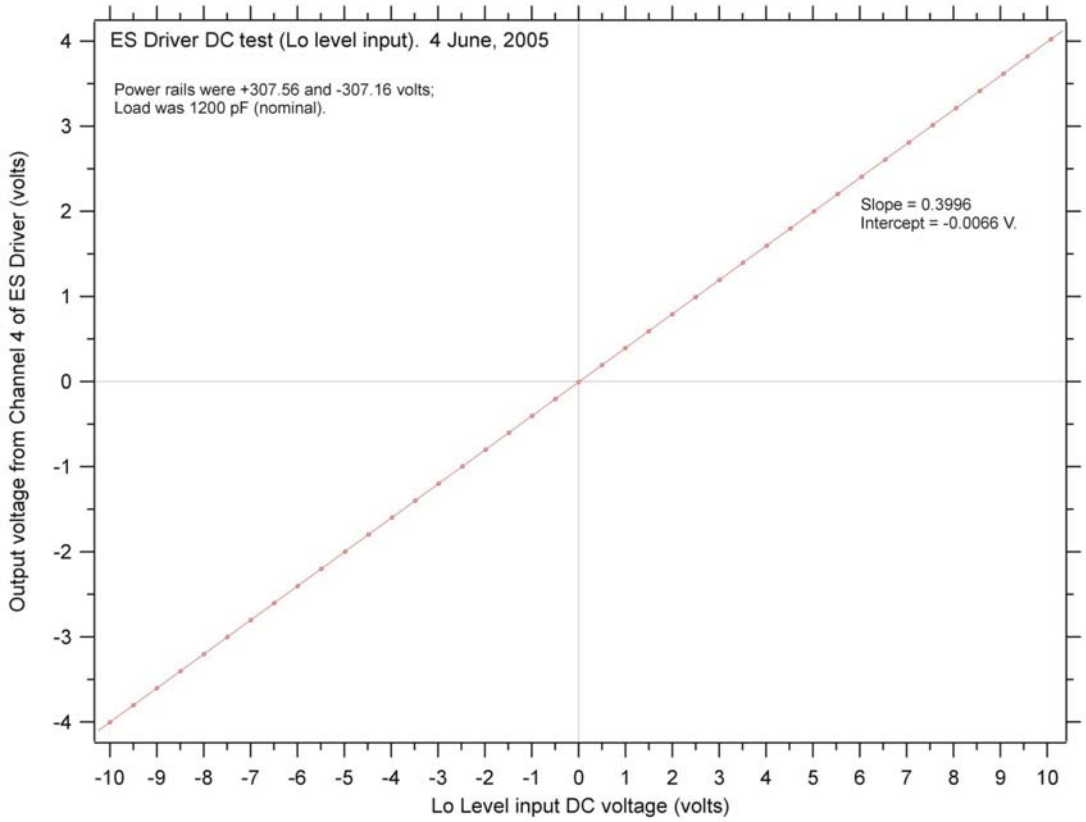

Figure 8. DC response of the ESD, using the Lo level input. Conversion slope = 0.39960 ±0.00001.

5.3 ESD performance: noise

Initially, the OP-27/PA94 composite amplifier was stabilized using 1.5 pF and 10 pF capacitors in parallel with the 500 k resistors of the outer and inner feedback loops, respectively.

	Power Spectral Density $\left(\mathrm{nV}/\sqrt{\mathrm{Hz}}\right)$ @			
Frequency (Hz):	1	10	8192	16384
PA94, alone	44	43	8	38
PA94 + OP27	220	85	16	60

Table 1. Power Spectral Density of ES Driver, referred to its input. In order to test the PA94 alone the OP-27 was removed from the circuit, and the PA94's 10k input resistor was grounded.

Nevertheless, very low (millivolt) level of oscillation and/or noise was visible in the output, and this was mitigated to some degree by increasing the feedback capacitors to 10 pF and 28 pF, respectively, as indicated in Fig.3.

Table 1 indicates, however, that the potentially low noise OP-27 (used for its low voltage noise of typically 3.5 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ @ 10 Hz, coupled with a reasonably high slew-rate of 2.8 V/μs) has actually degraded the noise performance of the ensemble. Much of the degradation probably can be attributed to the input noise current of the OP-27 flowing in the (at present) fairly high-value feedback resistor network. Note that the noise level quoted in document LIGO-E040109-00-K for the controls prototype ESD is equal to the voltage noise of the PA94 alone (11 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ @ 10 Hz is the value given for the PA94's voltage noise in the Apex data sheet).

5.4 A modification to the ESD circuit

The fairly minor modification to the present circuit shown in Fig.9 should improve its phase margin—which may have a useful impact on the residual noise. Furthermore, the reduction in number and a subsequent reduction in value of the resistors around the composite op-amp, by a uniform factor of 5, say, should decrease the noise level. This, together with a change to an ultra-low noise JFET input op-amp such as the AD745, in place of the OP-27, should reduce the level of noise significantly at both DC and 16 kHz.

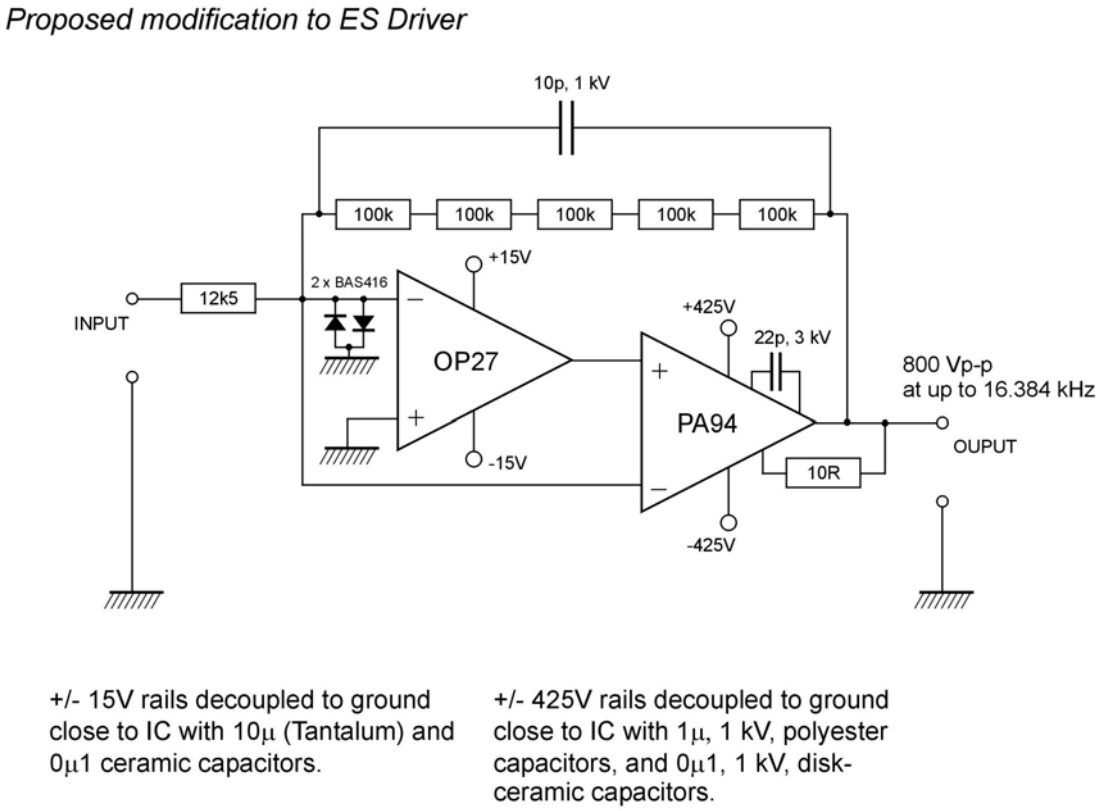

Figure 9. First phase of the proposed modification to the HV output stage of the driver, which follows the design in "Composite Amplifier has Low Noise and Drift", Electronic Design, 12 June, 2000, by Paul Brokaw (Analog Devices). In a second phase the resistors would be replaced by ones a factor of 5 smaller in value.

5.5 ESD performance: thermal issues

The Apex thermal model predicted the actual dissipation of the ESD quite well for the conditions of ±307 V supplies, and a capacitance of ~2300 pF driven with a 496 Vp-p sine wave at 16.384 kHz. The prediction was 20.8 W dissipated in the PA94, compared with the measured value of 20.6 W. For the target maximum ESD output of 800 Vp-p at this same frequency, using ±425 V supply rails, and with a 1300 pF load, the predicted dissipation rises to 29.7 W.

Figure 10 shows the heatsink temperature, as measured with a passive contactless IR thermometer, when the cooling fan was switched off, and then back on again, with 20.6 W dissipation in each of two output channels (41.2 W, total). The Apex thermal model indicates that this arrangement would still be satisfactory under the higher dissipation, mentioned above, of $2 \times 29.7 = 59.4$ W.

Therefore, as the actual fan-assisted heatsink was measured to have an efficiency of 0.15°C/W, the minimum acceptable individual heatsink per PA94 device must be rated at 0.3°C/W.

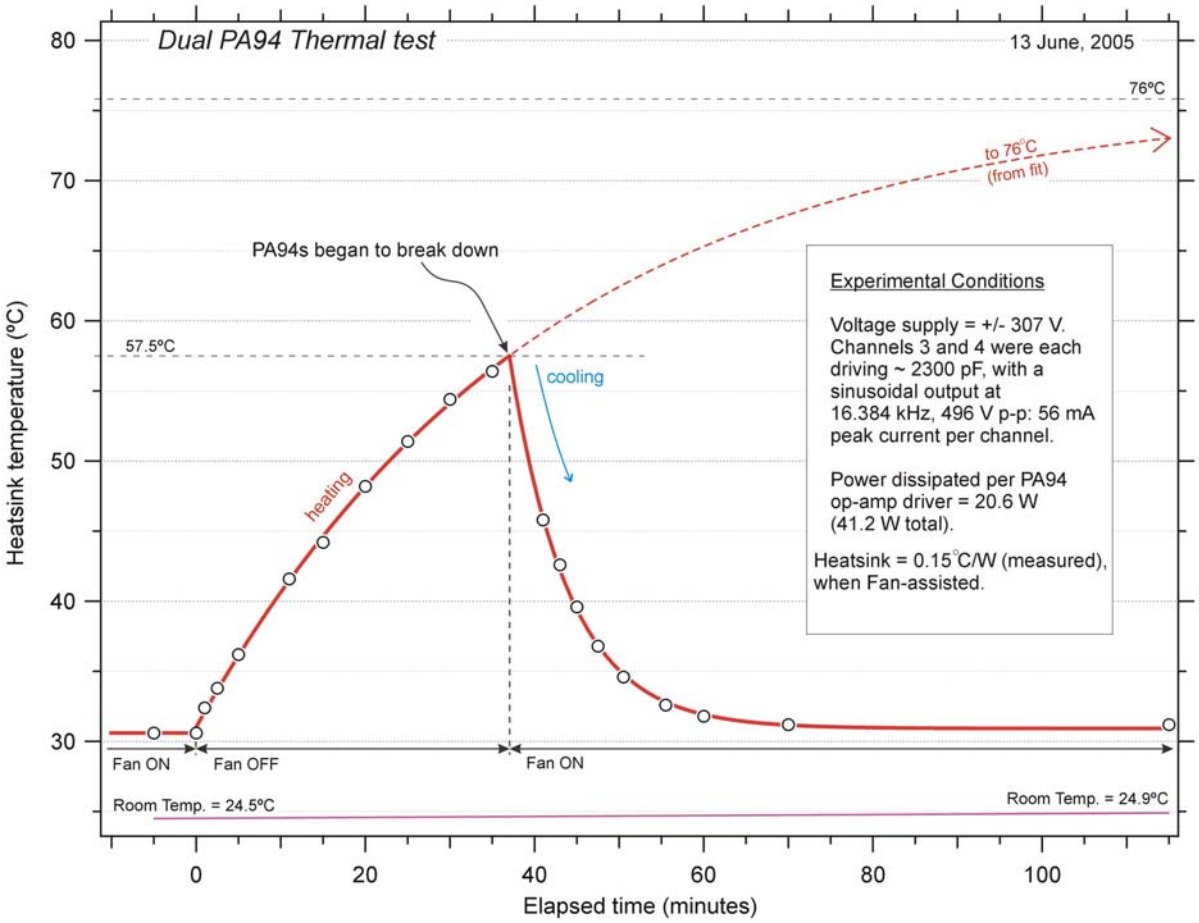

Figure 10. Thermal response of the ESD with 2 channels each driving 496 Vp-p into into ~2300 pF at a frequency of 16.384 kHz. The PA94 HV op-amps for both channels were mounted onto the same '0.13°C/W' (0.15°C/W, as measured) fan-cooled heatsink.

In terms of physical size, such a passively cooled heatsink might measure 300 mm × 300 mm × 40 mm fin depth—such as the (order code) 490-7040, from RS Components. Naturally, other fin geometries can be more compact.