LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
- LIGO -
CALIFORNIA INSTITUTE OF TECHNOLOGY
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# PROPOSAL FOR A NEW CONVERTER DESIGN

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of the LIGO Project.

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# 1 INTRODUCTION AND OVERVIEW

This is a proposal to develop a new converter technology for advanced LIGO. This includes both analog-to-digital converters (ADC) and digital-to-analog converters (DAC) which operate at fast data rate. It also includes fiber-based data distribution links which simplify the interfacing with the compute engines. The current technology has several severe limitations:

*i)* **Collocation of analog and digital:**
Due to restrictions in cable length the location of the computer which is used to process the data dictates the location of the converters as well as the location of the low noise analog electronics. The close proximity of the analog electronics to the fast digital electronics causes problems with EMI contamination. A much better solution would be to have computers and analog electronics in separate rooms.

*ii)* **Poor noise performance:**
Most commercially available units are not engineered with low noise and low latency in mind. Typically, one has to choose between low noise units based on the ΣΔ-technology which have a long pipeline delay and units which have a short delay but poor noise performance. By moving the converters away from the noisy backplane buses one can provide them with clean regulated power.

*iii)* **Inadequate throughput:**
A solution that is based on multiple boards talking to a local bus such as VME has a limited data throughput since the online controls processor has to perform a scatter-gather-read at every processing cycle. This also adds significant delays and reduces the time the processor has to crunch the data. It would be better to assemble all the ADC data into a single block before pushing it into the processor. On the output side the data is preferably sent out as a single block and distributed between the different DACs by hardware.

*iv)* **Limited timing support:**
Most commercial converters support an external clock input. In order to synchronize the converters with UTC the processor has to start the clock on the 1 pps boundary and hope that the converter keeps counting correctly for days and weeks. Errors can occur without anyone noticing. It is much better to run the converters synchronized with our timing distribution system at all times and push time-stamped data into the processor at a regular rate.

*v)* **Convoluted data paths:**
In some cases the processor and the converters can not be located close to each other. For example, the QPDs are located in the end stations but need to send their data to the ASC and LSC in the corner station. Currently, the suspension controller reads these channels and sends them to LSC and ASC through reflective memory. If all converters are fiber coupled, they can be located anywhere on site and connect to any other unit on site.

*vi)* **High costs:**
LIGO deploys about 500 converters per interferometer without counting HEPI and without counting spares and channels that are not used. The price per converter is between $500 and $4000. If we assume an average cost of $700 per channel, the estimated total cost for all 3 interferometers was about $1M (see Appendix A). For advanced LIGO we can expect this number to increase by at least a factor of 2—but probably more considering that HEPI alone adds about 300 converters. We estimate that off-the-shelf converters for advanced LIGO would cost us between $2M and $4M using the same technology.

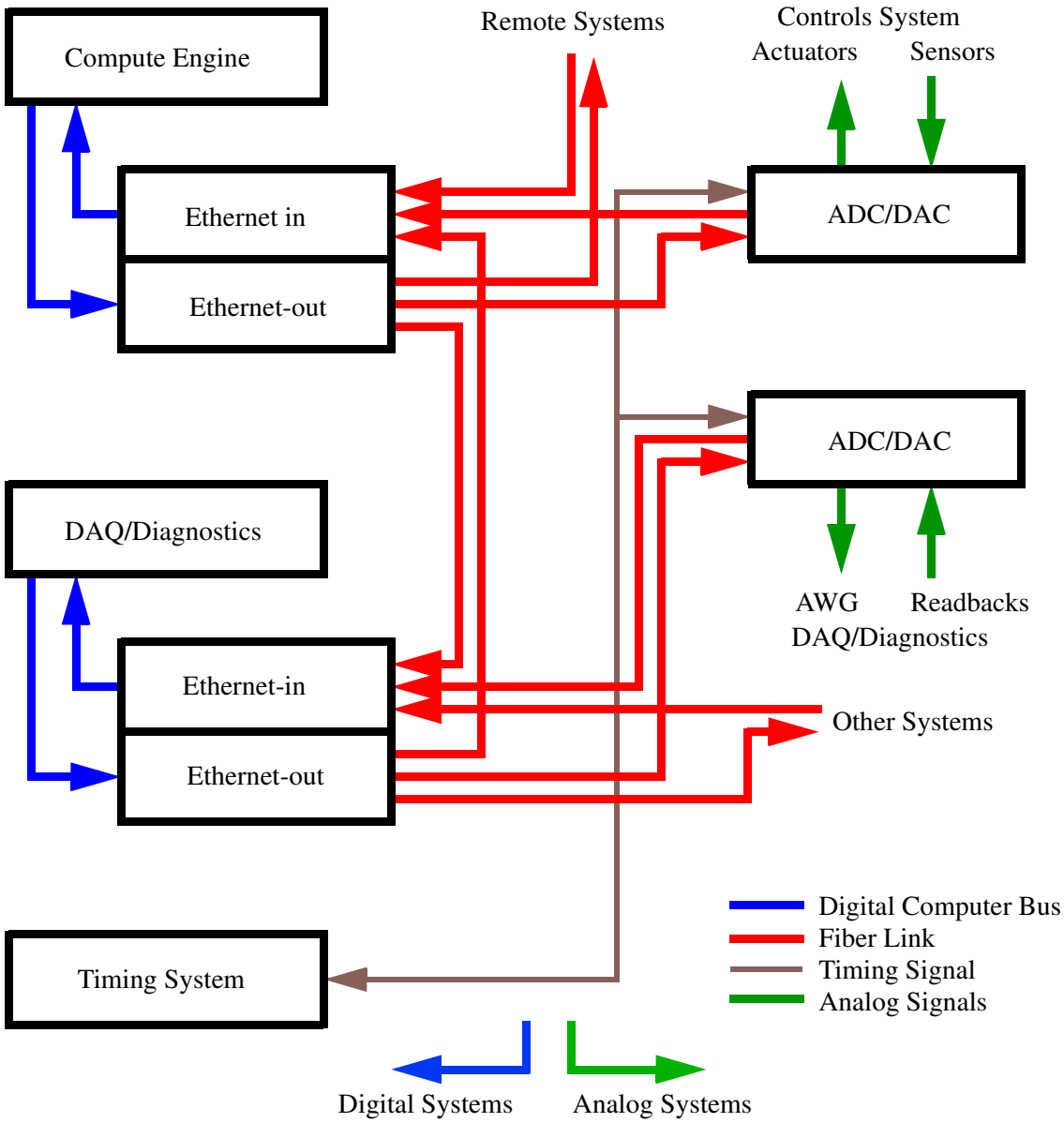


Figure 1: System Overview.

We propose to develop a system which separates the converters from their back-ends (see Figure 1). This will allow us to place converters and analog electronics close to sensors and actuators and avoid long cable runs in analog. We propose to use gigabit ethernet cards with DMA that communicate with the converters through fiber optics and transfer data to and from a processor by raw ethernet frames. This should significantly reduce the communication overhead of the processor and keep the latencies short. The gigabit fiber links could also be used for point-to-point communication between the processors.

An important feature of our converter system is that timing and synchronization with UTC is built-in reliably. The converters are clocked by the new timing system and run synchronized at all

times without any processor intervention. The ADC data is time-stamped and sent to the processor at regular intervals—again without burdening the processor. This significantly reduces the timing responsibility of the processor which just has to guarantee that the processed data is ready before it is needed by the DACs. This system would no longer have to rely on the correct counting of electronic pulses over long periods of time. Any timing error would be immediately corrected and reported by the new timing system.

When choosing a low noise ADC or DAC we are limited to what is commercially available. The lowest noise ADCs and DACs are currently based on ΣΔ-modulators. However, they also introduce long pipeline delays and are not suitable for our digital controls system. There are other technologies that avoid the long pipeline delay but typically have worse noise figures. We propose to utilize the over-sampling technique to improve their noise performance. With the current system increasing the sampling rate means increasing the processor load. Since our current controls system operate near maximum capacity, this is not easily possible to the extend we want. In the proposed system we intent to implement decimation and interpolation filters in hardware. As an added benefit this will eliminate analog anti-aliasing and anti-image filters which have to operated near the Nyquist frequency of the computer data rate.

# 2 Basic Requirements

Here is a list of the fundamental requirements:

- Absolute timing precision relative to UTC: 1 µs.
- Converter range: ±10 V single-ended, or ±20 V differentially.
- Converter noise single ended: 100–300 nV/√Hz (best effort).
- Latency between converter and processor: < 5 µs.
- No restriction on converter location.
- No electrical connection between converters and processors (fiber links).
- Detection of transmission errors.
- Support for diagnostics.

# 3 Design Considerations

This section outlines a conceptual design and goes through some of the technical considerations that went into this proposal. An important point is to allow for future growth. We therefore chose a design that is based on programmable logic chips, that has a clearly defined hardware interface between converter units and processing, that is fast enough to support increased demands on channel density and that is flexible enough to allow for different topologies as may be dictated by changing requirements for data acquisition and feedback networks.

## 3.1 ADC

An ADC suitable for our purpose is the AD7634 from Analog Devices. It is a 18-bit design and boosts a dynamic range of 103 dB. Running this device at 524288 Hz ($2^{19}$ Hz) and utilize an input range of ±10 V yields a theoretical noise level of 100 nV√Hz. Figure 2 shows a sketch of the ADC input section. Since the final decimation is done by the converter logic, the anti-aliasing filter can

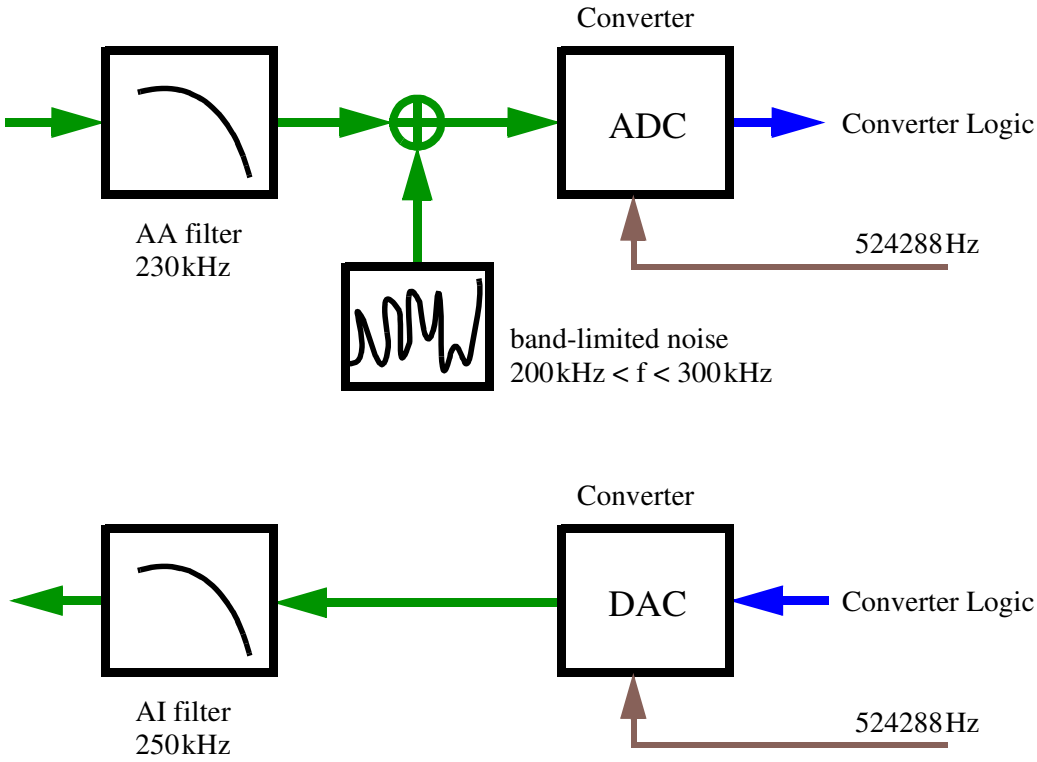


Figure 2: Analog input section (top) and analog output section (bottom).

be chosen with a cut-off around 200kHz. To guarantee that the last bit of the conversion is random a band-limited random noise source can be added to the analog input signal before it is fed into the ADC. To reach the ultimate noise level it is in principle possible to run several ADCs in parallel and add the individual signals in digital.

## 3.2 DAC

A DAC suitable for our purpose is the PCM1794 from Texas Instruments. We propose to run them at a rate of 524288Hz including an 4 time oversampling. Figure 2 shows a sketch of the DAC output section. The converter logic must provide the oversampling as well as a suitable interpolation filter. The cut-off of the anti-image filter can then be chosen around 50kHz. To reach the ultimate noise level it is in principle possible to run multiple DACs in parallel and add the individual output signals in analog.

## 3.3 Converter Logic

Figure 3 shows a diagram of the converter logic for a single input and output channel. The ADC data is clocked into a 32-bit register. Depending whether the desired output rate is 2048Hz, 16384Hz or 524288Hz the data is fed through a 1kHz low pass filter, an 8kHz low pass filter or a bypass path, respectively. In the first and second case the decimation is done by ignoring 255 out

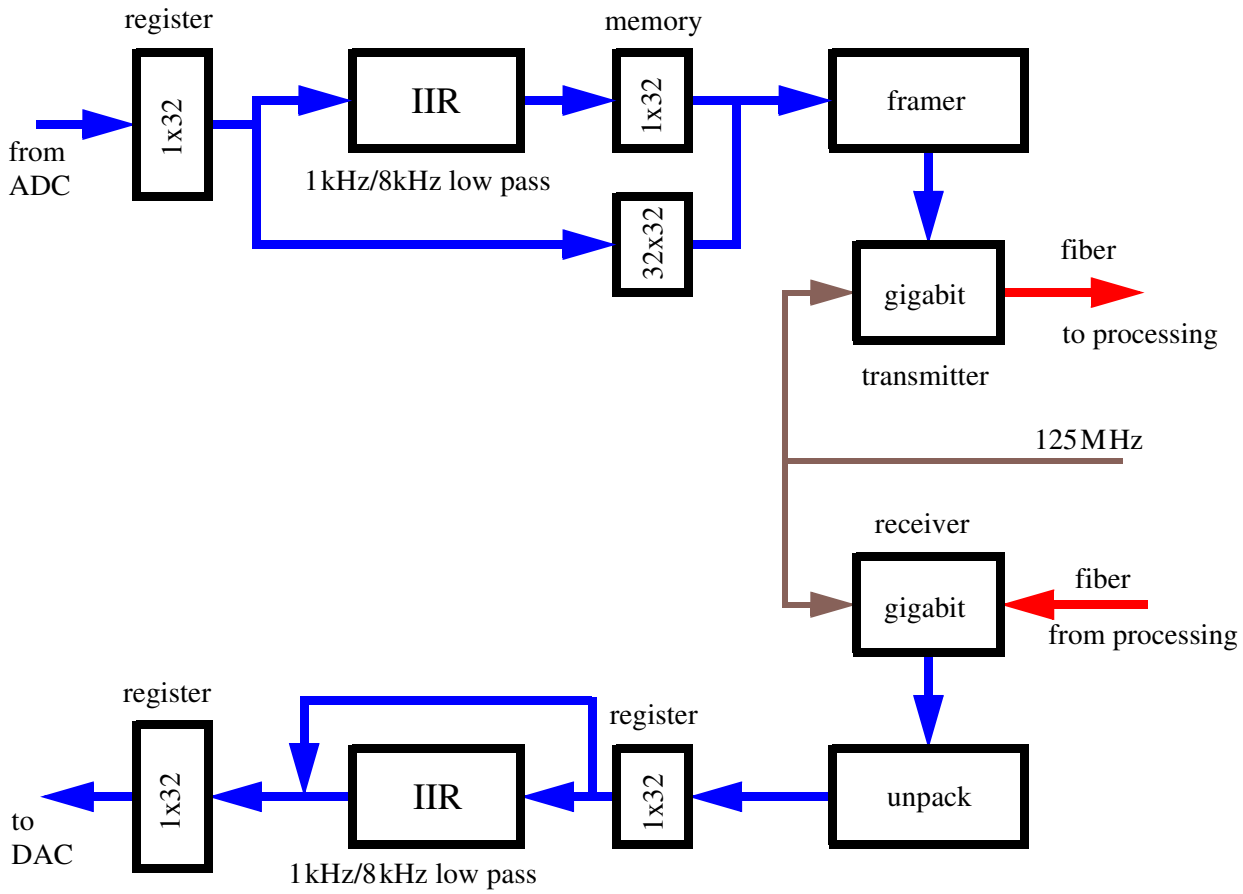


Figure 3: Diagram of converter logic for one input channel (top) and one output channel (bottom).

256 samples or 31 out of 32 samples, respectively. The data is then written into a memory block where it waits to be combined with other ADC channels and sent away through the gigabit transmitter. The oversampling architecture has the advantage that multiple sampling rates could be supported simultaneously. In the diagram of Figure 3 these are 2048 Hz/16384 Hz and 524288 Hz. The first rate might be useful for data acquisition, the second rate for the online controls system and the third rate for diagnostics.

Data received by the gigabit receiver is unpacked and fed to the corresponding DAC channel. A simple register that is read faster than it is written can be used to up-sample the input data to 524288 Hz. Depending on the input rate a low pass filter with 1 kHz cut-off, a low pass filter with 8 kHz cut-off or a bypass is required as an interpolation filter. To minimize delays it is important that the decimation and interpolation filters are implemented as IIR filters.

We propose to usa a field programmable gate array (FPGA) to implement the functionality of the converter logic. For example, the Spartan-3A DSP family implements a high number of logic cells and hardware multipliers in a single chip for relatively low costs, whereas the Virtex-4 FX family implements gigabit transceiver modules.

## 3.4 Fiber Link

### 3.4.1 Hardware Layer

Gigabit receivers can operate with a rate anywhere between 600Mb/s and 10Gb/s. We propose to run our transmitters at the gigabit ethernet line rate of 1.25 GHz. A suitable optical transceiver is the HFBR-5710L (multi-mode fiber, up to 500m) and the HFCT-5710L (single mode fiber, up to 10km) from Agilent. Both of these devices are compliant with the SFP (small form factor pluggable) standard and are hot pluggable. The maximum data rate through such a fiber link will be approximately 100MB/s.

### 3.4.2 Protocol Layer

The most common encoding scheme for gigabit links is called 8B/10B. Eight data bits are encoded as 10 bits so that during transmission the disparity between zeros and ones is minimized. This code also allows for additional control characters that can be used to indicate a start of frame and an end of frame. A special comma character is used to align the bit stream to a byte boundary. Most gigabit serializer/deserializer devices support this encoding scheme by default and also support the calculation of a cyclic redundant checksum (CRC) in hardware.

We propose to make use of the same encoding scheme by using raw Ethernet frames. The protocol includes configuration and converter data frames (see Converter Uplink, T060212, section 4). This allows the use of commercial Ethernet cards at the processor end.

## 3.5 Processor Interface

We propose to use Ethernet cards, preferably with direct memory access, to interface the fiber links to the processor. They will probably be attached to a PCI Express or PCI-X bus. It would also be possible to connect the fiber through switches or routers depending on the latency introduced.

# 4 Advanced Features

The features in this section are meant to be ideas how the proposed system can be expanded in the future. Using a large FPGA as the main logic core makes it possible to add future expansions by reprogramming. In particular, extensions of the link protocol and improvements in the switching rules should be easy to add at a later date. The proposed design does not depend on a particular ADC or DAC chip and a future redesign of the converter unit will be able to implement improvements in converter technology transparently.

## 4.1 End Station Processors

The only truly fast feedback signal of the end station suspension processor comes from the LSC which is located in the corner station. The fiber links of the new system would make it straight forward to move the suspension processor into the corner station. This is even more true for the DAQ channels or any other slow feedback system like HEPI. This means all processing engines

can be located in the corner station and only the analog electronics with their converter units would remain in the end station.

Since the signal travel time in a fiber to the end stations is about 20µs, this arrangement would add a full clock cycle delay in both the sensing path and the actuator path. To reduce the round-trip delay by 2 one could run the end stations with an offset of exactly half a clock cycle (about 30.5µs).

## 4.2 Support for Heterodyning

Another technique that has proven useful in recording the anti symmetric port signal at the free-spectral-range of the arm cavity is to heterodyne the data. Since a sampling rate of 524288Hz will cover the first 6 multiples of the free-spectral-range frequency, support for heterodyning might be build directly into the converter units. But, even if not, one should be able to avoid extra converters.

## 4.3 Integration with the Slow Controls System

One of the problems in LIGO is that it is impossible to record all the slow controls signal at a rate of 16Hz. The main problem is that it is very inefficient to collect the data through ethernet network connections one signal at the time. Another problem is that the converters and binary IO channels of the slow controls system are not synchronized by our timing system. All these problems could be solved by synchronizing the front-ends of the slow controls system with our timing system and by sending the gathered data through one of the new fiber links directly to the data acquisition system.

## 4.4 Advanced Diagnostics Functions

The new system will make it possible to support an arbitrary waveform generator with higher sampling rate which can send its output directly to any DAC channel. The signal could be added to a controls signal by the converter unit before it is written to the DAC. Similarly, it could be added to the signal read from an ADC—making it possible to implement a simple loop back test.

To test the input path the new converter units could also support a pattern generator that can replaces the ADC signal with a well-known one. If a converter unit supports both ADCs and DACs, a loop back test can also be implemented in analog by switching the ADC inputs to one of the DAC outputs.

# 5 PRELIMINARY DESIGN

## 5.1 OVERVIEW

In order to design the prototype components of the converter system it is necessary to define a few basics like form factor, signal conventions, power supplies and connectors. A number of factors go into determining these things. First, the FPGAs which are central to the design generate a large noisy supply current due to the internal switching nodes. In order to keep the converter grounds quiet it is necessary to isolate the FPGAs from the converters. So, the FPGAs were moved off the converter card to a separate controller card.

This also allows switching regulators on the controller card to supply the FPGA power and other low voltage logic from a +12V source which greatly reduces the associated heat and noise. To maintain the ground isolation the signals between the FPGA and the converters are LVDS. There are 7 dedicated clock lines and 21 data lines for a total of 28 differential pairs. Second, the analog circuits need quiet power supplies, so on board low noise dropout linear regulators were included. However, no negative voltage versions are available. So, a system using a clean reference voltage to drive power amplifiers was developed. In addition to the ±6.5 V and ±16.5 V for the ±5 V and ±15 V, respectively, it needs ±24 V for the controller circuit, but it is very quiet and immune to input noise. The need for enough circuit area with space for the cooling air flow and the desire to use an accepted standard led back to the eurocrate standard with 233mm (6U) high by 280mm deep by 30.48mm (6HP) wide boards. Each controller card connects to two converter cards, so there is room for four controller cards and eight converter cards in a full size crate. Standard VME connectors on the converter boards and a VME64x connector type layout on the controller boards are able to handle the power and interconnect requirements. The optical fiber timing and uplink connections are made to the front of the controller boards. A more detailed and complete description of the system can be found in Converter Backplane T060082-A-D.

## 5.2 ADC BOARD

A prototype of a 16 channel fully differential ADC board based on the Analog Devices AD7634 has been designed (D060535) and built. The AD7634 is an improved version of the AD7679 with wider input voltage range that simplifies the input amplifier-filter.

The board has been tested (T070XXX-00-C) and found to meet all design requirements including an input referred noise less than 320 nV/rtHz with 40Vpp sine input. The Total Harmonic Distortion and Crosstalk results are equally impressive. Only minor fixes and design tweaks are needed to go into production.

## 5.3 DAC BOARD

A prototype of a 16 channel differential out DAC board based on the Texas Instruments PCM1794A has been designed (D060293) and built. The PCM1794A is a better part than the PCM1704 which may soon be obsolete. The board is functional and in the process of being tested.

## 5.4 Controller Uplink Board

A prototype of the Controller Uplink board has been designed (D060309). The board is in the process of being laid out and the programming (T060212) simulated. The controller board contains two FPGAs for the IIR digital filter engines (T050060 and T070240) and converter interfaces. It also has an FPGA for the gigabit uplink and the timing receiver.

The FPGAs selected to do the decimation filtering are from the Xilinx Spartan 3A DSP family. The smaller of the two devices, the XC3SD1800A, implements 84 hardware multipliers and plenty of additional logic slices. It should easily handle 16 channels of IIR filters. Since the family members are pin compatible, the larger device, the XC3SD3400A, can also be used, if need arises.

The uplink FPGA is connected to the two filter engine FPGAs and to two more filter engine FPGAs on another controller board via the backplane. Therefore, any uplink can access up to four converter boards. In addition to the front panel optical fiber ports for the gigabit links and the timing signal there are two digital control connectors and a JTAG connector for programming the FPGAs.

The uplink FPGA is from the Virtex 4 FX family and comes with integrated gigabit transceiver tiles and ethernet media access controllers. The smallest device utilizing the gigabit links is the XC4VFX20 and should be sufficient. Again, pin compatible larger devices are also available (XC4VFX40 and XC4VFX60). Two ethernet ports will be implemented per controller board.

## 5.5 Decimation Filtering

A general purpose IIR filter engine has been developed. There are two versions available currently: a version with 35 bit fixed point precision (T050060-00) and one with 52 bit fixed point precision (T070240-00). Both filter engines have been fully simulated and tested in real hardware. Both use 128 cycles for each acquisition cycle to compute 7 and 3 second-order sections, respectively. By using two instead of one multiplier per filter the number of second order sections can be increased to 12 and 6, respectively, without adding additional latency. 35 bit precision is sufficient to decimate the data rate to 16384Hz. However, the 52 bit precision filter engine has to be used to decimate down to 2048Hz or lower.

# 6 Production and Testing

## 6.1 Production

All the boards have been sent out for production and stuffing with no special problems. Slowly increasing the batch size and watching for problems should maintain control.

## 6.2 Testing

It is planned that the testing be automated as much as possible. Each controller board implements two AES/EBU links. The AES3 standard specifies that each link contains two stereo channels. One link will be used as an input, whereas the other is an output. The AES/EBU links can be

directly interfaced with the Audio Precision analyzer. These analyzers were developed for the audio community and have full support for mixed analog/digital testing. The Audio Precision analyzer can be programmed by a PC and with some relay boxes (also from Audio Precision) it should be possible to automatically test the ADC and DAC boards. Since the controller boards are programmable we can load a self test program to test the hardware.

# 7 RELEVANT DOCUMENTS

[1] ADC Performance Testing, D070000-00

[2] Test Board Report, T060203-00

[3] Crate design (form factor), T060082-A

[4] Crate thermal management, D070000-00

[5] Converter uplink design, T060212-00

[6] Configuration EEPROM design, T070152-00

[7] ADC board schematics, D060535-B

[8] DAC board schematics, D060293-A

[9] Controller uplink schematics, D060309-A

[10] IIR Filter (35 bit precision), T050060-00

[11] IIR Filter (52 bit precision), T070240-00

[12] Uplink simulations, D070000-00

[13] Xilinx Spartan-3A DSP data sheet, http://direct.xilinx.com/bvdocs/publications/ds610.pdf

[14] Xilinx Spartan-3 family user guide, http://direct.xilinx.com/bvdocs/userguides/ug331.pdf

[15] Xilinx Virtex-4 data sheet, http://direct.xilinx.com/bvdocs/publications/ds302.pdf

[16] Xilinx Virtex-4 user guide, http://direct.xilinx.com/bvdocs/userguides/ug070.pdf

[17] Audio Precision 2700 series analyzer, http://ap.com/pdf/2700Brochure4_04.pdf

# APPENDIX A SURVEY OF CURRENT CONVERTERS

This is an estimate on how many converters are currently installed by LIGO. It does not try to count converters that are available but not used.

**Table 1: Converter Count**

| System | Estimated number per ifo |
|---|---|
| DAQ | 250 |
| LSC | 30 |
| ASC | 70 |
| SUS | 180 |
| Total/ifo | 530 |
| SEI | 300(?) |

This is a list of converter boards currently installed at LHO and LLO. These numbers do not include HEPI, spares or the development costs of the FDI DAC (~$100k).

**Table 2: Installed Converter Boards**

| Board | Type | Channels | price [k$] | H1 | H2 | L1 | total | ext. [k$] |
|---|---|---|---|---|---|---|---|---|
| ICS-110B | ADC | 32 | 11 | 12 | 12 | 12 | 36 | 396 |
| Pentek | ADC/DAC | 8/8 | 8 | 21 | 24 | 21 | 66 | 528 |
| ICS-115 | DAC | 4–32 | 5–12 | 3 | 3 | 3 | 9 | 66 |
| ISC-130 | ADC | 8 | 8 | 1 | 1 | 1 | 3 | 24 |
| FDI | DAC | 8 | 8 | 3 | 3 | 3 | 9 | 72 |
| **total** | | | | 40 | 43 | 40 | 123 | 1086 |