LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
- LIGO -
CALIFORNIA INSTITUTE OF TECHNOLOGY
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PROPOSAL FOR A NEW CONVERTER DESIGN

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Table of Contents

1 INTRODUCTION AND OVERVIEW

This is a proposal to develop a new converter technology for advanced LIGO. This includes both analog-to-digital converters (ADC) and digital-to-analog converters (DAC) which operate at fast data rate. It also includes fiber-based data distribution links and data concentrators that simplify the interfacing with the compute engines. The current technology has several severe limitations:

i) **Collocation of analog and digital:**
Due to restrictions in cable length the location of the computer which is used to process the data dictates the location of the converters as well as the location of the low noise analog electronics. The close proximity of the analog electronics to the fast digital electronics causes problems with EMI contamination. A much better solution would be to have computers and analog electronics in separate rooms.

ii) **Poor noise performance:**
Most commercially available units are not engineered with low noise and low latency in mind. Typically, one has to choose between low noise units based on the ΣΔ-technology which have a long pipeline delay and units which have a short delay but poor noise performance. By moving the converters away from the noisy backplane buses one can provide them with clean regulated power.

iii) **Inadequate throughput:**
A solution that is based on multiple boards talking to a local bus such as VME has a limited data throughput since the online controls processor has to perform a scatter-gather-read at every processing cycle. This also adds significant delays and reduces the time the processor has to crunch the data. It would be better to assemble all the ADC data into a single block before pushing it into the processor. On the output side the data is preferably sent out as a single block and distributed between the different DACs by hardware.

iv) **Limited timing support:**
Most commercial converters support an external clock input. In order to synchronize the converters with UTC the processor has to start the clock on the 1pps boundary and hope that the converter keeps counting correctly for days and weeks. Errors can occur without anyone noticing. It is much better to run the converters synchronized with our timing distribution system at all times and push time-stamped data into the processor at a regular rate.

v) **Convoluted data paths:**
In some cases the processor and the converters can not be located close to each other. For example, the QPDs are located in the end stations but need to send their data to the ASC and LSC in the corner station. Currently, the suspension controller reads these channels and sends them to LSC and ASC through reflective memory. If all converters are fiber coupled, they can be located anywhere on site and connect to any other unit on site.

vi) **High costs:**
LIGO deploys about 500 converters per interferometer without counting HEPI and without counting spares and channels that are not used. The price per converter is between $500 and $4000. If we assume an average cost of $700 per channel, the estimated total cost for all 3 interferometers was about $1M (see Appendix A). For advanced LIGO we can expect this number to increase by at least a factor of 2—but probably more considering that HEPI alone adds about 300 converters. We estimate that off-the-shelf converters for advanced LIGO would cost us between $2M and $4M.

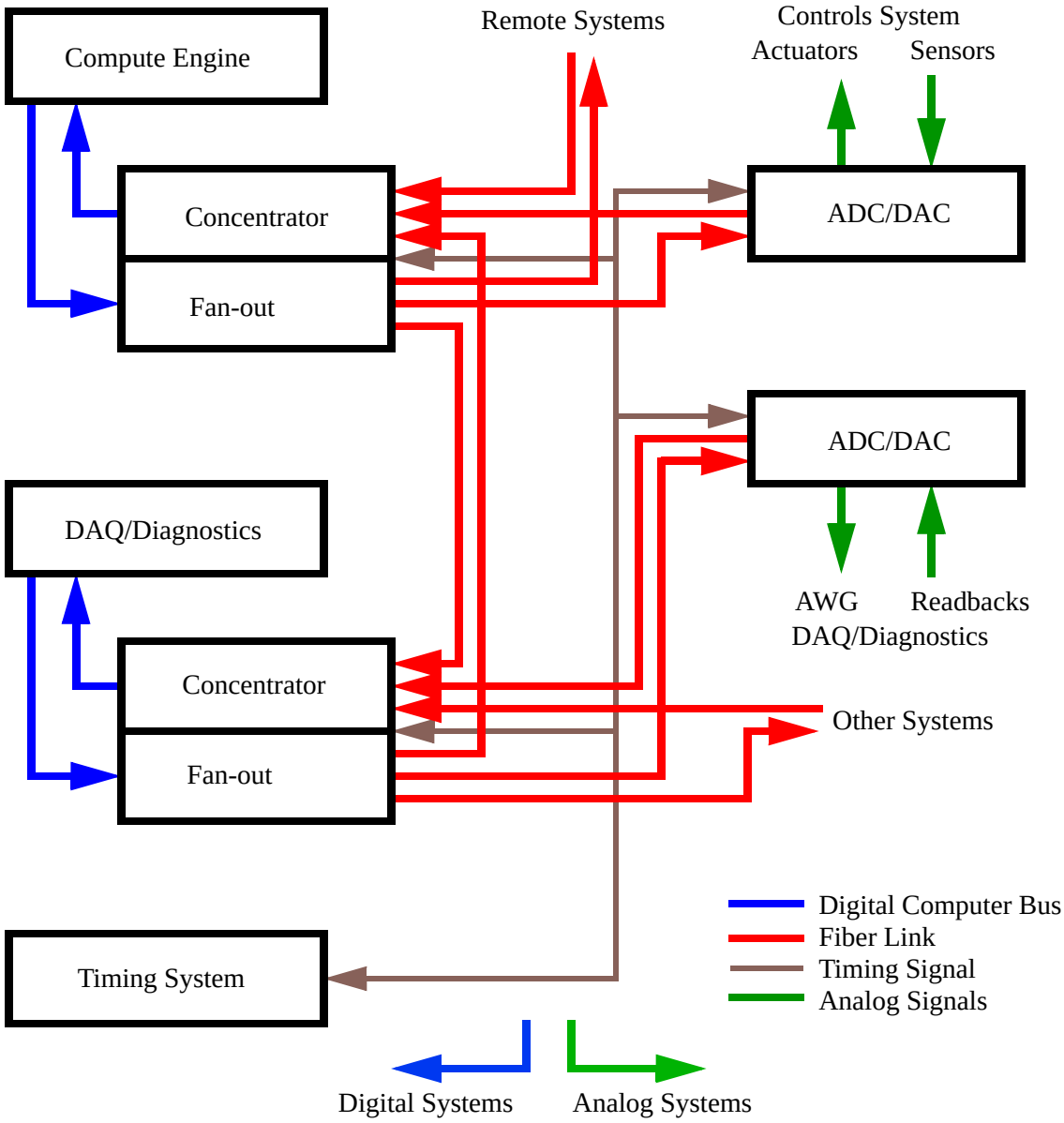

Figure 1: System Overview.

We propose to develop a system which separates the converters from their back-ends (see Figure 1). This will allow us to place converters and analog electronics close to sensors and actuators and avoid long cable runs in analog. We propose to develop data concentrators and data fan-outs that communicate with the converters through fiber optics and transfer data to and from a processor by a fast digital bus. The purpose of the data concentrators will be to collect data from the analog-to-digital converters, assemble them into a single block and push them into the processor. The purpose of the data fan-outs will be to receive data from the processor, split them into individual pieces and send them to the corresponding digital-to-analog converters. This should significantly reduce the communication overhead of the processor and keep the latencies short. The fiber links can also be used for point-to-point communication between the processors.

For example, a front-end controls processor can write its output consisting of control values and data acquisition values to the data fan-out unit which in turn forwards the data acquisition part to a data acquisition processor. Conversely, a diagnostics processor can prepare an arbitrary waveform and send it to the front-end processors through the return link.

An important feature of our converter system is that timing and synchronization with UTC is built-in reliably. The converters are clocked by the new timing system and run synchronized at all times without any processor intervention. The ADC data is time-stamped and sent to the processor at regular intervals —again without burdening the processor. This significantly reduces the timing responsibility of the processor which just has to guarantee that the processed data is ready before it is needed by the DACs. This system would no longer have to rely on the correct counting of electronic pulses over long periods of time. Any timing error would be immediately corrected and reported by the new timing system.

When choosing a low noise ADC or DAC we are limited to what is commercially available. The lowest noise ADCs and DACs are currently based on ΣΔ-modulators. However, they also introduce long pipeline delays and are not suitable for our digital controls system. There are other technologies that avoid the long pipeline delay but typically have worse noise figures. We propose to utilize the over-sampling technique to improve their noise performance. With the current system increasing the sampling rate means increasing the processor load. Since our controls system operate near maximum capacity, this is not possible. In the proposed system we intent to implement decimation and interpolation filters in hardware.

1 Basic Requirements

Here is a list of the fundamental requirements:

- Absolute timing precision relative to UTC: 1 μs.
- Converter range: ±10 V.
- Converter noise: 100–300 nV/√Hz (best effort).
- Latency between converter and processor: < 5 μs.
- No restriction on converter location.
- No electrical connection between converters and processors (fiber links).
- Detection of transmission errors.
- Support for diagnostics.

1 Design Considerations

This section outlines a conceptual design and goes through some of the technical considerations that went into this proposal. An important point is to allow for future growth. We therefore chose a design that is based on programmable logic chips, that has a clearly defined hardware interface between converter units and concentrator/fan-out units, that is fast enough to support increased demands on channel density and that is flexible enough to allow for different topologies as may be dictated by changing requirements for data acquisition and feedback networks.

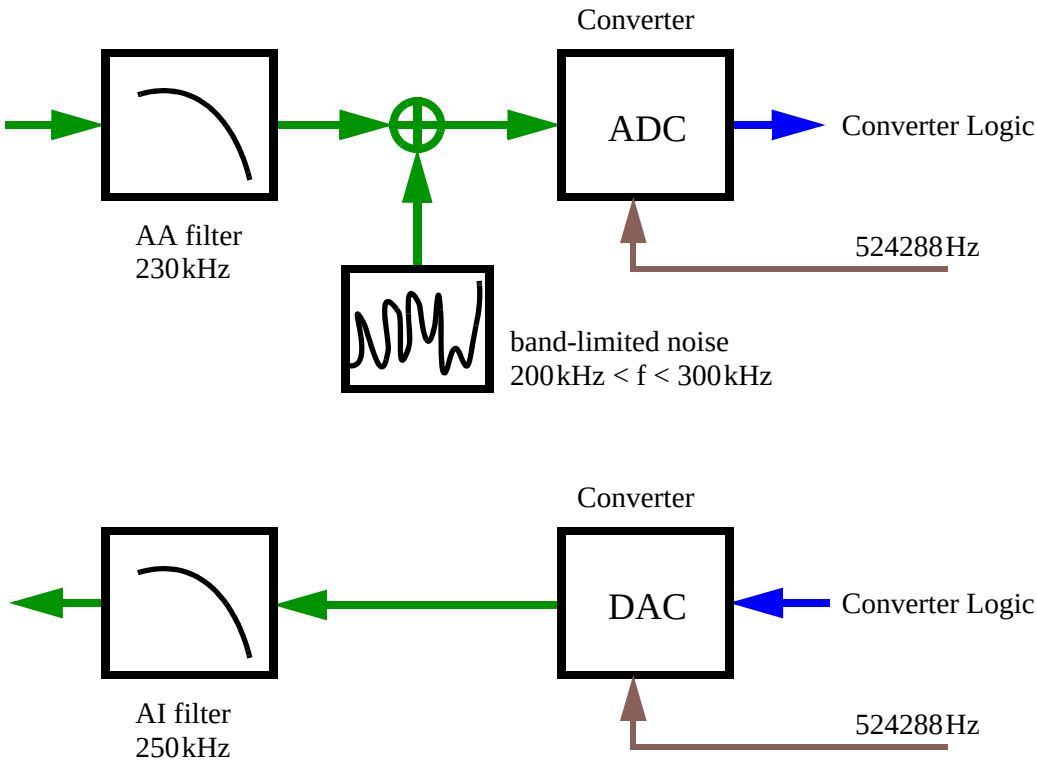

Figure 2: Analog input section (top) and analog output section (bottom).

1.1 ADC

An ADC suitable for our purpose is the AD7679 from Analog Devices. It is a 18-bit design and boosts a dynamic range of 103 dB. Running this device at 524288 Hz (2^{19} Hz) and utilize an input range of ±10 V yields a theoretical noise level of 100 nV$\sqrt{\text{Hz}}$. Figure 2 shows a sketch of the ADC input section. Since the final decimation is done by the converter logic, the anti-aliasing filter can be chosen with a cut-off around 230 kHz. To guarantee that the last bit of the conversion is random a band-limited random noise source can be added to the analog input signal before it is fed into the ADC. To reach the ultimate noise level it is in principle possible to run several ADCs in parallel and add the individual signals in digital.

1.2 DAC

A DAC suitable for our purpose is the PCM1704 from Texas Instruments. This is the same DAC that is used in the modules from FDI. We propose to run them at a rate of 524288 Hz including an 8 time oversampling. Figure 2 shows a sketch of the DAC output section. The converter logic must provide the oversampling as well as a suitable interpolation filter. The cut-off of the anti-image filter can then be chosen around 30 kHz. To reach the ultimate noise level it is in principle possible to run multiple DACs in parallel and add the individual output signals in analog.

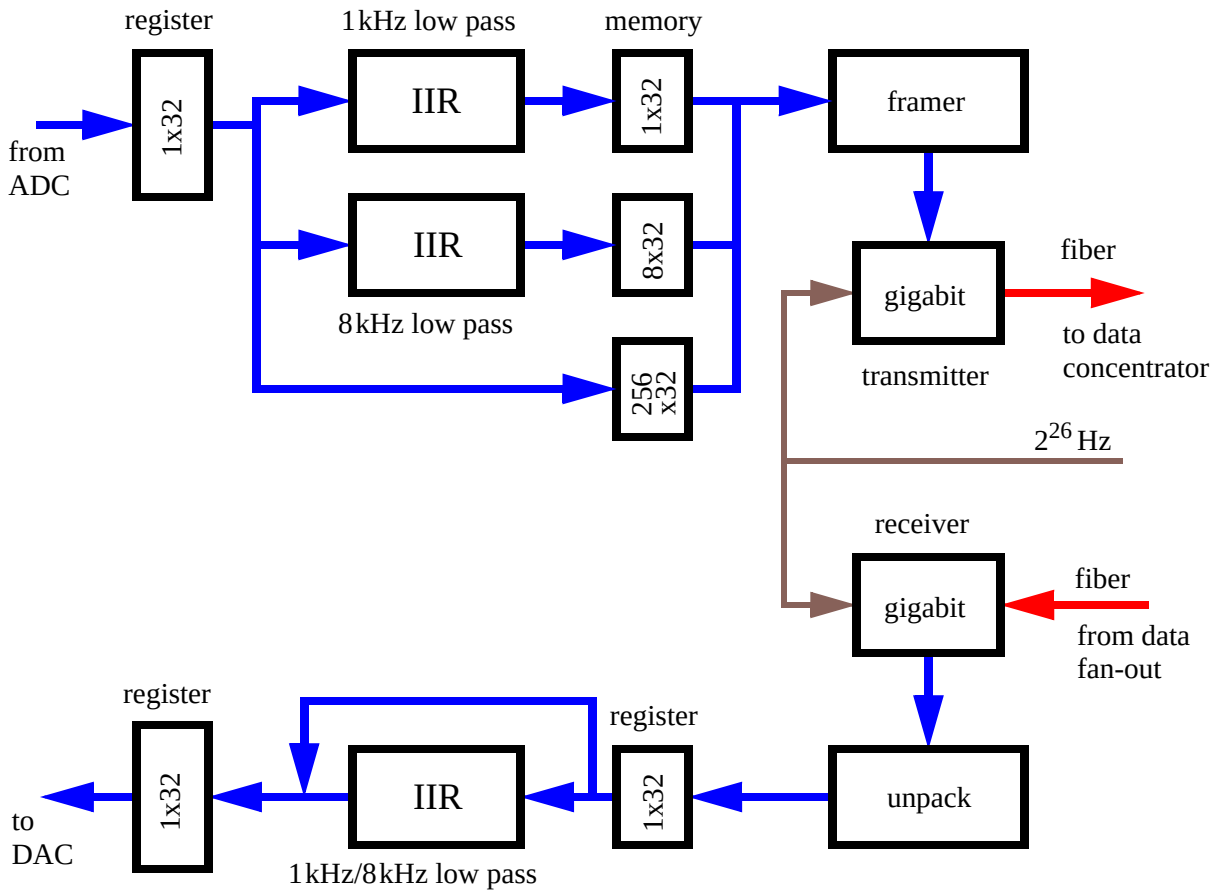

Figure 3: Diagram of converter logic for one input channel (top) and one output channel (bottom).

1.3 Converter Logic

Figure 3 shows a diagram of the converter logic for a single input and output channel. The ADC data is clocked into a 32-bit register. Depending whether the desired output rate is 2048Hz, 16384Hz or 524288Hz the data is fed through a 1kHz low pass filter, an 8kHz low pass filter or bypass path, respectively. In the first and second case the decimation is done by ignoring 255 out 256 samples or 31 out of 32 samples, respectively. The data is then written into a memory block where it waits to be combined with other ADC channels and sent away through the gigabit transmitter. The oversampling architecture has the advantage that multiple sampling rates can be supported simultaneously. In the diagram of Figure 3 these are 2048Hz, 16384Hz and 524288Hz. The first rate might be useful for data acquisition, the second rate for the online controls system and the third rate for diagnostics.

Data received by the gigabit receiver is unpacked and fed to the corresponding DAC channel. A simple register that is read faster than it is written can be used to up-sample the input data to 524288Hz. Depending on the input rate a low pass filter with 1kHz cut-off, a low pass filter with

8kHz cut-off or a bypass is required as an interpolation filter. To minimize delays it is important that the decimation and interpolation filters are implemented as IIR filters.

We propose to usa a field programmable gate array (FPGA) to implement the functionality of the converter logic. For example, the Virtex-II Pro family from Xilinx implements a high number of logic cells, hardware multipliers and gigabit transceivers all in one chip. Further study will be required to determine the exact part number.

1.4 Fiber Link

1.4.1 Hardware Layer

Gigabit receivers can operate with a rate anywhere between 600Mb/s and 10Gb/s. We propose to run our transmitters at a multiple of the timing clock. Since there is a 20% overhead in the encoding scheme, the bit rate that is closest to gigabit ethernet is 10×2^{27} Hz ≈ 1.342 GHz. A suitable optical transceiver is the HFBR-5710L (multi-mode fiber, up to 500m) and the HFCT-5710L (single mode fiber, up to 10km) from Agilent. Both of these devices are compliant with the SFP (small form factor pluggable) standard and are hot pluggable. The maximum data rate through such a fiber link will be approximately 100MB/s.

1.4.2 Protocol Layer

The most common encoding scheme for gigabit links is called 8B/10B. Eight data bits are encoded as 10 bits so that during transmission the disparity between zeros and ones is minimized. This code also allows for additional control characters that can be used to indicate a start of frame and an end of frame. A special comma character is used to align the bit stream to a byte boundary. Most gigabit serializer/deserializer devices support this encoding scheme by default and also support the calculation of a cyclic redundant checksum (CRC) in hardware.

We propose to make use of the same encoding scheme and loosely follow the fibre channel convention for start of frame, end of frame and idle sequences. These are 4 byte sequences that fit well with a protocol which is based on 32 bit words. A data frame then consist of a start of frame, the payload (a series of 32 bit words), the CRC and the stop of frame.

1.4.3 Packet Definition

Packet format: TBD.

1.5 Data Concentrator and Fan-Out

A data concentrator collects data from multiple sources such as multiple ADC converter units and assembles them into a single data block. The data block is then shipped to a processor through the processor interface or any other unit through a fiber link port. A data fan-out unit works in the reverse direction. Data that is received from the processor though the processor interface is sent to one or multiple DAC converter units. Data fan-outs can be linked to other data concentrators but care must be taken to not exceed the maximum allowed latency.

1.5.1 Latency Rules

TBD.

1.5.2 Packet Switching Rules

TBD.

1.5.3 Configuration

TBD.

1.6 Processor Interface

We propose to use the front panel data port (FPDP) to transport data between the data concentrator/fan-out and the processor. FPDP is a 32 bit unidirectional bus with a clock rate of up to 40 MHz—facilitating a maximum transfer rate of 160 MB/s. There is also a serial version of FPDP which might provide a better form factor for the connectors.

We propose to use fixed size repeating frame data with a sync pulse on the last word. For a front-end processor which works at a 16384 Hz sampling rate one frame is transmitted and received every 61 µs. Similarly, a front-end which works at a 2048 Hz sampling rate will receive and send one frame every 488 µs.

1 Advanced Features

The features in this section are meant to be ideas how the proposed system can be expanded in the future. Using a large FPGA as the main logic core makes it possible to add future expansions by reprogramming. In particular, extensions of the link protocol and improvements in the switching rules should be easy to add at a later date. The proposed design does not depend on a particular ADC or DAC chip and a future redesign of the converter unit will be able to implement improvements in converter technology transparently.

1.1 End Station Processors

The only truly fast feedback signal of the end station suspension processor comes from the LSC which is located in the corner station. The fiber links of the new system would make it straight forward to move the suspension processor into the corner station. This is even more true for the DAQ channels or any other slow feedback system like HEPI. This means all processing engines can be located in the corner station and only the analog electronics with their converter units would remain in the end station.

Since the signal travel time in a fiber to the end stations is about 20 µs, this arrangement would add a full clock cycle delay in both the sensing path and the actuator path. To reduce the round-trip delay by 2 one could run the end stations with an offset of exactly half a clock cycle (about 30.5 µs).

1.2 Fast Feedback Networks

Some of the fast feedback paths that are currently implemented in analog—such as the common mode servo and the mode cleaner servo—might be considered for being implemented digitally in advanced LIGO. Assuming the common mode servo has a unity gain frequency around 25 kHz every 1 µs of delay will remove 9° of phase margin. This will most likely make it impossible to use the same converter units, data concentrators/fan-outs and processors as for the slower systems.

However, implementing fast ADCs, hardware IIR filters and fast DACs all on one board would make it possible to implement faster loops in digital. Running at a sampling rate of 524288 Hz the delays in the system would add up to about 2.5 clock cycles or about 45 degree of phase margin. One half cycle delay is simply from the sample-and-hold, another delay close to a full cycle is due to the conversion delay and another cycle will be needed to calculate the filter response. Further reduction of the phase margin will come from the anti-aliasing and the anti-image filters. A feedback loop like that could be made stable but a more comfortable solution would be to reduce the delay by half by increasing the sampling rate by 2. Hence, the common mode servo could be implemented digitally with a sampling rate of at least 2^{20} Hz (1MHz), whereas the mode cleaner servo would require a sampling rate of at least 2^{22} Hz (4MHz). This should be possible with a modern FPGA. A gigabit link will still be useful to send data to the data acquisition system and receive data from the diagnostics system.

1.3 Support for Heterodyning

Another technique that has proven useful in recording the anti symmetric port signal at the free-spectral-range of the arm cavity is to heterodyne the data. Since a sampling rate of 524288 Hz will cover the first 6 multiples of the free-spectral-range frequency, support for heterodyning might be build directly into the converter units. But, even if not, one should be able to avoid extra converters.

1.4 Integration with the Slow Controls System

One of the problems in LIGO is that it is impossible to record all the slow controls signal at a rate of 16 Hz. The main problem is that it is very inefficient to collect the data through ethernet network connections one signal at the time. Another problem is that the converters and binary IO channels of the slow controls system are not synchronized by our timing system. All these problems could be solved by synchronizing the front-ends of the slow controls system with our timing system and by sending the gathered data through one of the new fiber links directly to the data acquisition system.

1.5 Advanced Diagnostics Functions

The new system will make it possible to support an arbitrary waveform generator with higher sampling rate which can send its output directly to any DAC channel. The signal could be added to a controls signal by the converter unit before it is written to the DAC. Similarly, it could be added to the signal read from an ADC—making it possible to implement a simple loop back test.

To test the input path the new converter units could also support a pattern generator that can replaces the ADC signal with a well-known one. If a converter unit supports both ADCs and DACs, a loop back test can also be implemented in analog by switching the ADC inputs to one of the DAC outputs.

1 MODULAR DESIGN

The design of a converter box shall include the following features:

i) Modular design housed in a 1U high 19" rack-mountable enclosure,
ii) Front-panel connectors for analog and binary input/output lines,
iii) Back-panel connectors for power, timing and fiber connection, and
iv) Up to 4 optional modules to support ADCs or DACs.

A sketch is shown in Figure 4. The modules use 4 PMC-type high-density connectors with 64 pins each (AMP 120521-1 and 120527-1): 2 connectors to support the front-panel, 1 connector to support power and 1 connector to link to the FPGA which controls the gigabit interface.

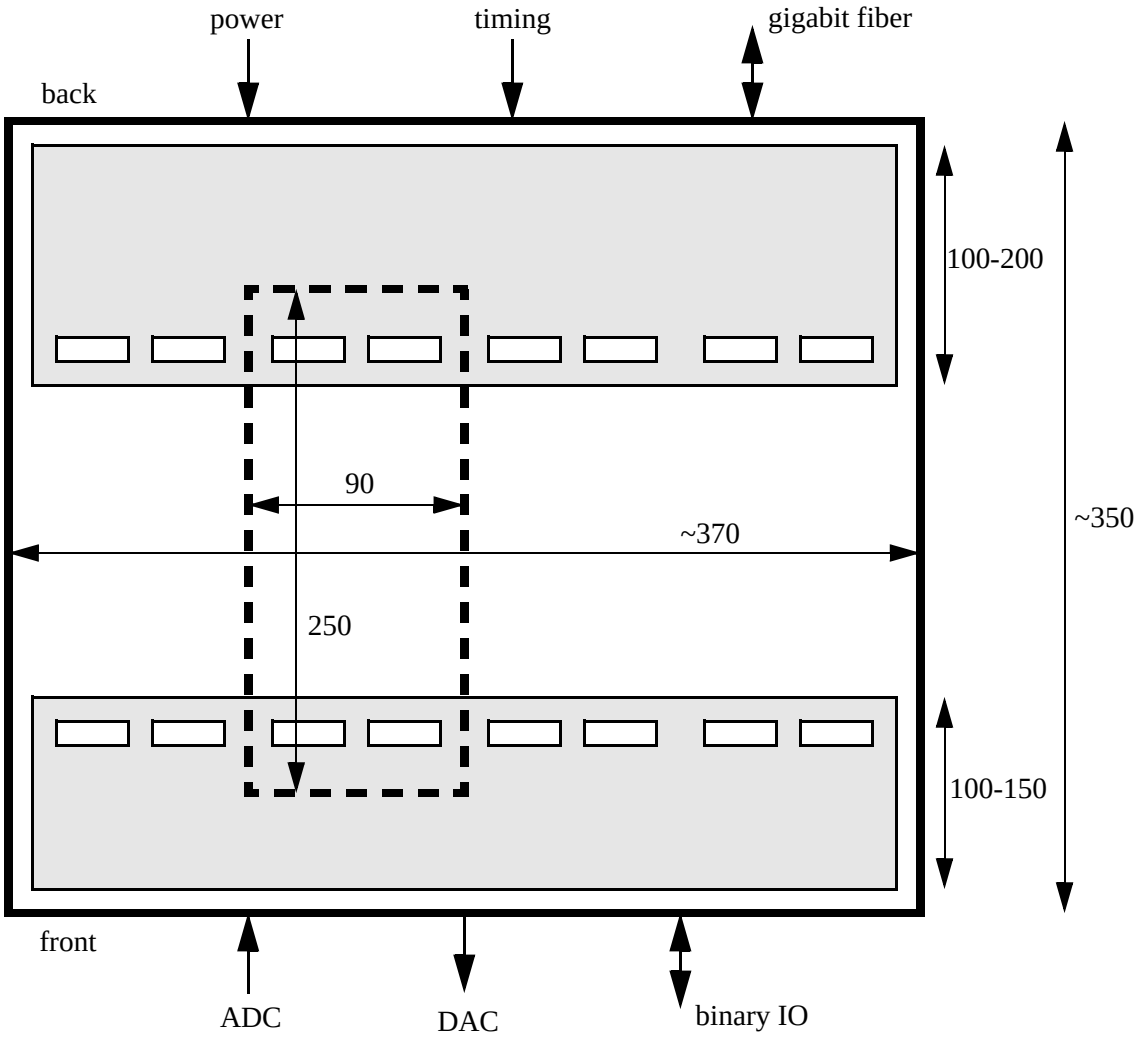

Figure 4: Modular design of a converter box (top view).

We envision that the following modules might be useful:

i) An 8 input ADC module with 16 binary outputs for switching whitening filters,
ii) An 8 output DAC module with 16 binary outputs for switching dewhitening filters,
iii) A low noise 1 or 2 input ADC module (with multiple ADCs per channel) with 4 or 8 binary outputs for switching whitening filters,
iv) A low noise 1 or 2 output ADC module (with multiple DACs per channel) with 4 or 8 binary outputs for switching dewhitening filters,
v) A mixed 4 input and 4 output ADC/DAC module with 16 binary outputs for switching (de)whitening filters,
vi) A generic binary input/output module with up to 128 channels, and
vii) A universal IO module for the slow controls supporting 1 or 2 standardized high-density interconnects.

The PCB in the back would contain the power regulators, the timing system with a 2^n Hz oscillator clock, the interface to the FPGAs on the daughter modules and the interface to the computer. Initially, we propose that the computer interface supports a parallel FPDP, a 100baseT ethernet connector and a serial gigabit link which can be configured to different data rates and standards by changing an oscillator. The serial gigabit link may support a proprietary protocol using the 2^n Hz clock, gigabit Ethernet, serial FPDP or any other serial 10B/8B standard that is compatible with the chosen FPGA. The back panel also contains a JTAG boundary scan connector to (re-)program FPGAs. For low noise operation any interface that is not needed can be powered down.

The PCB in front contains the front-panel connectors and the interface to the ADCs and DACs on the daughter boards. Multiple connector interfaces can be supported by inter-changeable front-panels and front PCBs. The daughter boards typically would implement an FPGA near the rear board connectors and ADCs, DACs and analog electronics near the front.

APPENDIX A SURVEY OF CURRENT CONVERTERS

This is an estimate on how many converters are currently installed by LIGO. It does not try to count converters that are available but not used.

Table 1: Converter Count

System	Estimated number per ifo
DAQ	250
LSC	30
ASC	70
SUS	180
Total/ifo	530
SEI	300(?)

This is a list of converter boards currently installed at LHO and LLO. These numbers do not include HEPI, spares or the development costs of the FDI DAC (~$100k).

Table 2: Installed Converter Boards

Board	Type	Channels	price [k$]	H1	H2	L1	total	ext. [k$]
ICS-110B	ADC	32	11	12	12	12	36	396
Pentek	ADC/DAC	8/8	8	21	24	21	66	528
ICS-115	DAC	4–32	5–12	3	3	3	9	66
ISC-130	ADC	8	8	1	1	1	3	24
FDI	DAC	8	8	3	3	3	9	72
total				40	43	40	123	1086