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Laser Interferometer Gravitational Wave Observatory (LIGO) Project

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Proposal for a new Timing Distribution System

Basic Goals:

The goals of the new timing distribution system are:

- Provide a time stamp aligned with UTC to within better than 1 μs.
- Provide a means to synchronize the front-end ADCs and DACs in hardware.
- Provide a reliable link to distribute the timing signal from a single source.
- Provide the capability to use commercial GPS units or an atomic clock as the timing standard.
- Provide diagnostics to monitor the status of the timing system.

Design Considerations:

All commercial time standards output a 1 pps (one pulse-per-second) signal that can be used to synchronize the LIGO timing system. The fundamental clock frequencies for the LIGO ADCs and DACs are derived from a 2^n Hz clock. We propose to use dual master oscillators based on oven-stabilized low noise crystals (OCXO) that run at 2^{25} Hz (33.554432 Hz) and are locked to a 1 pps signal using a phase-locked loop (PLL). One of these master oscillators is locked to a commercial GPS clock whereas the other is locked to an atomic clock. One of the oscillators is used as the primary clock to drive the timing distribution system whereas the secondary one is used as a diagnostics to monitor the accuracy of the primary one. Either oscillator can be used as the primary clock.

To implement a reliable link for timing distribution we propose to use a fiber coupled timing signal that runs at 2^{23} Hz (8.388608 Hz). The timing signal is a square wave signal with 50% duty cycle using the positive edges for synchronization. To mark the location of the 1 pps the two closest negative edges to the positive edge aligned with the 1 second mark are moved inwards making the pulse starting at the 1 second mark half as long as the others and the one before 50% longer than the others (see timing diagram). Basically, the clock signal is determined by the positive edges whereas the interval length between the negative edges determines the location of the 1 pps. This type of timing signal has 50% duty cycle overall and is well suited to be distributed through an AC-coupled fiber link. Since the 1 pps signal is modulated onto the main clock signal only a single fiber link is required.

We propose to use a return link for diagnostics purposes. This return signal is the same type of clocking signal but is derived from the slave clock, therefore, indicating the exact state of the slave clock. Also, this makes it possible to daisy-chain multiple timing slaves within the same crate. The timing signal from the master connects to the input of the first board, its output

connects to the second board and so on. The output of the last board is then returned to the master as a diagnostics. The diagnostics return link is used to (a) determine that the slave(s) is(are) locked to the master and to (b) measure the timing delay in the fiber link. We propose to implement a time adjust on the master side that allows the clock to be shifted ahead. This will compensate for the time delay in the fiber and guarantee accurate timing of the slave. Since the returned diagnostics signal has passed through the fiber delay twice, it is straight forward to determine the delay and further diagnostics can be implemented to check that the time adjustment is half the total round-trip delay. We propose to use the period of the 8 MHz clock, i.e., 119.2 ns, as the smallest time step for time adjustments and time interval measurements.

Since each timing slave needs its own clock signal feed with time adjustment and diagnostics we propose to use a separate timing distribution board that sits between the master oscillator and the slave clocks. This fan-out module would basically look like a slave clock, meaning multiple timing distribution modules can be daisy-chained to give a larger fan-out. It would further provide multiple outputs to synchronize slave modules in the LVEA or any of the out-buildings. Both single-mode fiber and multi-mode fiber are supported for long range (>1 km) and short range (<1 km), respectively.

A slave module implements a crystal oscillator (VCXO) running at 2^{25} Hz that is locked to the positive edges of the timing distribution signal using a PLL. It regenerates the timing distribution signal from its internal clock and compares the location of the 1 pps mark to the one in the received timing signal. If the 1 pps marks differ for a couple of consecutive seconds the internal counters are zeroed with the external 1 pps and an error flag is set. It is envisioned that slave modules come in different variety depending on the ADC and DAC modules they are driving. A slave module will generate all the necessary clock signals for an ADC or DAC from its internal oscillator which should be immune to noise on the timing distribution system.

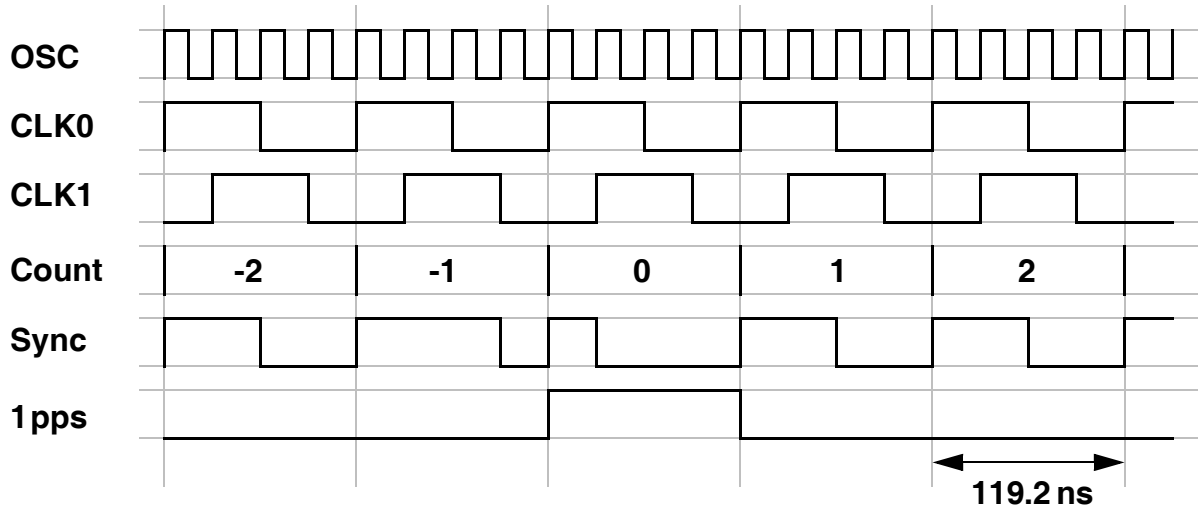

Figure 1: Timing Diagram. The oscillator (OSC) runs at 2^{25} Hz. The timing distribution signal is derived from the Sync signal. All following counts repeat until the next 1 pps.