LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

CALIFORNIA INSTITUTE OF TECHNOLOGY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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Test procedure	LIGO-T030184-A-C	29 July, 2005
ISS board Test Procedure		
Flavio Nocera, Richard Abbott		Richard Abbott Digitally signed by Richard Abbott DN: CN = Richard Abbott, C = US, O = LIGO Reason: I attest to the accuracy and integrity of this document Date: 2005.08.16 11:26:10 -07'00'

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California Institute of Technology
LIGO Project – MS 18-33
Pasadena, CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project – MS 20B-145
Cambridge, MA 01239
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

www: http://www.ligo.caltech.edu/

1 Overview

The following procedure refers to D020241-D, all revisions up to D02.
The board is the Controller for the laser Intensity Stabilization Servo (ISS).

The ISS interfaces with two [four when the Outer Loop is implemented] custom designed photodetector heads (D030452-00-C) for monitoring and control through two DB9 connectors, on the back panel of the chassis.

4-pin LEMO connectors on the front panel are used to interface the ISS with the DAQ system.

2 Test Equipment

The following test equipment is necessary:

Dual DC power supply (capable of ± 24VDC)
Handheld Voltage Calibrator
Scope with scope probe
Dynamic Signal Analyzer (SR785)
Function Generator (DS345)
BNC cables (for transfer function measurements with the SR785)
1 Dual-pin male LEMO to BNC adapter
37 pin male D connector to be used in applying power to device under test (DUT)

3 Test Setup

Establish jumper settings per paragraph 5.0 of this procedure
Apply ± 24VDC using a male 37 pin D-sub connector configured as a test connector.

37 PIN D-SUB CONNECTOR PIN	FUNCTION
Pin 1	+24VDC
Pin 3	-24VDC
Pin 20	Ground

4 Test Overview

The test procedure is divided into the following sections:

Input Power level
This test will verify that the ISS board gets the proper amount of current from the power supply in the two possible test modes.

Servo path Transfer Functions
These tests will verify that the transfer functions implemented by the various stages are the ones expected according with the design.

Saturation Detection
These tests will verify that in event of saturation a 1 second pulse is produced and made available to EPICS.

Monitor and DAQ signal integrity
These tests will verify that signals available for the DAQ and as monitor on the board front panel are an accurate replica of the ones used in the servo.

Filter time response
These two tests will verify the proper behavior of the low pass filters specified in par 5.5.

5 Test procedure

1.0 Jumper normal operating positions (Outer loop disabled)

JP1-**12**	JP2-23	JP3-23	JP4-12
JP5-23	JP6-23	JP7-12	JP8-12
JP9-23	JP10-12		

1.1 Input Power

Supply	Nominal Current	Actual Current	Check if OK
-24 V	600 mA (± 150 mA)		
+24 V	600 mA (± 150 mA)		

By observing the 4 board mounted LEDs (D10, D11, D12, D13) verify that the front panel power switch functions correctly to turn power on and off to the DUT

Check box if OK

There are 4 DB-9 connectors on the front panel of the ISS chassis. These connectors supply power and ground to the remotely located photo-detector modules. A check must be performed to verify that the correct voltages are present on these connectors. The pinout is identical on each DB-9 connector and is pinned as follows:

FUNCTION	PIN
+ 5VDC	1
+15VDC	2
-15VDC	3
Ground	5, 6, 7, 8

Check box if the correct voltages are present on each of the 4 connectors

1.2 Inner Loop Transfer Functions

The SR785, in conjunction with the scope (to avoid taking measurements affected by saturation), will be used to measure the various transfer functions to assess the proper behavior of the DUT.
Set up the SR785 for Transfer Function measurement using 201 points

Inner Loop DC Offset and Oscillation Check

This step verifies that the inner loop op-amps are not oscillating and no significant DC offsets exist (>2mV).

The method for adjusting the DC offset potentiometers for any arbitrary chain of AD-829 op-amps on the ISS board is given next. The method exploits the fact that the AD-829 op-amp is tolerant of continuous short circuit to ground on its output. The example uses the chain of op-amps at the output of the ISS and nulls the offsets back to the point where the servo has an AC coupling point. The same technique can be used at other points in the board provide that the preceding stage is an AD-829.

Starting at the 2-pin Lemo connector associated with the "Current Shunt Drive", insert a spare pin into one pin of the Lemo connector and hook up a Fluke Multimeter to read the voltage with respect to ground. It's a good idea to allow 5 minutes or so for the unit to warm up, and avoid doing the procedure in the presence of large air currents, as these will cause drift.

Start the process by grounding TP2 with a clip lead. Adjust R59 until the "Current Shunt Drive" output is as close to zero as possible. Remove the clip lead and move it back one stage to TP1. Now adjust R6 until the "Current Shunt Drive" output is again as close as possible to zero. Continue this process of grounding, adjusting and measuring working backwards with R2/TP6. With all clip leads removed, R4 can be adjusted without shorting its input, as U3 is AC coupled by C25.

Check box after using the above process to establish the Current Shunt Drive output offset to be within 2mV of zero.
Check box after verifying that all grounding clip leads have been removed.

Record the final DC offset at the "Current Shunt Drive" output. _____VDC

While shorting TP21 and TP5 to ground, measure the DC offset at TP3 and adjust R5 to be as close as possible to zero. Remove the shorting clip from TP21 while temporarily leaving the jumper on TP5 in place.

Adjust R186 to put TP3 as close as possible to zero. Remove the shorting clip lead from TP5 after completion of this step.

Now, with no clip leads on the DUT, adjust R10 until TP3 is as close to possible to zero.

Check box after using the above process to establish the offset at TP3 to be within 2mV of zero.
Check box after verifying that all grounding clip leads have been removed.

Record the final DC offset at TP3. _____VDC

Check box if no oscillations, RF or otherwise are found on:

- All panel mounted DAQ Lemo Jacks
- All BNC panel mounted monitoring points
- DB37 connector pins 5 through 18 and 24 to 30 inclusive
- TP44, TP45, TP47, TP48, TP28, TP5, TP37, TP35, TP27, TP26, TP7

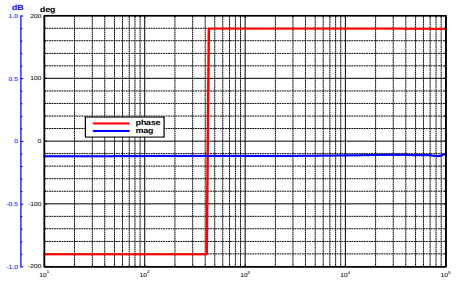
Date _____
Tech _____
Board Serial Number_____

1) Functional check of stages U6, U5, U14, U1, U44C, U44D, U46A and U46B

Input	Output	Vsource	Frequency Span
DB1-4 (+) and DB1-9 (-)	Err Point BNC (JTC1-1) -Inner Loop-PD DC	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check if OK
52.48	Gain (dB) 0 ± 1	Gain (dB)	
	Phase (deg) -180 ± 3	Phase (deg)	
91.2e3	Gain (dB) 0 ± 1	Gain (dB)	
	Phase (deg) 180 ± 3	Phase (deg)	

Transfer Function 1



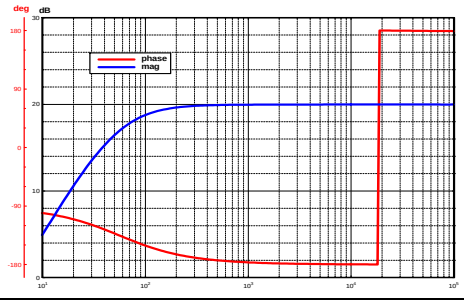
Input	Test Name	Output		Transfer Function	Check if OK
DB1-4 (+) and DB1-9 (-)	1b2	J3-pin3 (IL Sensor PD DAQ)		Same shape as above, gain 20 dB lower	
DB1-4 (+) and DB1-9 (-)	1b3	DB3-pin5		Same as (Transfer Function 1) but with 6 dB of attenuation	
DB1-4 (+) and DB1-9 (-)	1b4	J3-pin2 (IL Sensor PD DAQ)		Same as (1b2) but phase rotated 180 deg	
DB1-4 (+) and DB1-9 (-)	1b5	DB3-pin24		Same as (1b3) but phase rotated 180 deg	

2) Functional check of stages U45, U44A and U44B

Input	Output	Vsource	Frequency Span
DB1-4 (+) and DB1-9 (-)	J3-pin4 (IL Sensor PD DAQ) 	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK
52.48	Gain (dB) 20 ± 2	Gain (dB)	
	Phase (deg) -166 ± 5	Phase (deg)	
91.2e3	Gain (dB) 20 ± 2	Gain (dB)	
	Phase (deg) 180 ± 5	Phase (deg)	

Transfer Function 2



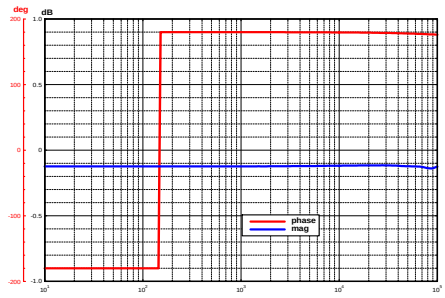
Input		Output		Transfer Function	Check if OK
DB1-4 (+) and DB1-9 (-)		J3-pin1 (IL Sensor PD DAQ)		Same as above, but phase rotated 180 deg	

3) Functional check of stage U11, U4 and U12

Input	Output	Vsource	Frequency Span
DB1-4 (+) and DB1-9 (-)	Test Out Ch2 BNC -Inner Loop- (JTC3-1)	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check if OK
52.48	Gain (dB) 0 ± 1	Gain (dB)	
	Phase (deg) -180 ± 5	Phase (deg)	
91.2e3	Gain (dB) 0 ± 1	Gain (dB)	
	Phase (deg) 180 ± 5	Phase (deg)	

Transfer Function 3

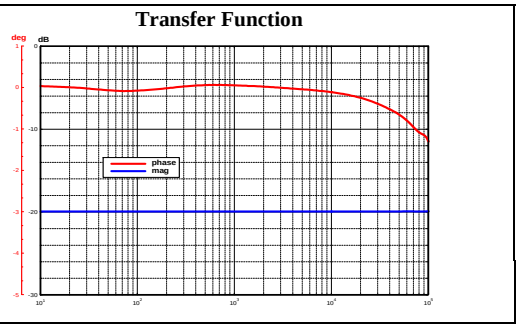


Input		Output		Transfer Function	Check if OK
DB1-4 (+) and DB1-9 (-)		Test Ch 1 BNC		Same as above, but phase rotated 180 deg	

5) Functional check of stages U49 and U30

Input	Output	Vsource	Frequency Span
Analog Input IL (J4)	"Test Ch1" BNC	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check if OK
52.48	Gain (dB) -20 ± 1	Gain (dB)	
	Phase (deg) 180 ± 3	Phase (deg)	
91.2e3	Gain (dB) -20 ± 1	Gain (dB)	
	Phase (deg) 180 ± 5	Phase (deg)	

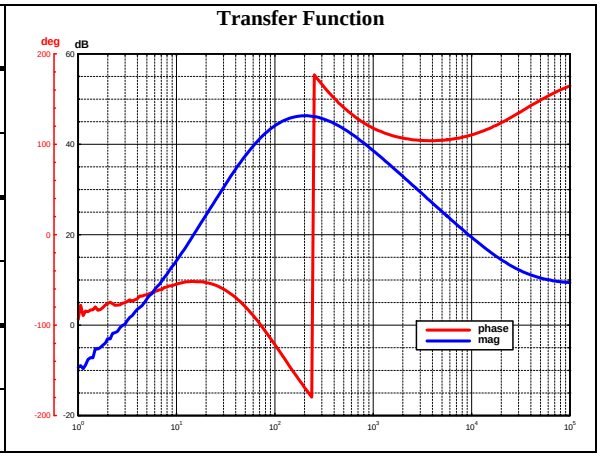


Repeat the measurement after moving JP5 from 23 to 12.
The output should go to zero (huge negative number in dB). Check Box if OK ☐
Put the jumper back on 23.

10) Functional check of stages U3, U2, U7, U13, U9, U10

Input	Output	Vsource	Frequency Span
Analog In IL (J4)	"Current Shunt Mon" BNC	**1** mV	**1**Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK
10	Gain (dB) 14.3 ±3	Gain (dB)	
	Phase (deg) 118 ± 5	Phase (deg)	
398.1	Gain (dB) 44 ± 2	Gain (dB)	
	Phase (deg) 154 ± 5	Phase (deg)	
94.4e3	Gain (dB) 9.9 ± 2	Gain (dB)	
	Phase (deg) 162 ± 5	Phase (deg)	



Repeat the measurement applying a DC voltage to "Rack Interface" (pin 14+, pin 32 -) – the gain control input - using a voltage source. Application of +/- 10VDC to the gain control input should result in +/- 20dB of gain change.

Check if +/-20dB (+/-1dB tolerance) gain variation is observed

10b) Functional check of stages U43C, U43D, U47A and U47B

Input		Output	Transfer Function		Check if OK
Analog In IL (J4)	10b1	DB3-pin8		Same as (10)	
Analog In IL (J4)	10b2	DB3-pin27		Same as (10b1) but phase rotated 180 deg	

Repeat the measurement increasing the source level up to 100 mV.
Although the measurement is affected by saturation, this is no concern here.
The objective is to see both LEDs light up and flicker.

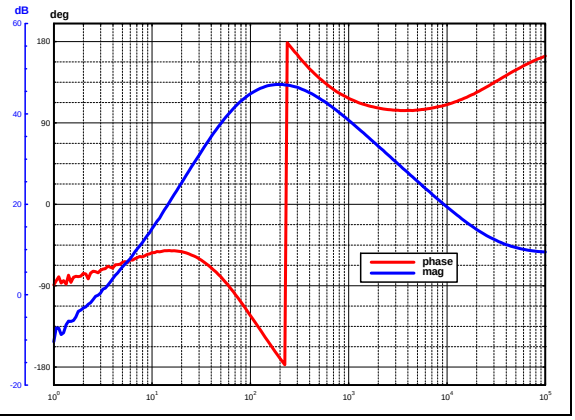
Bring the source level back to 1mV. Check Box if OK

11) Functional check of stages U34C and U34D

Input	Output		Vsource	Frequency Span
Analog In IL (J4)	J5-pin3 (ACT DAQ HF)		1 mV	1Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK
10	Gain (dB) 14.3 ±3	Gain (dB)	
	Phase (deg) -58± 5	Phase (deg)	
398.1	Gain (dB) 45.3 ± 2	Gain (dB)	
	Phase (deg) 144 ± 5	Phase (deg)	
94.4e3	Gain (dB) 9.9 ± 2	Gain (dB)	
	Phase (deg) 163 ± 5	Phase (deg)	

Transfer Function

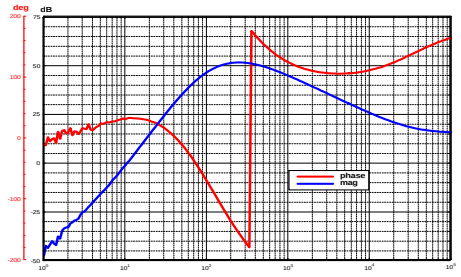


11b)

Input		Output	Transfer Function		Check if OK
Analog In IL (J4)	11b1	J5-pin2 (ACT DAQ HF)		Same as (11) but phase rotated 180 deg	

12) Functional check of stages U48, U43A and U43B

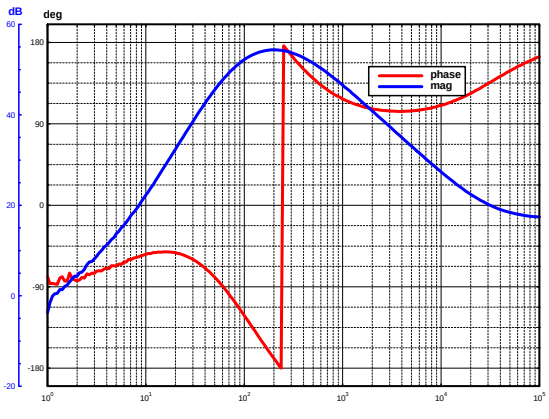
Input	Output	Vsource	Frequency Span
Analog In IL (J4)	DAQ "Current Shunt"  Pin 4	1 mV	1Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK	Transfer Function
53.08	Gain (dB) 35 ± 2	Gain (dB)		
	Phase (deg) -16 ± 5	Phase (deg)		
94.4 e3	Gain (dB) 15.9 ± 2	Gain (dB)		
	Phase (deg) 164.1 ± 5	Phase (deg)		

Input	Test Name	Output	Transfer Function		Check if OK
Test In	12b1	DAQ "Current Shunt" Pin 1		Same as above (12) but phase rotated 180 deg	

13) Functional check of stage U22

Input	Output		Vsource	Frequency Span
Analog In IL (J4)	J1-pin1 (Current Shunt Drive)		1 mV	1Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK	Transfer Function
10	Gain (dB) 23.9 ± 3	Gain (dB)		
	Phase (deg) -58 ± 5	Phase (deg)		
398.1	Gain (dB) 52 ± 3	Gain (dB)		
	Phase (deg) 154 ± 5	Phase (deg)		
94.4e3	Gain (dB) 18 ± 3	Gain (dB)		
	Phase (deg) 165 ± 5	Phase (deg)		

Repeat the measurement after moving JP3 from 23 to 12.
The output should go to zero (great negative number in dB). Check Box if OK ☐
Put the jumper back on 23.

13b)

Input	Output		Vsource	Check if OK
Test In	J1-pin2 (Current Shunt Drive)		Same as above but phase rotated 180 deg	

5.3 Inner Loop Monitor PD (and associated monitoring points) Transfer Functions

1) Functional check of stages U53, U54, U56, U51C, U51D, U52A, U52B

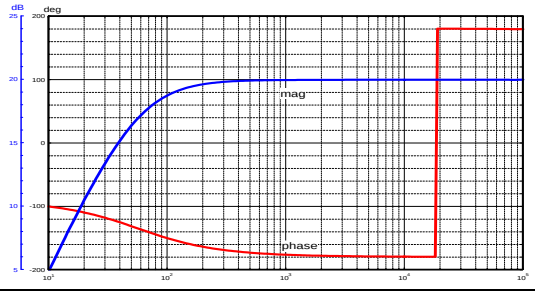
Input	Output	Vsource	Frequency Span
Rear Panel DB-9 "Monitor PD-IL" Pin4 (+), Pin9 (-)	Rear Panel BNC "Monitor PD-IL-PD DC"	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK	Transfer Function
52.48	Gain (dB) 0 ± 1	Gain (dB)		
	Phase (deg) -180 ± 3	Phase (deg)		
91.2e3	Gain (dB) 0 ± 1	Gain (dB)		
	Phase (deg) 180 ± 3	Phase (deg)		

Input	Test Name	Output		Transfer Function	Check if OK
Same as above	1b1	J7-pin3 (IL Mon PD DAQ)		Same shape as above (1), gain 20 dB lower	
Same as above	1b2	DB3-pin6		Same as (1) but with 6 dB of attenuation	
Same as above	1b3	J7-pin2 (IL Mon PD DAQ)		Same as (1b1) but phase rotated 180 deg	
Same as above	1b4	DB3-pin25		Same as (1b2) but phase rotated 180 deg	

2) Functional check of stages U55, U51A, U51B

Input	Output	Vsource	Frequency Span
Rear Panel DB-9 "Monitor PD-IL" Pin4 (+), Pin9 (-)	Front Panel "DAQ-Monitor PDs-IL" 	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK	Transfer Function
52.48	Gain (dB) 20 ± 2	Gain (dB)		
	Phase (deg) -165 ± 5	Phase (deg)		
91.2e3	Gain (dB) 20 ± 2	Gain (dB)		
	Phase (deg) 180 ± 5	Phase (deg)		

Input		Output		Transfer Function	Check if OK
Same as above	2b1	J7-pin1 (IL Mon PD DAQ)		Same as (2) but phase rotated 180 deg	

1.3 Filter time response

Evaluate the step response of the LP filters implemented with U8 and U50.
A Function Generator and a two-channel scope are needed.
Apply the output of the Function Generator as input to the board where indicated and to channel 1 of the scope.
Feed the output of the filter to channel 2 of the scope.

Use the suggested settings

Function Generator

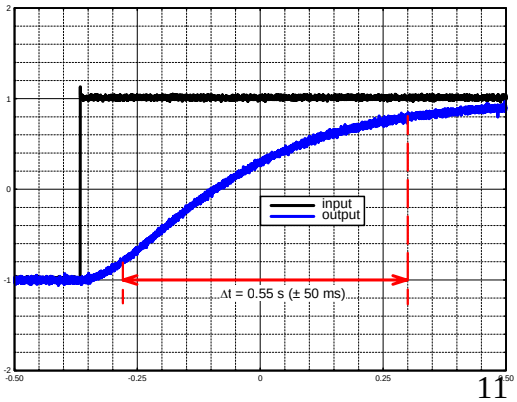
Function	Square wave
Freq	0.03 Hz
Amplitude	2 Vpp

Scope (both channels)

Coupling	DC
Vertical Axis	1V/div
Horizontal Axis	1 s/div

Set up the scope for a single shot, triggering on the rising front of channel 1 (and setting the trigger level just above 0 V).
There could be the need of shifting the two signals on the Y-axis relatively to each other in order to overlap the traces.
Once the waveforms are acquired, use the vertical cursors and place the first of them at where the output is 0.8 V, the second at –0.8 V instead.

Measure the time delta between the cursors (using the scope's utility for it).



Filter1)

Input	Output	Nominal rise time	Actual rise time	Check if OK
Rear Panel "Rack Interface" DB-37 Pin13 (+), Pin31 (-)	Front Panel "LF Act Drive"  Pin1	0.5 s (± 0.1 s)		
Rear Panel "Rack Interface" DB-37 Pin13 (+), Pin31 (-)	Front Panel "LF Act Drive"  Pin2	5.1 s (± 0.1 s)		

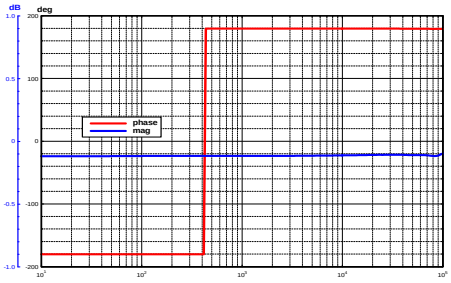
5.5 Outer Loop Transfer Functions

1) Functional check of stages U20, U19, U27, U28C, U28D, U23A and U23B

Input	Output	Vsource	Frequency Span
DB2-4 (+) and DB2-9 (-)	Err Point BNC (JTC5-1) -Outer Loop-	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK
52.48	Gain (dB) 0 ± 1	Gain (dB)	
	Phase (deg) -180 ± 5	Phase (deg)	
91.2e3	Gain (dB) 0 ± 1	Gain (dB)	
	Phase (deg) 180 ± 5	Phase (deg)	

Transfer Function 1



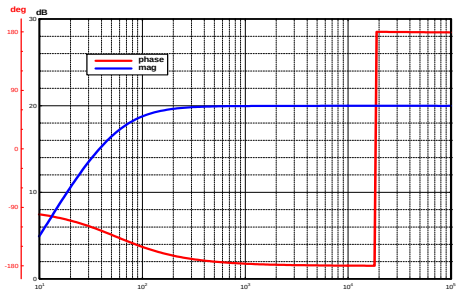
Input	Test Name	Output		Transfer Function	Check if OK
DB2-4 (+) and DB2-9 (-)	1b2	J2-pin3 (OL Sensor PD DAQ)		Same shape as above, gain 20 dB lower	
DB2-4 (+) and DB2-9 (-)	1b3	DB3-pin10		Same as (Transfer Function 1) but with 6 dB of attenuation	
DB2-4 (+) and DB2-9 (-)	1b4	J2-pin2 (OL Sensor PD DAQ)		Same as (1b2) but phase rotated 180 deg	
DB2-4 (+) and DB2-9 (-)	1b5	DB3-pin29		Same as (1b3) but phase rotated 180 deg	

2) Functional check of stages U29, U28a, U28b

Input	Output	Vsource	Frequency Span
DB2-4 (+) and DB1-9 (-)	J2-pin4 (OL Sensor PD DAQ) 	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK
52.48	Gain (dB) 20 ± 2	Gain (dB)	
	Phase (deg) 13 ± 5	Phase (deg)	
91.2e3	Gain (dB) 20 ± 2	Gain (dB)	
	Phase (deg) 0 ± 5	Phase (deg)	

Transfer Function 2



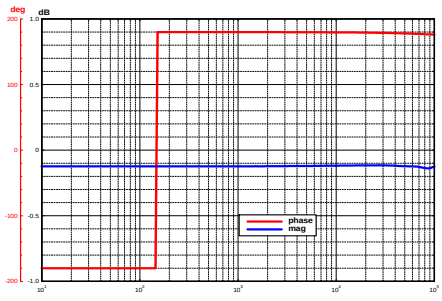
Input		Output		Transfer Function	Check if OK
DB2-4 (+) and DB2-9 (-)		J2-pin1 (OL Sensor PD DAQ)		Same as above, but phase rotated 180 deg	

3) Functional check of stage U26

Input	Output	Vsource	Frequency Span
DB2-4 (+) and DB2-9 (-)	Test Out Ch2 BNC -Outer Loop- (JTC6-1)	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK
52.48	Gain (dB) 0 ± 1	Gain (dB)	
	Phase (deg) -180 ± 5	Phase (deg)	
91.2e3	Gain (dB) 0 ± 1	Gain (dB)	
	Phase (deg) 180 ± 5	Phase (deg)	

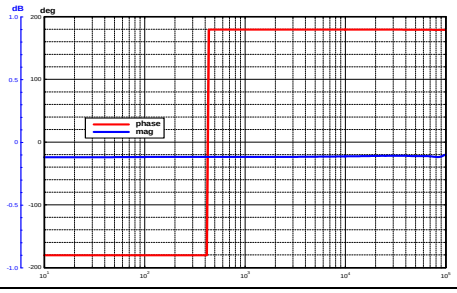
Transfer Function 3



5.6 Outer Loop Monitor PD (and associated monitoring points) Transfer Functions

1) Functional check of stages U64, U63, U59, U61C, U61D, U58A, U58B

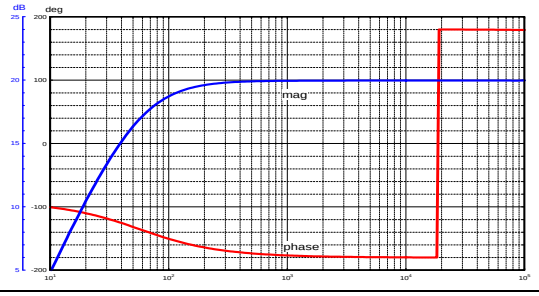
Input	Output	Vsource	Frequency Span
Rear Panel DB-9 "Monitor PD-OL" Pin4 (+), Pin9 (-)	Rear Panel BNC "Monitor PD-OL-PD DC"	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK	Transfer Function
52.48	Gain (dB) 0 ± 1	Gain (dB)		
	Phase (deg) 180 ± 3	Phase (deg)		
91.2e3	Gain (dB) 0 ± 1	Gain (dB)		
	Phase (deg) 180 ± 3	Phase (deg)		

Input	Test Name	Output		Transfer Function	Check if OK
Same as above	1b1	J8-pin3 (OL Mon PD DAQ)		Same shape as above (1), gain 20 dB lower	
Same as above	1b2	DB3-pin11		Same as (1) but with 6 dB of attenuation	
Same as above	1b3	J8-pin2 (OL Mon PD DAQ)		Same as (1b1) but phase rotated 180 deg	
Same as above	1b4	DB3-pin30		Same as (1b2) but phase rotated 180 deg	

2) Functional check of stages U62, U61A, U61B

Input	Output	Vsource	Frequency Span
Rear Panel DB-9 "Monitor PD-OL" Pin4 (+), Pin9 (-)	Front Panel "DAQ-Monitor PDs-OL" 	100 mV	10Hz – 100 kHz

Freq (Hz)	Theoretical values	Measured values	Check OK	Transfer Function
11.22	Gain (dB) 17 ± 2	Gain (dB)		
	Phase (deg) -135 ± 5	Phase (deg)		
91.2e3	Gain (dB) 20 ± 2	Gain (dB)		
	Phase (deg) -175 ± 5	Phase (deg)		

Input		Output		Transfer Function	Check if OK
Same as above	2b1	J8-pin1 (OL Mon PD DAQ)		Same as (2) but phase rotated 180 deg	

5.7 Outer Loop DC Offset and Oscillation Check

Verify that the outer loop op-amps are not oscillating and that they don't have significant DC offsets (>20mV)

Check box after using each op-amps associated offset trim potentiometer, to establish each op-amp's offset to be within 20mV of zero. Applies to U18, U21, U17, U57

Check box if no oscillations, RF or otherwise are found on U57-Pin6, TP36, TP18, TP12, TP14, Outer Loop "Test Out Ch1" BNC using an oscilloscope

5.8 **Tests of Saturation Monitors**

There are three separate saturation monitors used on the ISS board. The first is on the Inner loop photodetector input, and is AC coupled. It's function is to catch sharp pulses that may be causing saturation events on the early stages of the ISS op-amps, but due to the filters later on the board, the events may not be observable as saturations at the current shunt output.

A second saturation monitor looks for saturation events at the output of the servo just prior to the current shunt drive output.

The third monitor functions exactly the same as the inner loop photodetector monitor and is AC coupled. Its function is fast glitch detection at the plane of the outer loop photodetector input circuitry.

Once the threshold for a glitch is exceeded in any of these monitors, an approximately 1 second pulse is generated and presented as an output from the board.

All three of these monitors are tested by the application of square wave pulses to various inputs on the ISS board, and observation of the ~1sec pulse that is generated as a response. The following details the method:

A 0.2 Hz 50% duty cycle square wave of the specified amplitude is the stimulus during all the following tests of the saturation monitors. Use a scope and a signal generator to observe and stimulate during this step

It can be tricky to get a low enough drive level to get below the trigger threshold of the current shunt drive saturation monitor. Either a signal generator capable of millivolt level square waves must be used, or a voltage divider or attenuator must be used.

For the inner loop saturation monitors (U33, U41, U39), the stimulus is applied to the "Inner Loop DB-9 Sensor PD" input. The idea here is to find the threshold of pulses observed at TP-27 that just triggers the ~1 second pulses on the appropriate pin of the "Rack Interface".

INPUT	OUTPUT	DRIVE AMPLITUDE	EXPECTED THRESHOLD VALUE	MEASURED THRESHOLD VALUE
"Inner Loop DB-9 Sensor PD" pin4 (+), Pin9 (-)	Pin 7 of the 37 pin Rack Interface connector on the front panel	Start at about 0.4V p-p out of the function generator and decrease the drive until there are no more ~1 second trigger events on the rack interface	Pulses above 0.5 volts +/- 0.1 volts at TP-27 should trigger the generation of ~1 second pulses at the specified rack interface output pin	

For the Outer loop saturation monitors (U37, U34, U42), the stimulus is applied to the "Outer Loop DB-9 Sensor PD" input. The idea here is to find the threshold of pulses observed at TP-22 that just triggers the ~1 second pulses on the appropriate pin of the "Rack Interface".

INPUT	OUTPUT	DRIVE AMPLITUDE	EXPECTED THRESHOLD VALUE	MEASURED THRESHOLD VALUE
"Outer Loop DB-9 Sensor PD" pin4 (+), Pin9 (-)	Pin 12 of the 37 pin Rack Interface connector on the front panel	Start at about 0.4V p-p out of the function generator and decrease the drive until there are no more ~1 second trigger events on the rack interface	Pulses above 0.5 volts +/- 0.1 volts at TP-22 should trigger the generation of ~1 second pulses at the specified rack interface output pin	

For the Current Shunt Drive saturation monitors (U31, U38, U35), the stimulus is applied to the "IL Analog Input". The idea here is to find the threshold of pulses observed at TP-26 that just triggers the ~1 second pulses on the appropriate pin of the "Rack Interface".

INPUT	OUTPUT	DRIVE AMPLITUDE	EXPECTED THRESHOLD VALUE	MEASURED THRESHOLD VALUE
"IL Analog Input" Pins 1&2	Pin 9 of the 37 pin Rack Interface connector on the front panel	Start at about 0.01V p-p out of the function generator (or voltage divider) and decrease the drive until there are no more ~1 second trigger events on the rack interface	Pulses above 1.5 volts +/- 0.1 volts at TP-26 should trigger the generation of ~1 second pulses at the specified rack interface output pin	

5.9 **Establishing Normal Jumper Positions**
Ensure the following jumpers are in the specified position:

- ❑ Check box when the following jumpers are verified in the indicated positions

JP1-**12** JP2-23, JP3-23, JP4-12, JP5-23, JP6-23, JP7-12, JP8-12, JP9-23, JP10-12