LIGO-T030076-00-W

High-frequency operation of Frequency Stabilization Servo

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Mofidied on April 15, 2003 to include Appendix A.

Basic Design Requirements

Use of the PSL as a frequency actuator for the modecleaner servo (via the VCO wideband input) requires that the frequency response be flat within 2 dB up to 100 kHz with less than 20 deg. Of phase lag at 20 kHz. To satisfy this requirement, the FSS gain at 100 kHz should be at least 12 dB. We use 20 dB as the design goal.

Experience with Rev. D FSS cards (LIGO-D980536-D) at LHO

Although the detailed Simulink model that we generated for the H1 FSS loop indicated that the designed architecture should meet the high-bandwidth requirements, we found that we were unable to reliably increase the unity gain frequency of the FSS servos for either the H1 or H2 PSLs above about 100 kHz.

Analysis and in-situ measurements revealed the following problems:

1) The PC driver and output stages (U11 and U14, respectively, on D980536-D) had insufficient loop gain at high frequency, resulting in large phase lags.
2) The signal levels at the variable gain stages (U8) were excessive.
3) Potential for slew rate problems in the FAST path.
4) Uncompensated PC resonance at about 1.67 MHz.
5) Long cables between FSS card and RFPD and PC add delays and cause peaking in the PC path due to cable resonances.
6) RF summing box adds 10-20 deg. of phase lag at 1 MHz.

Changes made in revised FSS card

The revised FSS card schematic is LIGO-D980536-D+. A .pdf version can be found at http://blue.ligo-wa.caltech.edu/ilog/pub/ilog.cgi?group=detector&date_to_view=01/17/2003&anchor_to_scroll_to=2003:01:29:20:56:21-rick.

(Note: Richard McCarthy has asked Rich Abbott to "officially" release a Rev. E schematic.) A list of specific component changes can be found in Appendix A.

1) Added 100 kHz pole and 10 MHz zero to PA85 PC output stage (U14) and increased the output resistor (R42) from 0 to 100 ohms. This gives a nearly constant loop gain around the PA85 above 100 kHz (~26 dB) and proper operation to well above 1 MHz (~ 5 MHz). The zero can be moved down in frequency to compensate the RFPD pole (~2.4 MHz) if needed.
2) Replaced the AD847 (U11) op-amp in the PC driver stage with a higher-bandwidth AD829 to improve the loop gain.
3) Replaced R31, which forms a bypassing zero that was used to compensate the RFPD pole (~2.4 MHz), with a lead network which moves the zero to ~330 kHz in order to reduce the rate of roll off to 1/f. The lead network includes a 10 dB notch at the PC resonance frequency (~1.67 MHz) and is built on a small (~ 1cm square) daughter board.
4) Increased the gain of both the FAST and PC paths after the AD602s by factors of 8. The component sequence in the FAST path was changed to match that of the PC path, OP27/AD797/AD847 and the gain profiles at high frequency in the two paths were made similar by changing gains and pole frequencies. These changes should fix problems 2 and 3 noted above.
5) Replaced the RF summing box with revised design that utilizes series-resonant coupling for the 35.5 MHz path. The measured phase lag at 1 MHz was reduced to less than 3 deg.

Performance of revised FSS card

Revised FSS cards have been installed, tested, and are presently operating in both the H1 and H2 PSLs. The unity gain frequencies for both cards are about 600 kHz, the phase margins are about 40 deg. and the gains at 100 kHz are about 25 dB. The measured open loop transfer functions can be found in the LHO elog for the H2 FSS at http://blue.ligo-wa.caltech.edu/ilog/pub/ilog.cgi?group=detector&date_to_view=12/27/2002&anchor_to_scroll_to=2002:12:27:22:57:35-rick and for the H1 FSS at http://blue.ligo-wa.caltech.edu/ilog/pub/ilog.cgi?group=detector&date_to_view=01/17/2003&anchor_to_scroll_to=2003:01:18:00:07:07-rick

The H1 FSS open loop transfer function is shown in Figure 1, below.

Both the H1 and H2 FSS servos occasionally break into oscillation when the modecleaner is knocked out of lock, usually when the fully-locked interferometer falls out of lock. The oscillation either stops on its own or is quenched by reducing then restoring the common gain. Although this can be a nuisance, it has not seriously limited interferometer operation

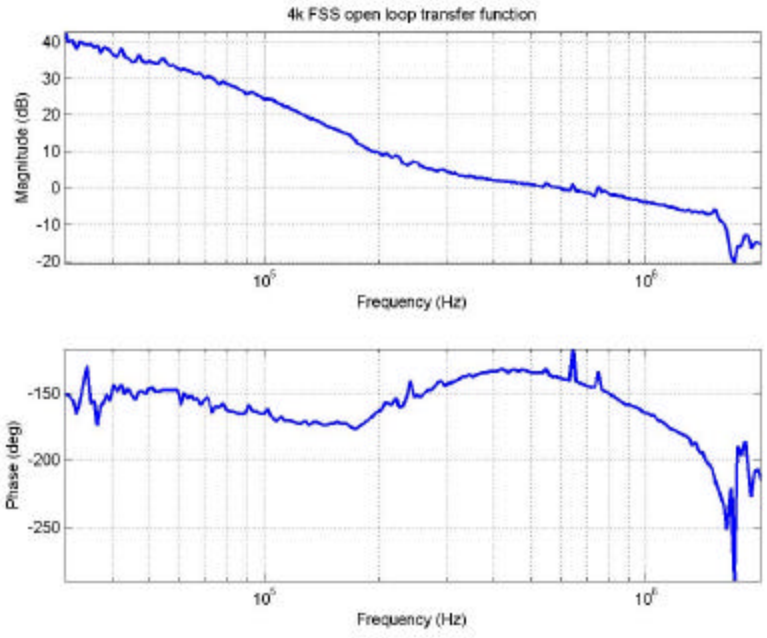

Figure 1 Measured H1 FSS open loop transfer function.

The FSS actuator transfer function (neglecting the VCO and AOM) is estimated by calculating GH/(1+GH) where GH is the open loop transfer function. For the H1 FSS, this is shown in Figure 2, below.

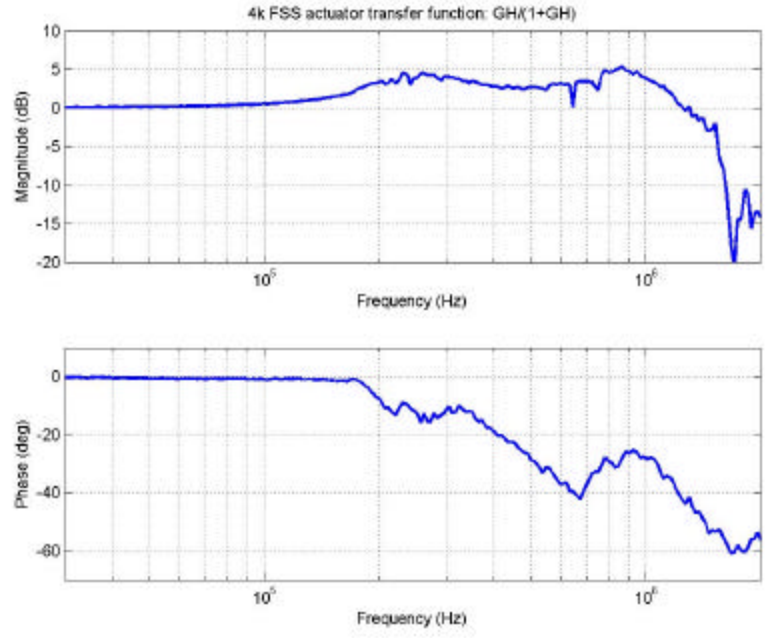

Figure 2 FSS actuator transfer function calculated from open loop transfer function.

Future work

Eliminating the long cables between the FSS card and the PSL table should enhance the performance by increasing the phase margin at the UGF and eliminating the gain peaking caused by the cable resonances. The actual FSS servo electronics (minus the control and read-back electronics) could be located on the PSL table near the 10-W laser, with the power supplies and interface electronics located in the Euro-crate in the PSL rack.

Appendix A

Changes to PA85 gain stage (U14)

1. R43 changed to 3.3 kΩ
2. R34 changed to 33 kΩ
3. R42 changed to 100 Ω
4. R44 changed to 332 Ω
5. R35 changed to 200 Ω
6. C33 changed to 22 pf; 500 V
7. Cadd1, 47 pf; 500 V, added in series with R44 to U14, pin 1

Changes made in the rest of the Pockels cell path

8. U11 changed to AD829
9. R28 changed to 500 Ω
10. R32 changed to 10 kΩ
11. R31 changed to the lead network on the daughter board
12. U9 changed to AD797
13. R22 changed to 665 Ω
14. R23 changed to 732 Ω
15. R27 changed to 73.2 kΩ
16. C23 changed to 2200 pf
17. U7 changed to OP27 (some boards may already use this component)

Changes made in the PZT (FAST) path

18. U21 changed to OP27 (some boards may already use this component)
19. R54 changed to 4.87 kΩ
20. U20 changed to AD797
21. R53 changed to 3.16 kΩ
22. C54 changed to 2200 pf
23. U19 changed to AD847
24. R52 changed to 31.6 kΩ

Changes made in the common path

25. U1 changed to AD847 (some boards may already use this component)