LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

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Pentek Noise and Glitch Measurements		
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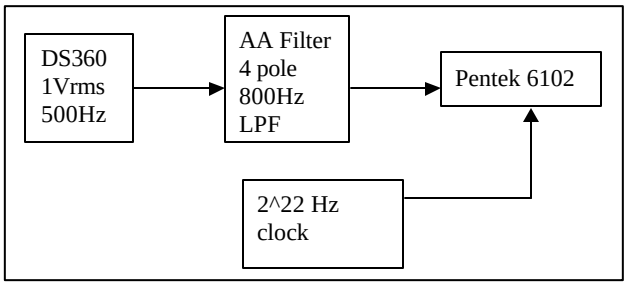
1 Introduction

This document describes the noise and glitch measurements made on a Pentek model 6102 ADC and DAC module. The measurements were made during December of 2002 at Caltech. All measurements were made using a Pentek model 6102 with options 007 and 014. The serial number for the module used was 0247071. Although only one Pentek module was used, several others were checked and it was verified that the results would be very similar to those described in this document.

2 Pentek ADC Input Referred Noise

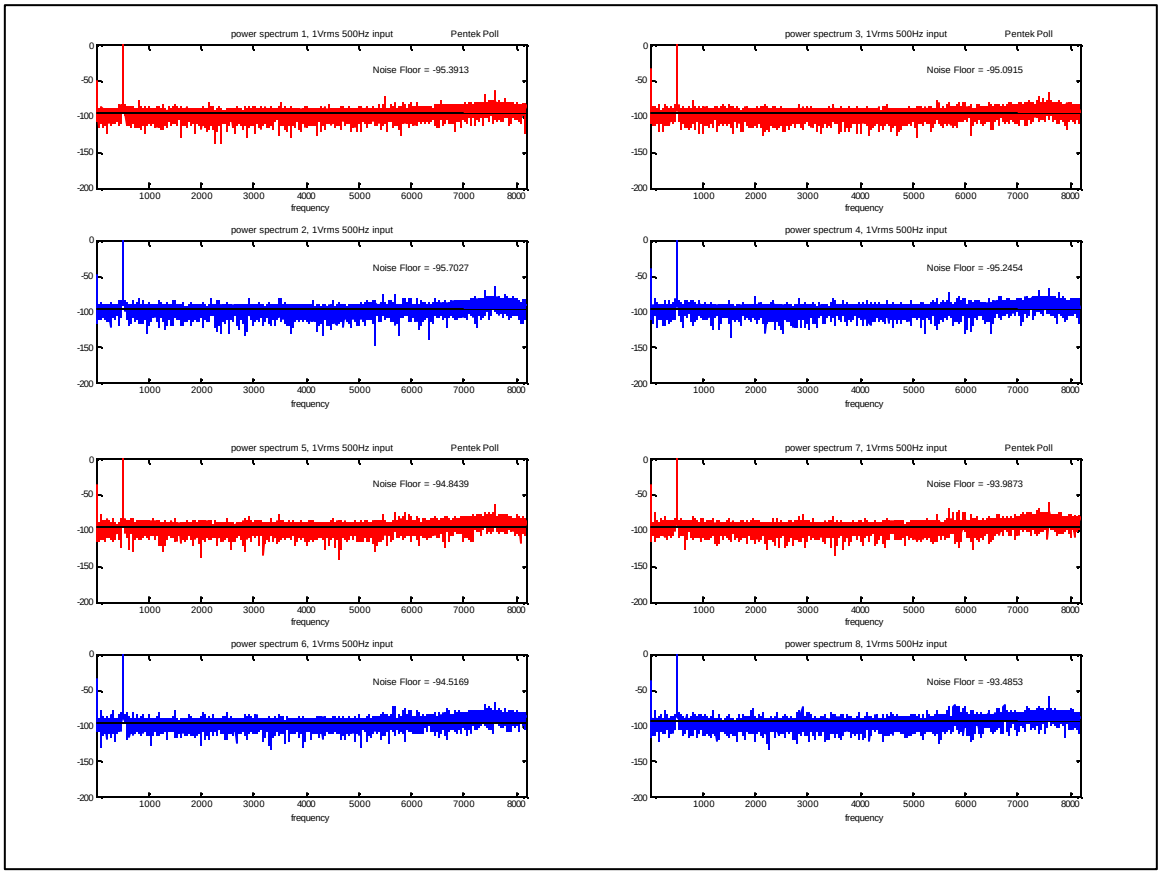
The input referred noise of the ADCs was measured for configurations using polling of the 6102 FIFO not empty bit and polling of the Variable Timing Delay ready bit. The test setup is shown in the figure below.



The 2^{22} Hz clock is derived from the GPS timing modules as in the LIGO interferometers. The internal clock divider was set such that the sample rate of the ADCs was 16384 Hz. The FFT used was a 32768 point FFT.

2.1 Input Referred Noise While Using Pentek Polling

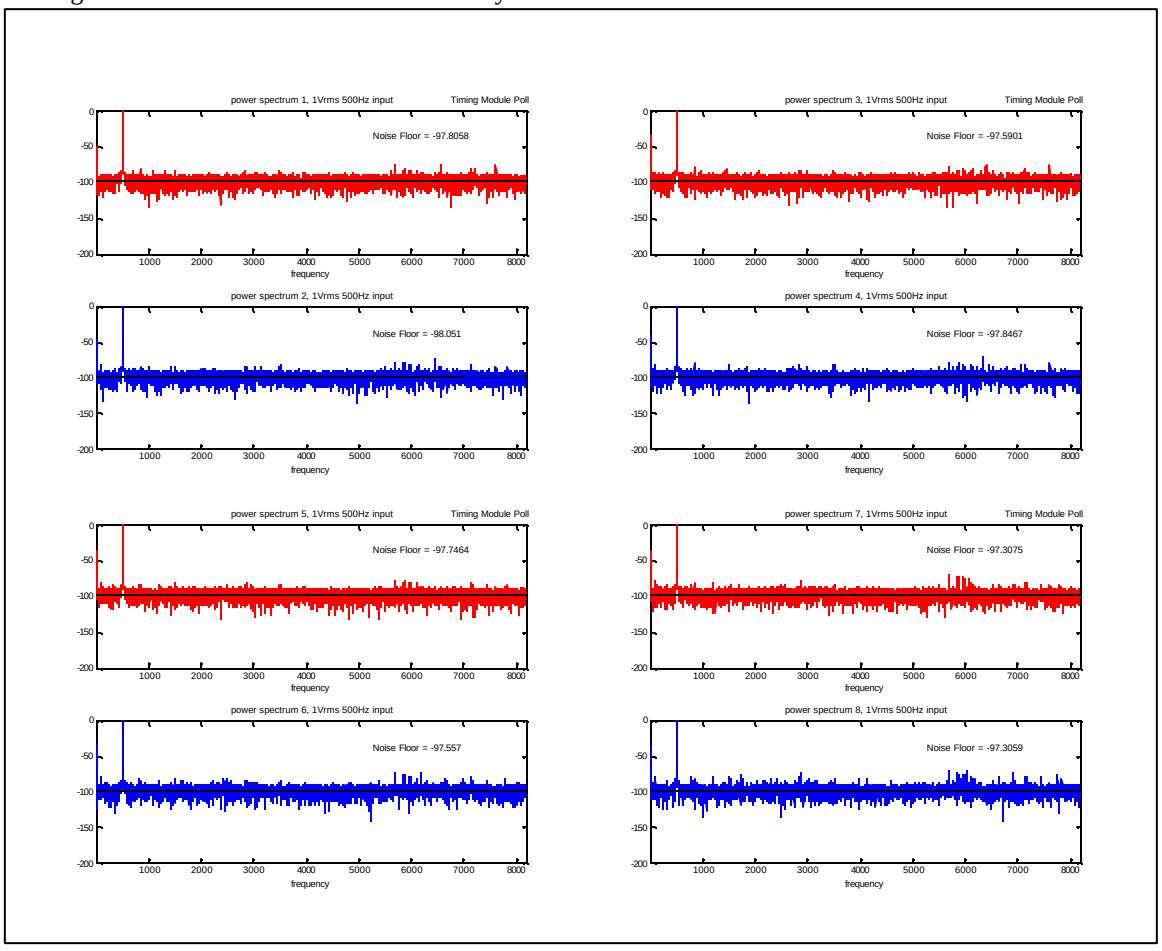
The figures below show the noise for the Pentek 6102 when using the FIFO not empty bit as the indication for data ready.



The average noise floor for each channel is approximately –95dBV/rtHz, which corresponds to approximately 18uV/rtHz. The spectrum is relatively free of spurs and other hash with the exception of the broad peak in all 8 channels around 7.5KHz. There is also another set of spikes around 6KHz.

2.2 Input Referred Noise While Using Variable Delay Timing Module Polling

The figures below show the noise for the Pentek 6102 when using the polling bit of the Variable Delay Timing Module as the indication for data ready.



The average noise floor for each channel is approximately –97dBV/rtHz, which corresponds to approximately 14uV/rtHz. It is worth noting that while the spikes around 6KHz still remain the broad peak in the spectrum around 7.5KHz has been eliminated.

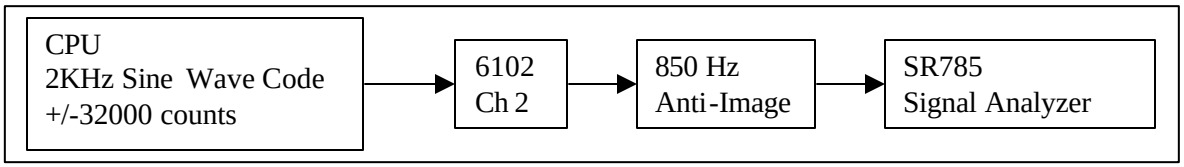
2.3 ADC Input Referred Noise Summary

Continuously polling the Pentek 6102 while it is sampling increases the input referred noise of the device. The increase is in the form of a broad peak in the spectrum. It has been noticed that the position of this peak will move around in frequency depending on when the CPU begins to poll the module. In the case of these tests the CPU was not loaded and so the polling of the module resumes as soon as the sample is taken. If the CPU performs functions such as filtering, the peak will move and has been seen as low as 2KHz.

The noise around 6KHz does not appear to be related to polling the module and could be related to the sampling process, VME bus activity or some other noise source.

3 Pentek DAC Output Referred Noise

The figure below shows the setup used to measure the DAC output referred noise.



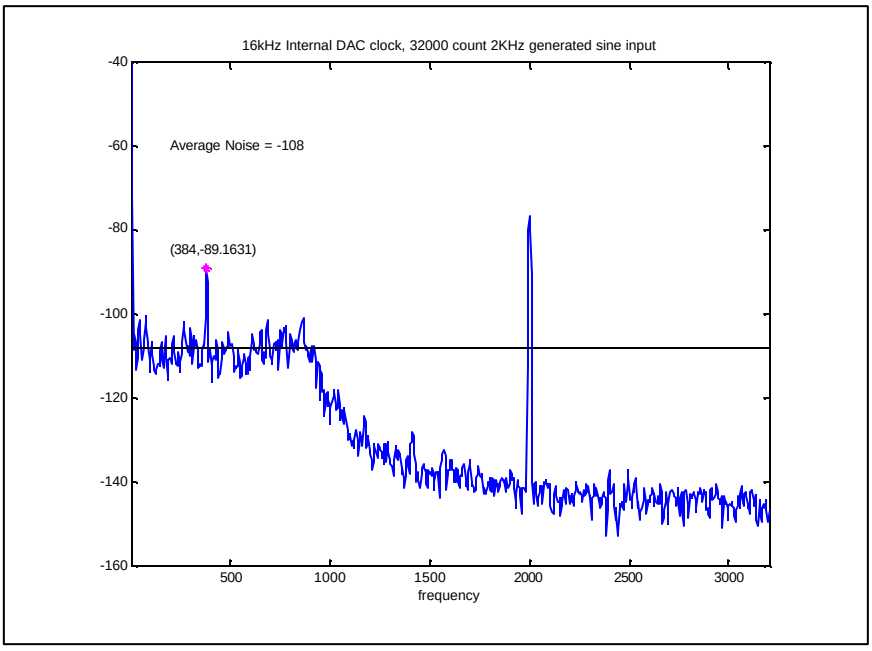
All of the measurements shown were performed on channel 2 of the Pentek, but they are consistent with the noise measured on all channels of the module. The output noise was measured for four different clocking options:

1. 16384 Hz DAC clock derived internal to the Pentek from the 2^{22} Hz input clock.
2. 16384 HZ DAC clock from the variable delay timing module. The variable timing delay module generates four 0.5 usec pulses at each 16384 Hz transition.
3. 2^{20} Hz DAC clock derived internal to the Pentek from the 2^{22} Hz input clock.
4. 2048 Hz DAC clock derived internal to the Pentek 6102 from the 2^{22} Hz input clock.

The measured output noise is shown in each of the figures below.

3.1 16384 Hz DAC Clock Derived Internal to Pentek 6102

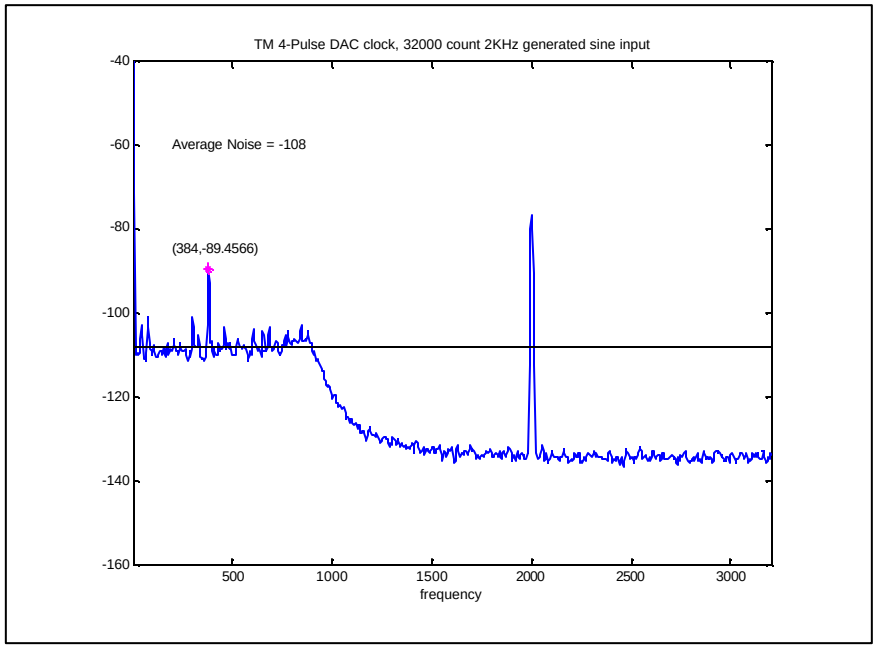
The figure below shows the measured output noise of the Pentek 6120 using a 16384 Hz clock that has been divided down internally from the standard LIGO 2^{22} Hz timing system clock.



The measured output noise of the DAC is approximately –108 dBV/rtHz which corresponds to 4uV/rtHz. The attenuated 2KHz sine wave peak can be seen in the plot. In addition there is a peak at 384 Hz. It was determined that this peak is an intermodulation term that is a result of how the sine wave is generated in software and it is not inherent in the output characteristics of the DAC.

3.2 16384 Hz Clock from Variable Delay Timing Module

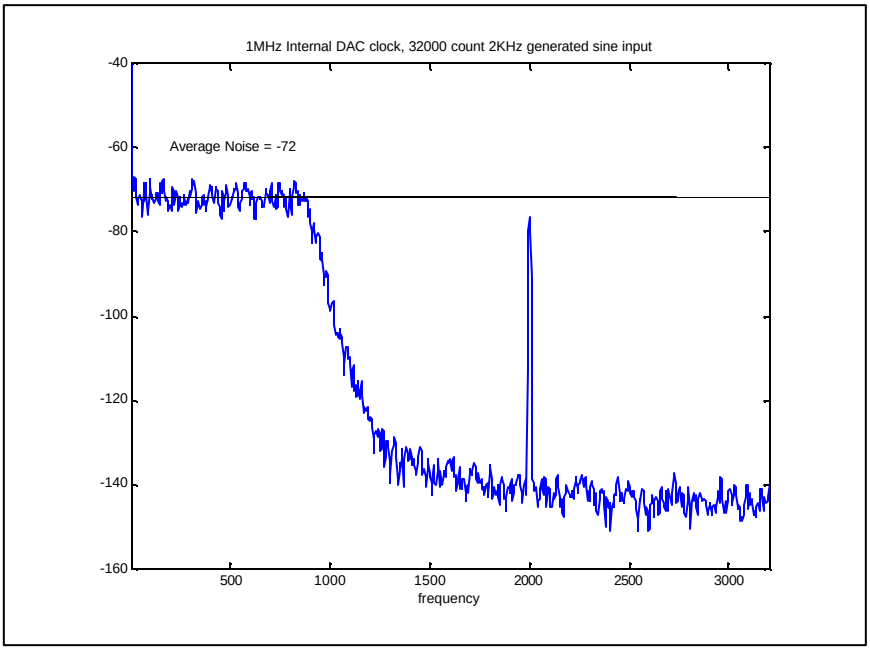
The figure below shows the measured output noise of the Pentek 6120 using a 16384 Hz clock from the LIGO Variable Delay Timing Module. This module divides the standard LIGO 2^{22} Hz timing system clock down to 16384 Hz and produces four 0.5 usec pulses at each clock transition. This is done to clear the DAC pipeline and reduce delay in the system.



As can be seen from the figure the measured noise is virtually the same as the 4uV/rtHz measured for the case above where the clock is derived internal to Pentek 6102. The difference in the "hashiness" of the plot is a result of the number of averages used for the measurement.

3.3 2^{20} Hz Clock Derived Internal to Pentek 6102

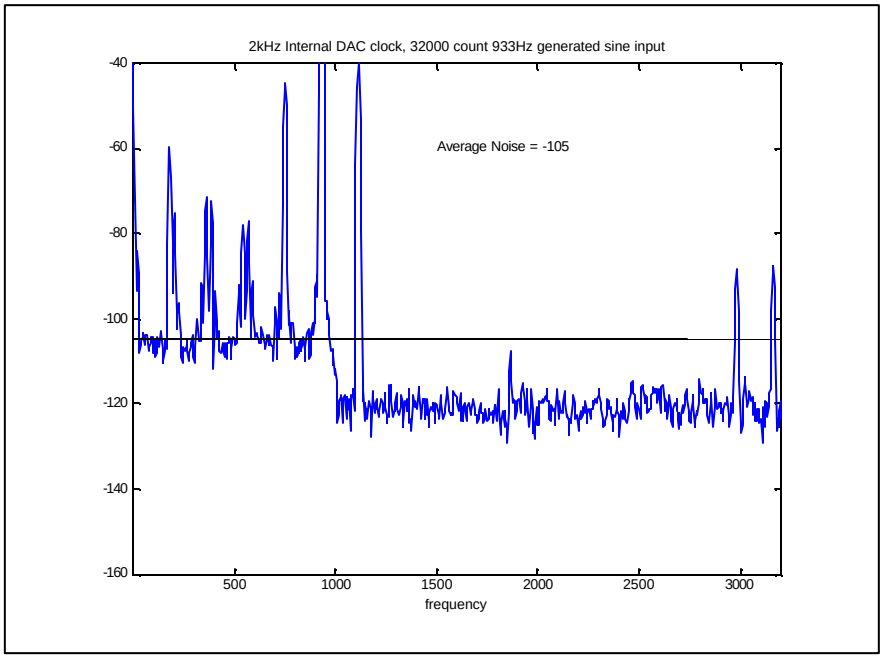
The figure below shows the measured output noise of the Pentek 6120 using a 2^{20} Hz clock that has been divided down internally from the standard LIGO 2^{22} Hz timing system clock.



The measured noise of the DAC output is approximately –72 dBV/rtHz which corresponds to 250uV/rtHz. This increase in noise is probably due to jitter across the 1usec sample boundaries. Clearly this is not something that should be done in a low noise system.

3.4 2048 Hz DAC Clock Derived Internal to Pentek 6102

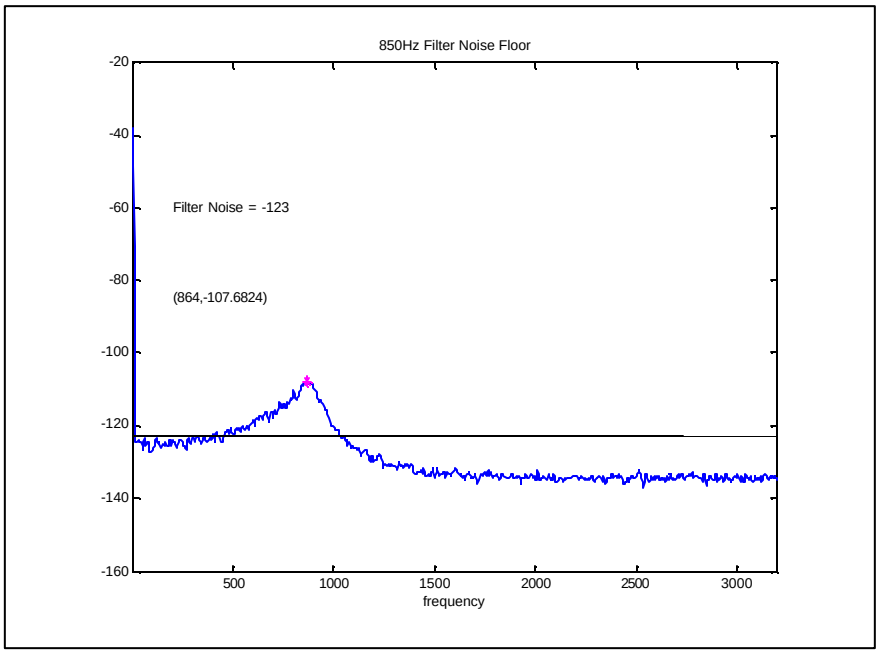
The figure below shows the measured output noise of the Pentek 6120 using a 2048 Hz clock that has been divided down internally from the standard LIGO 2^{22} Hz timing system clock.



For this test the sine wave frequency was changed to 933 Hz. The measured output noise of the DAC is approximately –105 dBV/rtHz, which corresponds to 5.6uV/rtHz. The peaks that are seen in the spectrum are intermodulation peaks related to the sine wave generation and not related to the DAC output noise.

3.5 Anti-Image Filter Noise

For consistency the noise of the 850 Hz Anti-Image filter is shown in the plot below.



As can be seen from the plot, the filter does contribute to the measured noise shown in the sections above for frequencies close to the 850 Hz cut off. But for frequencies below approximately 500 Hz the contribution can be considered negligible. In the measured noises quoted above we have assumed that the contribution from the filter noise is negligible for all frequencies below 850 Hz.

3.6 DAC Noise Summary

The output-referred noise for the Pentek 6102 DACs is approximately 4 uV/rtHz for a sample frequency of 16384Hz, regardless of whether the sample clock is generated from the dividers internal to the Pentek or from the LIGO Variable Delay Timing Module.

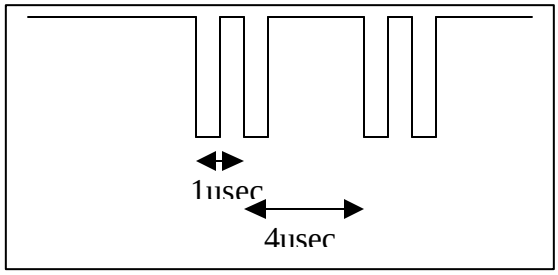
The output-referred noise of the Pentek 6102 increases substantially when the clock frequency is increased to 2^{20} Hz. This could be due to timing jitter inherent in the code used to calculate the sine wave, excess noise in the DAC circuitry at these frequencies, or a combination of both. This mode of operation should not be used for any application where noise is an issue.

4 Pentek 6102 DAC Output Glitches

It has been observed that the output of the Pentek 6102 DAC module is subject to glitches. This glitching is most commonly observed on channels 4, 5, and 6 when the output voltage crosses from a small negative value to a positive value, i.e. zero crossing. These glitches have not been observed on the other channels, but they may occur much more infrequently. The glitches resemble DAC glitch energy in appearance, but they do not occur on every zero crossing, and they are present for an entire DAC clock cycle. In order to measure the glitches for these tests it was determined that the glitches occur most frequently when the output transitions from the voltage corresponding to –1 bit (data word=0xFFFF) to zero (data word=0x0000). Software was written that sequentially wrote, at 16384 samples per second, the data pattern 0xFFFF, 0x0000, 0x0001, 0x0000, 0xFFFF…., i.e. –1, 0, 1, 0, -1, 0, 1…

Using this code, it was discovered that the output contained glitches at three discrete levels, the width of which are determined by the clock used for DAC sampling. If the 4 pulse sample clock generated by the Variable Delay Timing Module (VDT) is used the glitch is approximately 4 usec wide. This is the time

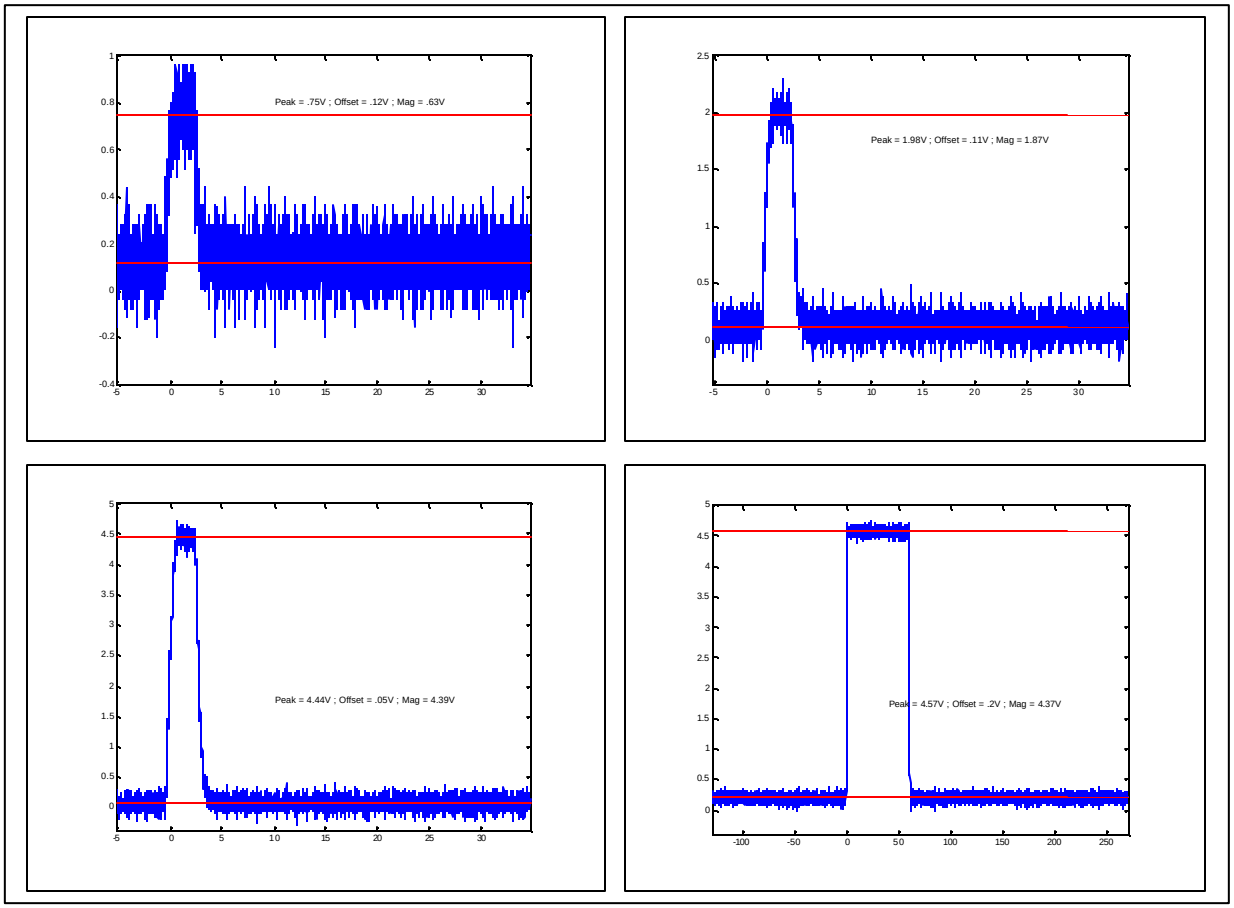
from the second clock pulse to the third clock pulse. For unknown reasons the clock pulses generated by the VDT are not the nominal 500 nsec wide. They are actually as shown in the figure below.



It was later confirmed that if a VDT that produces 4 symmetric pulses is used the glitch width is 1 usec. It should be noted that when a single DAC clock pulse at the nominal 16384 Hz is used, the width of the glitch is the full clock period, i.e. 61.04 usec. Additional testing confirmed that these output glitches are not seen on modules without option 014, i.e. low distortion DAC option. The only glitches that were observed with these modules are the typical glitch energy pulses you would expect to see from the DAC chips used in the module. This glitch energy was measured previously to be approximately 500nV-sec and this number was reconfirmed during these tests.

4.1 DAC Glitch Levels

The figures below show the 3 discrete voltage levels that have been observed for the DAC glitches. They correspond to 0.63V, 1.87V and 4.39V, respectively. No other voltage levels have been observed and the glitch voltage is always positive.

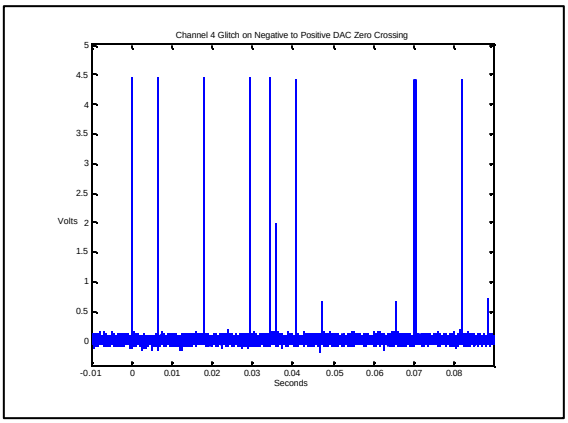


The fourth figure shows a 4.39V glitch that is the full sample clock width. This glitch width is produced when a single DAC clock pulse at the 16384 Hz sample frequency is used. The full-scale positive voltage of the Pentek 6102 DAC is 5V. Note that these three glitch voltage levels correspond to 1/8, 3/8 and 7/8 the positive full-scale range. These voltage levels would be produced if 0xFFF, 0x2FFF and 0x6FFF were written to the DACs by the software, but it has been verified using a bus analyzer that the proper values are being written to the 6102. Therefore, the problems must be internal to the board.

At first it was thought that the voltage glitches arose from some sort of race condition between the software and the board timing. This is probably not the case since the glitches appear on channels 4, 5, and 6 regardless of what order the channels are written to by the software, i.e. the glitches do not move to the other channels. It can not be stated categorically that the glitches are only on channels 4, 5 and 6, but they do occur at a much less frequent rate on the other channels, and to date have not been observed on any other channels .

4.2 DAC Glitch Timing

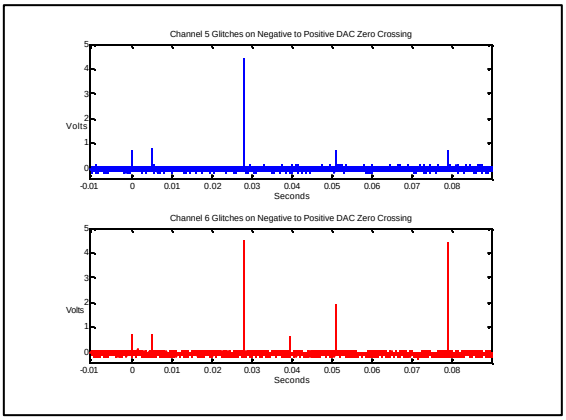
The figure below shows a sequence of glitches that were observed on channel 4 of the 6102 under test. The software used to produce these glitches wrote, at a 16384 sample rate, 0, -1, 0, -1, 0… As can be seen from the figure the glitches are what we would call psuedorandomly spaced.



In fact the time difference from each glitch to the next in the figure is approximately 6.45, 11.48, 11.48, 5.02, 1.46, 5.01, 6.42, 18.03, 4.97, 11.43, and 6.49 milliseconds, respectively. The time measurement accuracy was +/-10microseconds. A careful analysis of these spacings shows that various combinations of 1.46, and 5.01 milliseconds can used to obtain each, i.e. 11.48=5.01+5.01+1.46, etc, but a definite pattern for the spacing and the voltage level has not yet been determined.

4.3 DAC Glitch Correlation Between Channels

The figure below shows the glitches observed on channels 5 and 6 of the 6102 under test.



Note that for each glitch seen in channel 5 there is a corresponding glitch in channel 6, but there is an extra glitch in the channel 6 trace. It should also be noted that the glitch voltage level are not the same for each channel. Additional tests showed that there was no correlation between the glitch timing on channel 4 and either channel 5 or 6. In a way this makes sense since channel 5 and 6 are paired together in the module and channel 4 is paired with channel 3.

5 Conclusions

1. The input noise of the Pentek ADC for a sample frequency of 16384 Hz is approximately 14uV/rtHz. If the Pentek ready bit is polled via the VMEbus this nois e will increase and there will be a bump in the spectrum somewhere from 2KHz to 6KHz. The position of this bump depends on the timing of the VMEbus polling.
2. The output referred noise of the Pentek 6102 DAC is approximately 4uV/rtHz for a sample frequency of 16384 Hz. If the output sample clock is increased to 1MHz, the output noise increases tremendously.
3. DAC glitches appear at zero crossing for channels 4, 5 and 6. These glitches can be any one of three discrete levels, 0.63V, 1.87V or 4.39V. The timing of these glitches is pseudorandom in nature. There appears to be correlation between glitches on channels 5 and 6, but not channel 4. One theory is that these glitches are produced because of some race condition between the 2^{22} Hz clock frequency used by LIGO and the on board clock used by the 6102 for internal timing and synchronization of the module DACs. This issue will need to be addressed by Pentek. Since the DAC glitches are not seen the modules do not have option 014, it appears that the problem is in the circuitry or logic used for the low distortion DACs.