LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

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LIGO Variable Delay Timing Board Design Requirements		
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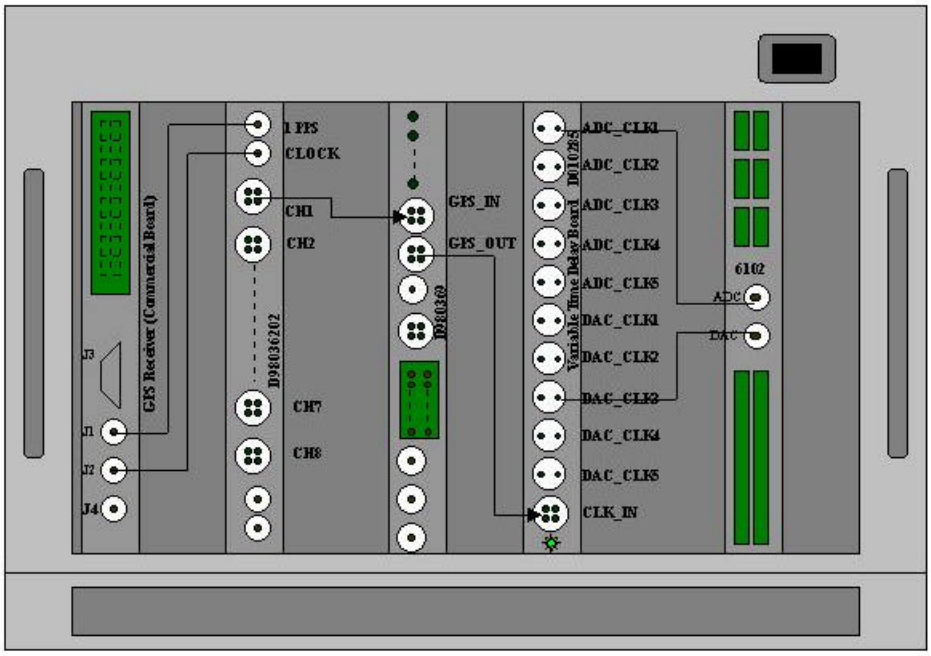
1 Introduction

2 General Description

2.1 Product Perspective

The Variable Delay Timing Module is part of the LIGO timing system. All timing information and clock signals in the system are derived from and/or referenced to the Global Positioning System (GPS). The figure below shows the components and connections for a typical LIGO Timing System crate.



In the far left slot of the crate is a GPS receiver module developed by Brandywine Communications for the LIGO project. This module receives and decodes signals from GPS satellites and provides 1 PPS (1 pulse-per-second) and 2^{22} Hz clock signals to a GPS Fanout Module (D980362-02) designed by LIGO Laboratory. The 2^{22} Hz clock is phase locked to the 1 PPS on the GPS receiver board.

The function of the GPS Fanout Module is to provide for eight 4 pin LEMO outputs that each contain the 1 PPS and 2^{22} Hz clock signals. Signals output from the GPS Fanout Module, which are differential ECL, then go to the GPS Clock Driver Module (D980369). The GPS Clock Driver is another custom module developed by LIGO Laboratory. In addition to providing a means of enabling and disabling the clock outputs to the Variable Delay Timing Module, the GPS Clock Driver Module has many features that are not applicable to this discussion. These features are fully described in other LIGO Timing Systems documents. The 1 PPS and 2^{22} Hz clock signals are passed through the GPS Clock Driver Module to the clock inputs of the Variable Timing Delay Module. These signals are differential ECL.

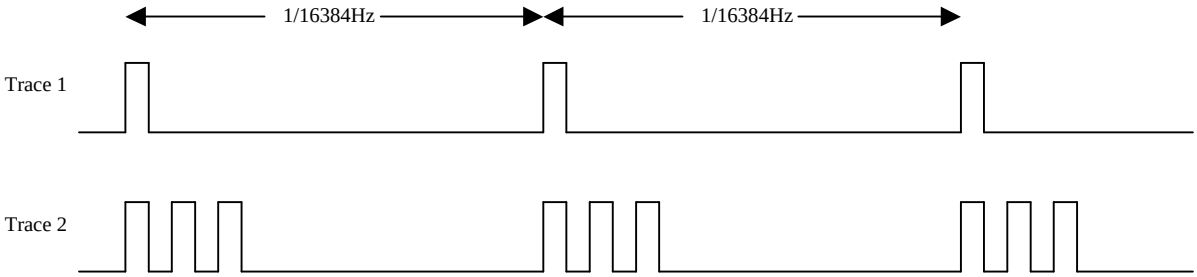
2.2 Product Functions

The Variable Delay Timing Module has two main functions:

- Provide the 2^{22} Hz clock to the LIGO ADC modules
- Provide a delayed clock at the fundamental sample frequency (16384 or 2048) to the LIGO DAC modules

In addition to these main functions there are several related sub-functions:

- Provide a delayed VMEbus interrupt or polling bit that can be used in lieu of polling the status of the LIGO ADC modules. This is desirable because it has been discovered that polling or reading the LIGO ADC modules during conversion causes the input referred noise of the devices to increase.
- Provide a means for ensuring that the 2^{22} Hz clock signal is always in sync with the 1 PPS, i.e. there are exactly 2^{22} clock pulses every second. If there are not exactly 2^{22} clock signals each second, the front-end software systems will lose synchronization.
- Provide a means for determining how many ADC samples there have been since the last sample has been read. If the LIGO front-end software used to read the ADCs is functioning correctly this number will always be less than or equal to 1. If the software gets out of sync ADC samples can be missed. By reading this count on every sample the software can determine if samples have been missed. If the number is greater than 1, an error can be generated and the software resynchronized.
- Provide multiple DAC clock pulses for each DAC clock. It has been determined that there is a pipeline delay in the DAC modules used by the LIGO front-end systems. A sample written to the module is not clocked out on the next DAC clock pulse. It actually takes three clocks for the sample to appear at the analog output of the module. For this reason it is desirable to have multiple, fast (~1 usec duration) pulses for each DAC clock output cycle. This concept is illustrated in the figure below. The fundamental DAC clock period in the figure is 1/16384Hz, but the same concept applies to other sample periods. The top trace (Trace 1) shows a system where only one clock pulse is output at this rate. The bottom trace (Trace 2) shows a system that uses three.



- Provide a bit that can be read from the VMEbus to determine if the input clock signals are hooked up and active.
- Provide a register or registers that can be used to read the status or position of all jumper settings on the board.
- Provide a means to reset or resynchronize all counters and delays on the board from the VMEbus.

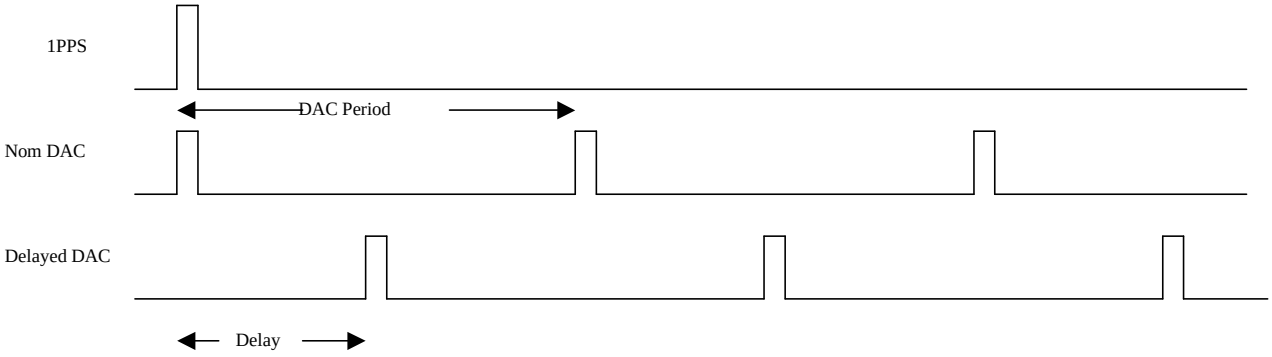
3 Requirements

3.1 Operational Requirements

3.1.1 DAC Clock Outputs

3.1.1.1 DAC Clock Delay

The module shall provide for delaying the DAC clock pulses as measured from the nominal DAC clock pulse aligned with the 1 PPS clock edge. The delay is illustrated in the figure below.



The delay shall be adjustable (from the VMEbus) over the entire range of the DAC clock period. The minimum step size for a 16384 Hz DAC clock period shall be one 2^{22} Hz clock period. The minimum step size for the 2048 Hz DAC clock period shall be eight 2^{22} Hz clock periods.

3.1.1.2 DAC Clock Pulse Generation

The module shall provide for the generation of a DAC clock pulse or pulses at the end of each DAC clock delay period. The number of pulses shall be selectable. Selections shall include 1, 2, or 4 pulses. Each pulse shall be a minimum of TBD nsec in width. The frequency of the pulses is TBD. In the figure above the number of DAC clock pulses shown is 1 per DAC clock period.

3.1.2 ADC Clock

3.1.2.1 ADC Clock Frequency

The ADC clock frequency shall be the 2^{22} Hz clock provided as an input to the board.

3.1.2.2 ADC Clock Pulse Width

The ADC clock shall be a 50% duty cycle 2^{22} Hz signal.

3.1.2.3 ADC Polling and Interrupt Delay

The module shall provide a means to delay the ADC polling bit (or register) and VMEbus interrupt generation. This delay is similar to that described for the DAC delay in section 3.1.1.1 above. The module shall also provide for a register that can be used to determine how many ADC polling delay pulses have occurred since the last ADC polling delay pulse was issued. This register shall accessible via the VMEbus. This feature is not necessary for the interrupt delay since the VMEbus automatically keeps track of the number of pending interrupts.

3.1.3 Interrupt versus Polling Mode of Operation

The module shall provide for selection of polling mode or interrupt mode. In polling mode the module shall set a bit or update a counter in the status register at the end of each polling delay. In the interrupt mode of operation a VMEbus interrupt is generated at the end of each polling delay.

3.1.4 Clock Resynchronization

The module shall provide for resetting or re-synchronizing, from the VMEbus, the clocks and delays generated on the board. When a reset is asserted, all delays and clocks will be re-synchronized with the 1 PPS signal.

3.1.5 Clock Error Detection

The module shall set a bit that can be read via the VMEbus if the number of 2^{22} Hz clock pulses received via the input connector is not exactly 2^{22} per second. This measurement shall use the 1 PPS signal as a reference.

3.1.6 Jumper Readback

The module shall provide for reading all jumper settings from the VMEbus.

3.2 VMEbus Requirements

3.2.1 Addressing

The module shall respond to both supervisory and non-supervisory mode of VME Short IO address space. The base address of the module shall be selectable within the short IO address space and selection switches shall be provided for A(10) through A(15).

3.2.2 VMEbus Interrupts

The module shall provide for the generation of VMEbus interrupts and interrupt vectors. The interrupt number shall be selectable for IRQ1 through IRQ7. The interrupt vector shall be selectable from 0 through 255. Interrupt generation shall be in accordance with the descriptions in the previous sections.

3.3 Electrical Requirements

3.3.1 2^{22} Hz Clock and 1 PPS Inputs

The 2^{22} Hz clock and 1 PPS inputs shall be compatible with the differential ECL signal supplied be the LIGO Clock Driver and/or LIGO Clock Fanout Modules.

3.3.2 ADC and DAC Clock Outputs

The ADC and DAC clock outputs shall be differential TTL.

3.3.3 Channel to Channel Clock Skew

TBD

3.3.4 Clock Jitter

The jitter on each ADC or DAC clock output shall be less than TBD. Jitter is defined as the variability in the pulse-to-pulse time delay of each clock output as measured from the nominal.

3.3.5 Clock Polarity

The polarity of the ADC and DAC clock outputs shall be selectable via jumpers on the board. One jumper controlling the polarity of the ADC clock signal is sufficient, but each DAC clock output shall have its own polarity selection jumper.

3.3.6 Number of Channels

There shall be 6 ADC and 4 ADC clock outputs per module.

3.4 Mechanical Requirements

3.4.1 Module Size/Dimensions

The module shall be a standard 6U, single slot VME module and conform to all applicable requirements of the VME specification.

3.4.2 Input and Output Connectors

The input clock connector shall be a LEMO EPG.1B.304.HLN connector (4 pin LEMO). The 2^{22} Hz input shall be pins 3 and 2 (3 being positive). The 1 PPS input shall be pins 4 and 1 (4 being positive).

The output connectors shall be LEMO EPG.0B.302.HLN connectors (2 pin LEMO). Pin 1 shall be the positive pin for these connectors.