Board Serial Number:

TTFSS_____ TTFSS Interface Board_____

LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
-LIGO-
CALIFORNIA INSTITUTE OF TECHNOLOGY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Technical Note	**LIGO-E040418- 04- W**	10/11/04

Test Plan
Table Top Frequency Stabilization Servo (TTFSS) - D040105 and TTFSS Interface Board – D040423

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This is an internal working note
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Date _____

Tested by _____

This plan tests both the TTFSS and the TTFSS Interface Board. The two modules should be connected via a 37-pin cable.

Note: No signals are applied via the P1 connector on the TTFSS Interface Board (switches and variable gain stages) unless specified. All measurements are made using active probes, where applicable.

1) **Current draw:**
Connect TTFSS Interface Board to the TTFSS card (with TTFSS Daughter Card installed) using the 37-conductor interconnect cable. Apply +,- 24V as specified on the TTFSS Interface Board drawing (using a Euro-card extender card works too).

+24V:
Design value: 200 mA +/-10% Measured value:_____ Pass/Fail _____

-24V:
Design value: 200 mA +/-10% Measured value:_____ Pass/Fail _____

2) **Test TTFSS Interface Board voltage regulator outputs:**

+15V:
Design value: +15V +/- 5% Measured value: _____ Pass/Fail _____

-15V:
Design value: -15V +/- 5% Measured value: _____ Pass/Fail _____

3) **Test TTFSS voltage regulator outputs:**

+15V:
Design value: +15V +/- 5% Measured value: _____ Pass/Fail _____

+5V:
Design value: +5V +/- 5% Measured value: _____ Pass/Fail _____

-15V:
Design value:: -15V +/- 5% Measured value: _____ Pass/Fail _____

-5V:
Design value: -5V +/- 5% Measured value: _____ Pass/Fail _____

4) **Check that TTFSS daughter card is getting power:**

+15V:
Design value: +15V +/- 5% Measured value: _____ Pass/Fail _____

-15V:
Design value:: -15V +/- 5% Measured value: _____ Pass/Fail _____

5) **Check for overall offset; TP10 to ground:**

Design value: < +/- 2 V Measured value: _____ Pass/Fail _____

6) **Test LO mon indicator:**
Drive the LO input on the TTFSS front panel with a 21.5 MHz sine wave at 17 dBm. Measure TP14 to ground.

Design value: 5V +/- 0.5V Measured value: _____ Pass/Fail _____

7) **Test switches:**

a) Short pin P1-1A on the P1 connector of the TTFSS Interface Board (pin 2 on FLKM connected to P1) to ground and observe that the path from Test1 In of the TTFSS front panel to TP3 on the TTFSS opens (normally closed).

Measurement result: Pass/Fail _____

b) Short pin P1-14A on the P1 connector of the TTFSS Interface Board (pin 28 on FLKM connected to P1) to ground and observe that the path from Test1 In of the TTFSS front panel to TP2 on the TTFSS opens (normally closed).

Measurement result: Pass/Fail _____

c) Short pin P1-2A on the P1 connector of the TTFSS Interface Board (pin 4 on FLKM connected to P1) to ground and observe that the path from Test2 In of the TTFSS front panel to TP3 on the TTFSS closes (normally open).

Measurement result: Pass/Fail _____

8) **Test variable gain stages:**

Note: measurements can be made, for instance, by driving TEST1 IN (-30 dBm) and measuring the TF (10 kHz to 100 kHz span) between specified points using active probes).

a) **Common gain**: apply voltage between pin P1-5A on the P1 connector of the TTFSS Interface Board (pin 10 on FLKM connected to P1) and ground. Verify gains between TP3 and TP2 as follows. Note that the gain measured with 0 V applied is the "nominal" gain.

Voltage applied	Design Gain	Measured Gain
0 V	3 to 4 dB	_____(nom.) Pass/Fail _____

-6.25 V	nom. -20 +/-2 dB	_____ Pass/Fail _____
+6.25 V	nom. +20 +/-2 dB	_____ Pass/Fail _____

b) **FAST gain**: apply voltage between pin P1-11A on the TTFSS Interface Board P1 connector (pin 22 on FLKM connected to P1)and ground. Verify gains between TP11 and TP2 as follows. Note that the gain measured with 0 V applied is the "nominal" gain.

Voltage applied	Design Gain	Measured Gain
0 V	2 +/- 0.5 dB	_____(nom.) Pass/Fail _____
-6.25 V	nom. -20 +/-2 dB	_____ Pass/Fail _____
+6.25 V	nom. +20 +/-2 dB	_____ Pass/Fail _____

9) **Test variable voltage outputs:**

a) **Input offset**: Apply voltage between P1-3A on the TTFSS Interface Board P1 connector (pin 6 on FLKM connected to P1) and ground. Measure on the TTFSS card between the side of R8 closest to TP1 and ground. Note: voltages are inverted.

Voltage applied	Design Voltage	Measured Voltage
0 V	0 +/- 0.5 V	_____ Pass/Fail _____
-10 V	+10 +/- 0.5 V	_____ Pass/Fail _____
+10 V	-10 +/- 0.5 V	_____ Pass/Fail _____

b) **SLOW voltage**: Apply voltage between P1-7A on the TTFSS Interface Board P1 connector (pin 14 on FLKM connected to P1)and ground. Measure at the SLOW out BNC on the back of the TTFSS box Note: BNC shield is the common.

Voltage applied	Design Voltage	Measured Voltage
0 V	0 +/- 0.1 V	_____ Pass/Fail _____
-10 V	+2.2 +/- 0.2 V	_____ Pass/Fail _____
+10 V	-2.2 +/- 0.2 V	_____ Pass/Fail _____

10) **Test fast channel monitor points (on the Interface card front panel):**

a) **MIXER**: Drive Test1 In and measure the TF between TP3 on the TTFSS and the front panel MIXER monitor point on the TTFSS Interface Board.
Design value: 0 +/- 0.5 dB @ 100 kHz Measured value: _____ Pass/Fail_____

b) **FAST**: Drive Test1 In and measure the TF between TP10 on the TTFSS and the front panel FAST monitor point on the TTFSS Interface Board.
Design value: 0 +/- 0.5 dB at 100 kHz. Measured value: _____ Pass/Fail_____

c) **PC**: Power the PA85 with +,- 100V using the CPC connector on the front of the TTFSS Interface Board. **CAUTION**: HIGH VOLTAGE- current drawn should not exceed 30 mA!.
Drive the Test1 In input with a 100 kHz sine wave @ -10 dBm. Measure the DC voltage at the PC front panel connector on the TTFSS Interface Board.

Design value: 3.16 +,-0.5 V Measured value: _____ Pass/Fail_____

11) **Transfer functions:** Eventually they will be compared with a model. For now make hard copies and record data files. Drive Test1 In input.

a) **Verify 21.5 MHz notch**: Measure TF between Test1 In (ref.) and TP1 and measure the notch frequency. Range: 4 MHz to 40 MHz; BW: 100 Hz; Source: -30 dBm.

Design value: 21.5 +,-.25 MHz. Measured value: _____ Pass/Fail_____

File_____

b) **Mixer to common**: Measure TF between Test1 In (ref.) and TP2. Range: 10 kHz to 20 MHz; BW: 100 Hz; Source: -30 dBm; Marker: 1 MHz.

Design marker value: +12.2 +,- 1 dB. Measured value:_____ Pass/Fail_____

File_____

c) **FAST path 1**: Measure TF between TP2 (ref.) and TP12. Range: 1 kHz to 10 MHz; BW: 100 Hz; Source: -30 dBm; Marker: 10 kHz. Verify the pole at 10 kHz.

Design marker value +17.6 +,- 1 dB. Measured value:_____ Pass/Fail_____

File_____

d) **Fast path 2**: Measure TF between TP12 (ref.) and TP13. Range: 1 kHz to 10 MHz; BW: 100 Hz; Source: -30 dBm; Marker: 34.3 kHz. Verify the pole at 34 kHz.

Design marker value: +9 +,- 1 dB. Measured value:_____ Pass/Fail_____

File_____

e) **Fast path 3**: Measure TF between TP13 (ref.) and TP10. Range: 1 kHz to 10 MHz; BW: 100 Hz; Source: -30 dBm; Marker: at notch frequency (~222 kHz). Note: Notch frequency to be optimized during installation - PZT-specific.

Design value: 200-400 kHz Measured value: _____ Pass/Fail_____

File_____

f) **PC path 1**: Measure TF between TP2 (ref.) and TP5. Range: 1 kHz to 10 MHz; BW: 100 Hz; Source: -30 dBm; Marker: 100 kHz.

Design marker value: -7.2 +.- 1 dB Measured value:_____ Pass/Fail_____

File_____

g) **PC path 2**: Measure TF between TP5 (ref.) and TP6. Range: 100Hz to 10 MHz; BW: 100 Hz; Source: -30dBm; Marker: 33.4 kHz.

Design marker value: 3.6 +,- 1 dB. Measured value:_____ Pass/Fail_____

File_____

h) **PC path 3**: Measure TF between TP2 (ref.) and TP7. Range: 1 kHz to 10 MHz; BW: 100 Hz; Source: -50 dBm; Marker: 333.7 kHz.

Design marker value: 7 +,- 2 dB. Measured value:_____ Pass/Fail_____

File_____

i) **PC path 4**: Measure TF between TP2 (ref.) and TP7. Range: 1.5 MHz to 1.8 MHz; BW: 100 Hz; Source: -50 dBm; Marker: at notch. Adjust variable capacitor C50 to tune notch frequency.

Design value: 1.67 +/-0.015MHz Measured value: _____ Pass/Fail_____

File_____

j) **PC path 5**: Power the PA85 with +/- 100V using the CPC connector on the front of the TTFSS Interface Board. **CAUTION**: HIGH VOLTAGE - current drawn should not exceed 30 mA!.
Measure TF between TP7 (ref.) and TP8. Range: 20 kHz to 20 MHz; BW: 100 Hz; Source: -50 dBm; Marker: 1 MHz. Note: 100 V available at TP8; check with oscilloscope before connecting to network analyzer. Do not exceed +/- 10 V or acive probes will be damaged.

Design marker value: 0 +,- 1 dB. Measured value:_____ Pass/Fail_____

File_____

12) **Noise measurements:**

a) **PC path**: active probe at TP7; input not connected; spectrum analyzer mode; Range: 100 Hz to 100 kHz; BW: 100 Hz; Attenuator: 0 dB; Averages: 16; Marker: 50 kHz.

Design marker value: -100 +,- 10 dBm. Measured value:_____ Pass/Fail_____

File_____

b) **Fast path**: active probe at TP10; input not connected; Spectrum analyzer mode; Range: 100 Hz to 100 kHz; BW: 100 Hz; Attenuator: 0 dB; Averages: 16; Marker: 50 kHz.

Design marker value (TBD): _____Measured value:_____ Pass/Fail_____

File_____

END_____